



STP4NC80Z - STP4NC80ZFP STB4NC80Z - STB4NC80Z-1

N-CHANNEL 800V - 2.4Ω - 4A TO-220/FP/D²PAK/I²PAK
Zener-Protected PowerMESH™III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP4NC80Z/FP	800V	< 2.8 Ω	4 A
STB4NC80Z/-1	800V	< 2.8 Ω	4 A

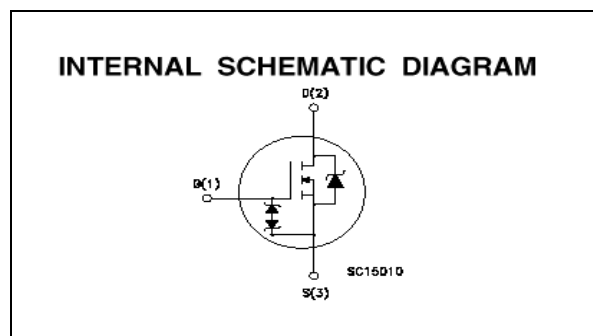
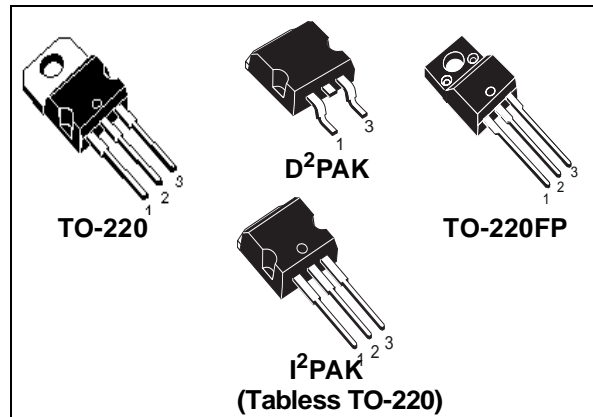
- TYPICAL R_{DS(on)} = 2.4 Ω
- EXTREMELY HIGH dv/dt AND CAPABILITY GATE-TO- SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW GATE INPUT RESISTANCE
- GATE CHARGE MINIMIZED

DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP4NC80Z	P4NC80Z	TO-220	TUBE
STP4NC80ZFP	P4NC80ZFP	TO-220FP	TUBE
STB4NC80ZT4	B4NC80Z	D ² PAK	TAPE & REEL
STB4NC80Z-1	B4NC80Z	I ² PAK	TAPE & REEL

STP4NC80Z - STP4NC80ZFP - STB4NC80Z - STB4NC80Z-1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)4NC80Z(-1)	STP4NC80ZFP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	800		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	800		V
V _{GS}	Gate- source Voltage	± 25		V
I _D	Drain Current (continuous) at T _C = 25°C	4	4(*)	A
I _D	Drain Current (continuous) at T _C = 100°C	2.5	2.5(*)	A
I _{DM} (•)	Drain Current (pulsed)	16	16(*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	100	35	W
	Derating Factor	0.8	0.28	W/°C
I _{GS}	Gate-source Current	±50		mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15KΩ)	2.5		KV
dv/dt(1)	Peak Diode Recovery voltage slope	3		V/ns
V _{ISO}	Insulation Winthstand Voltage (DC)	--	2000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 4A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

(*)Pulse width Limited by maximum temperature allowed

THERMAL DATA

		TO-220 / D ² PAK / I ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	1.25	3.57	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	30		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	4	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	225	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	800			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 1 mA, V _{GS} = 0		0.9		V/°C
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating			1	μA
		V _{DS} = Max Rating, T _C = 125 °C			50	μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	μA

STP4NC80Z - STP4NC80ZFP - STB4NC80Z - STB4NC80Z-1

ELECTRICAL CHARACTERISTICS (CONTINUED)

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$, $I_D = 2 A$		2.4	2.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 2A$		4		S
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $f = 1 MHz$, $V_{GS} = 0$		1200		pF
C_{oss}	Output Capacitance			90		pF
C_{riss}	Reverse Transfer Capacitance			11		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 400 V$, $I_D = 2 A$ $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		27		ns
t_r	Rise Time			10		ns
Q_g	Total Gate Charge	$V_{DD} = 640V$, $I_D = 4A$, $V_{GS} = 10V$		27	36.5	nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 640V$, $I_D = 4 A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 5)		11		ns
t_f	Fall Time			10		ns
t_c	Cross-over Time			24		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				16	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 4 A$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4 A$, $di/dt = 100A/\mu s$, $V_{DD} = 50V$, $T_j = 150^\circ C$ (see test circuit, Figure 5)		560		ns
Q_{rr}	Reverse Recovery Charge			3.4		μC
I_{RRM}	Reverse Recovery Current			13		A

STP4NC80Z - STP4NC80ZFP - STB4NC80Z - STB4NC80Z-1

GATE-SOURCE ZENER DIODE

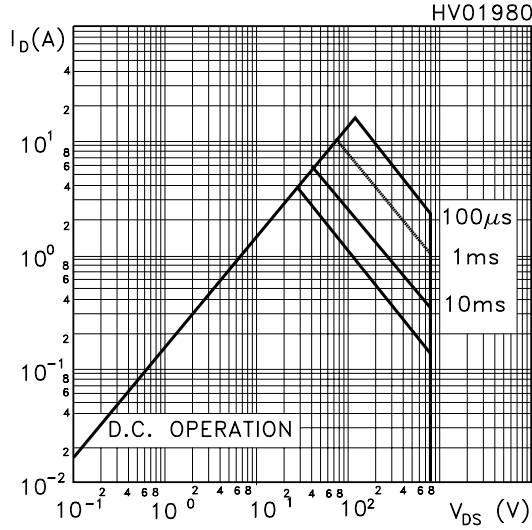
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	25			V
αT	Voltage Thermal Coefficient	T=25°C Note(3)		1.3		$10^{-4}/^{\circ}\text{C}$
Rz	Dynamic Resistance	$I_D = 50\text{mA}$,		90		Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $\Delta V_{BV} = \alpha T (25^{\circ} - T) BV_{GSO}(25^{\circ})$

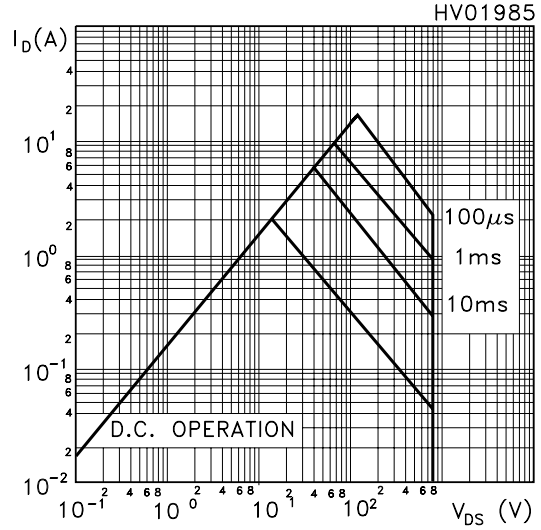
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

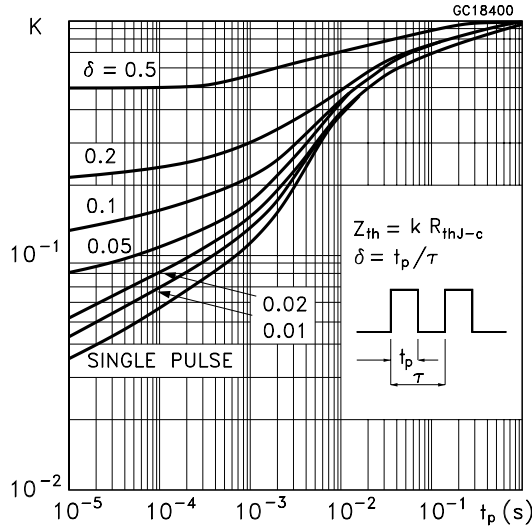
Safe Operating Area For TO-220/D²PAK/I²PAK



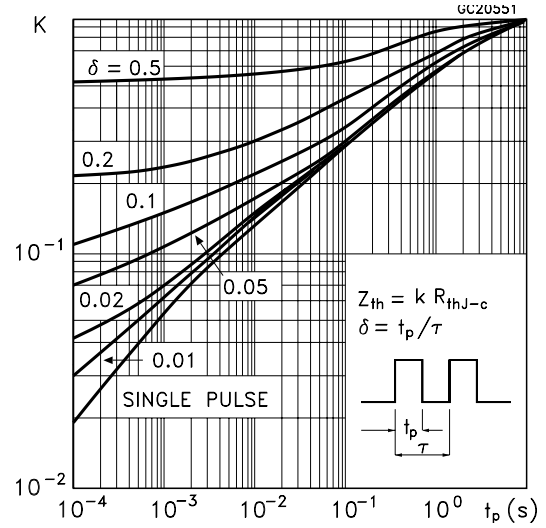
Safe Operating Area For TO-220FP



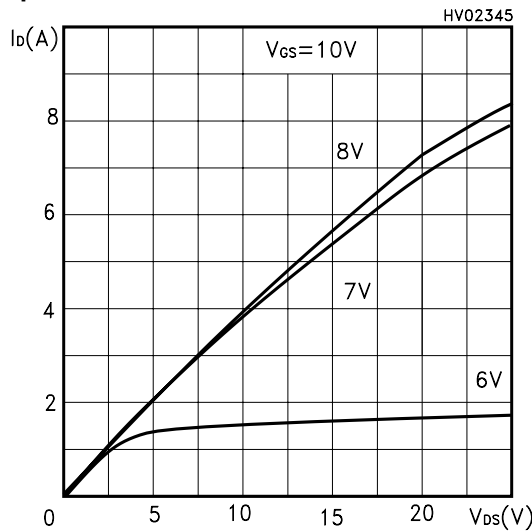
Thermal Impedance For TO-220/D²PAK/I²PAK



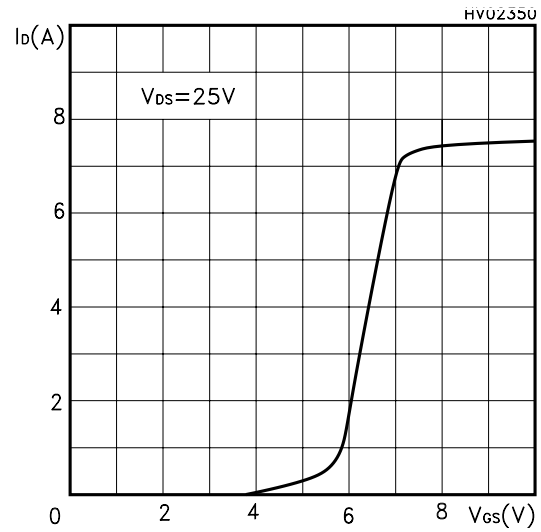
Thermal Impedance For TO-220FP



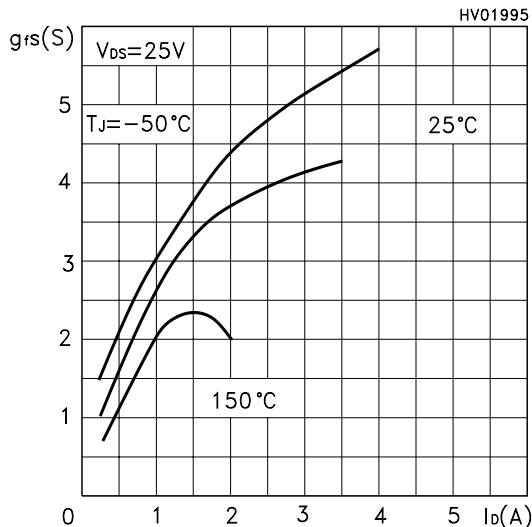
Output Characteristics



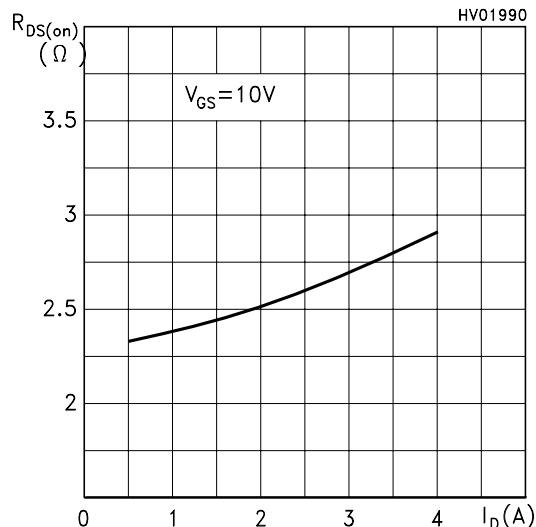
Transfer Characteristics



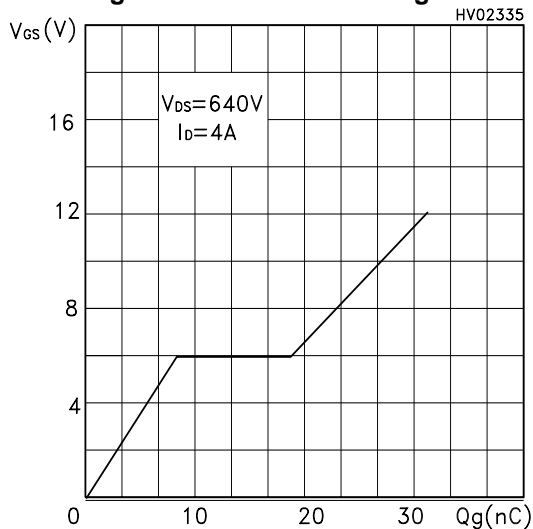
Transconductance



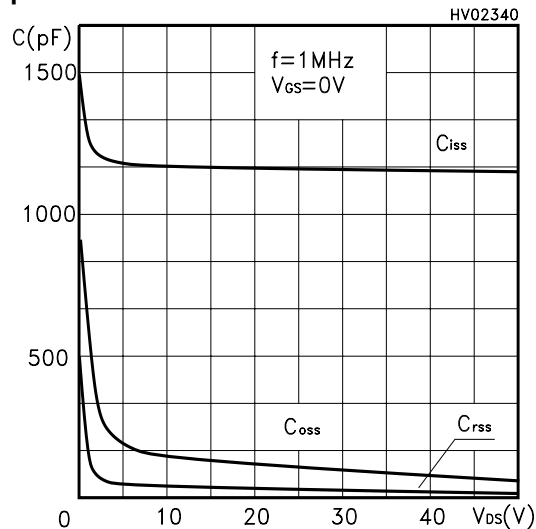
Static Drain-source On Resistance



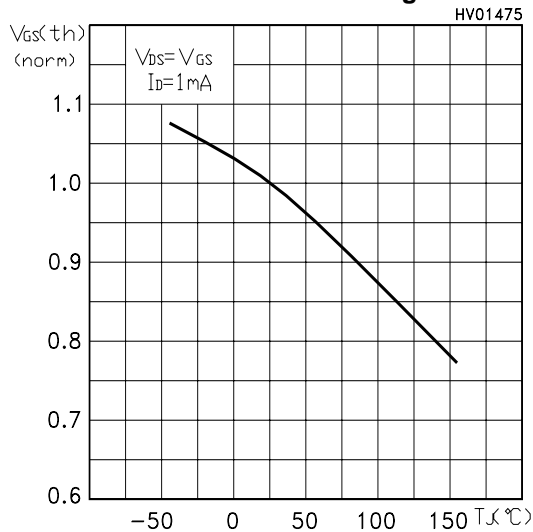
Gate Charge vs Gate-source Voltage



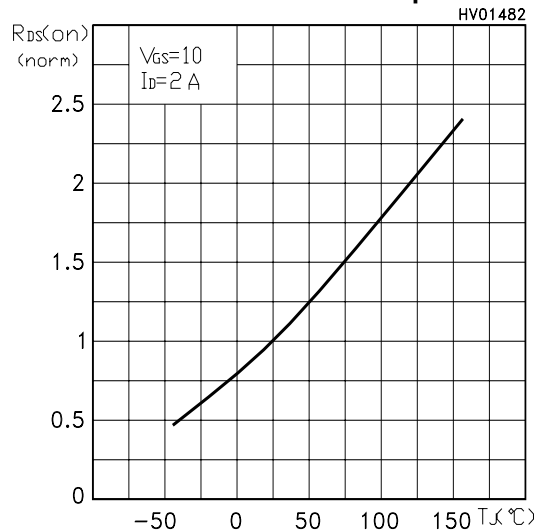
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

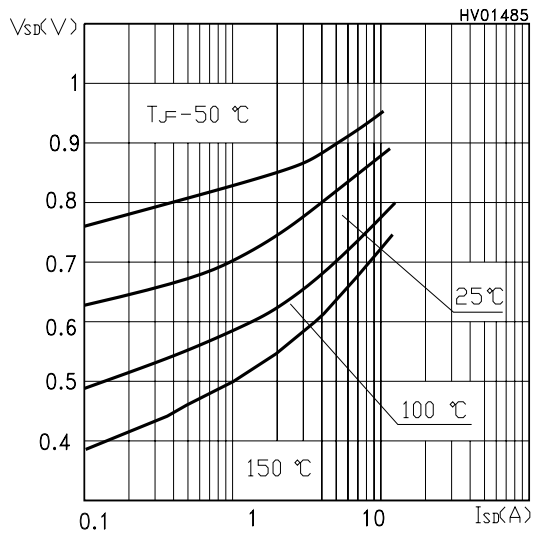


Fig. 1: Unclamped Inductive Load Test Circuit

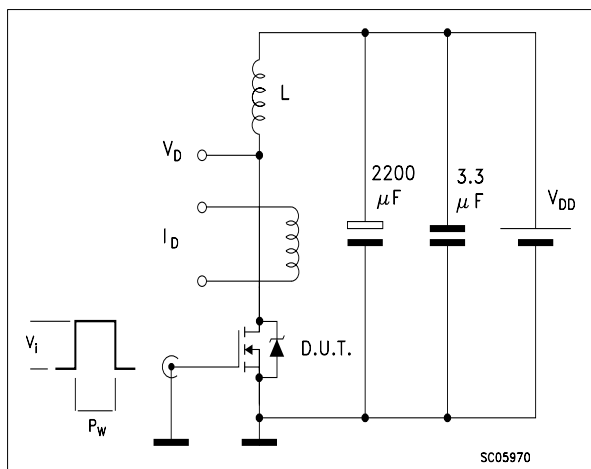


Fig. 2: Unclamped Inductive Waveform

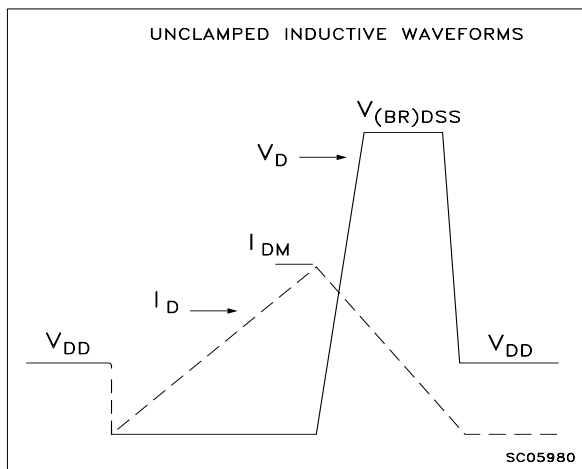


Fig. 3: Switching Times Test Circuits For Resistive Load

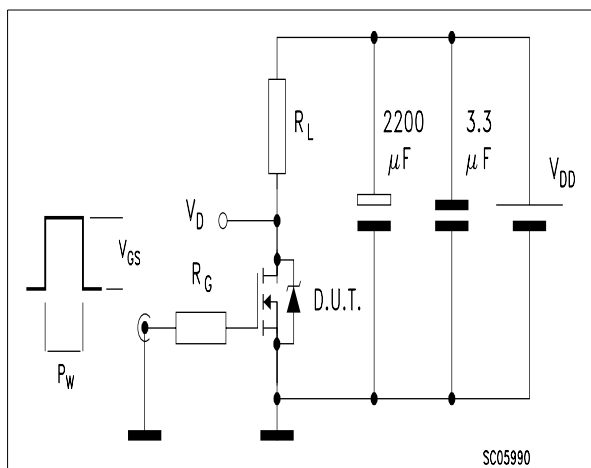


Fig. 4: Gate Charge test Circuit

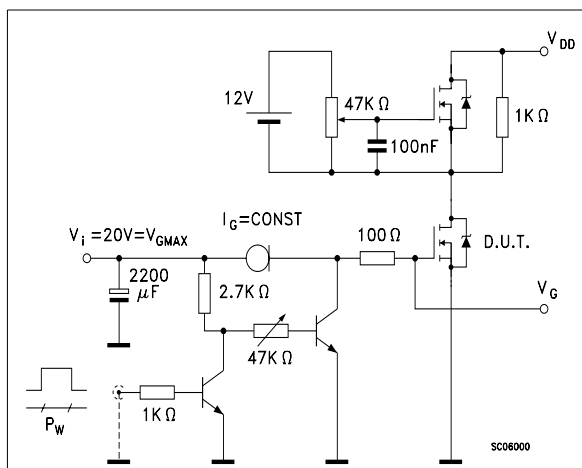
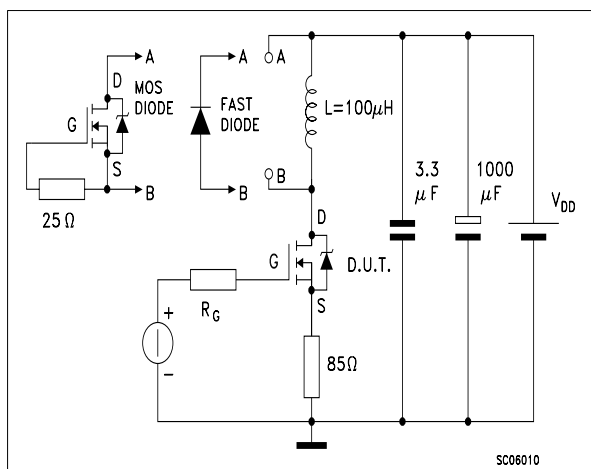
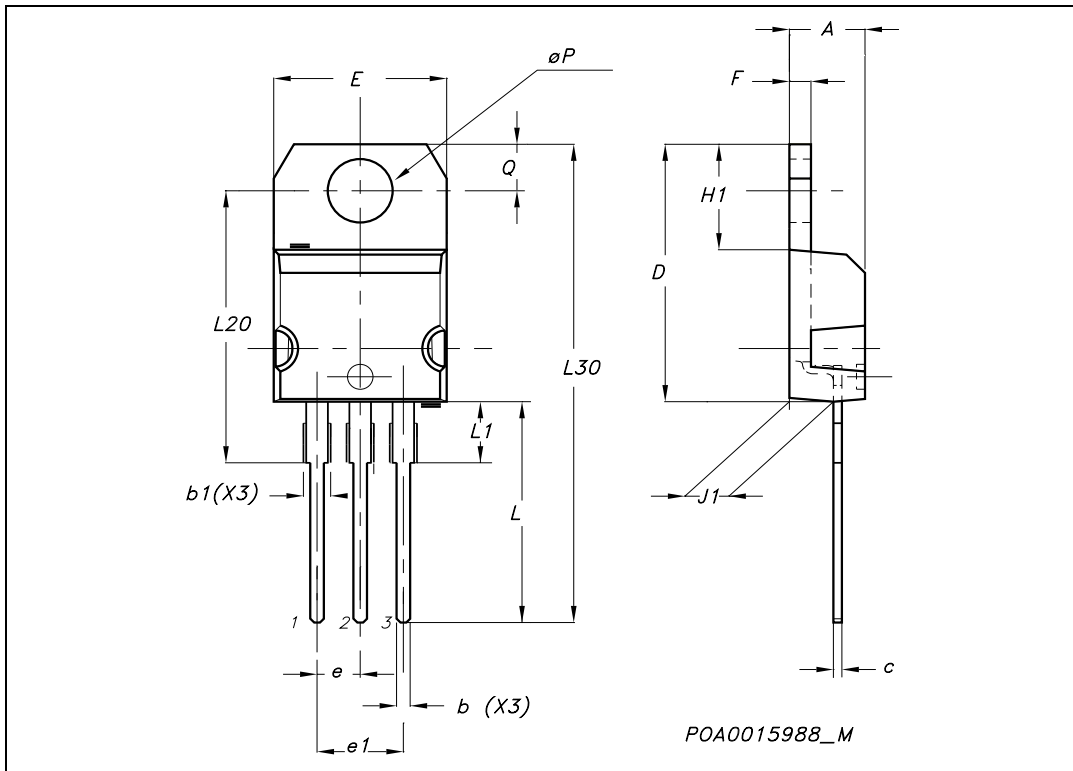


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



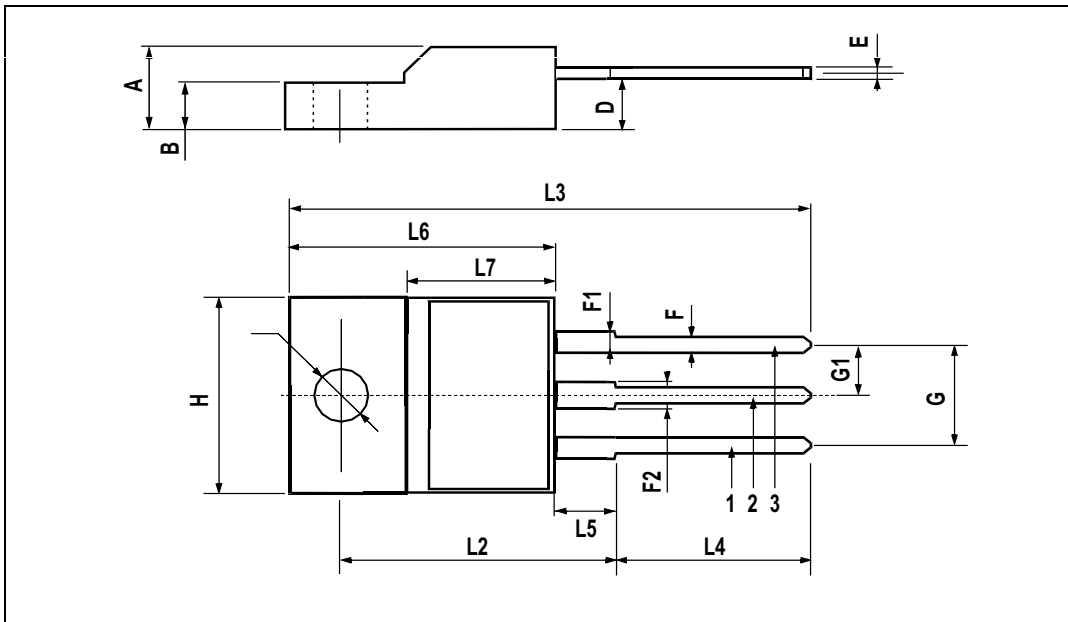
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



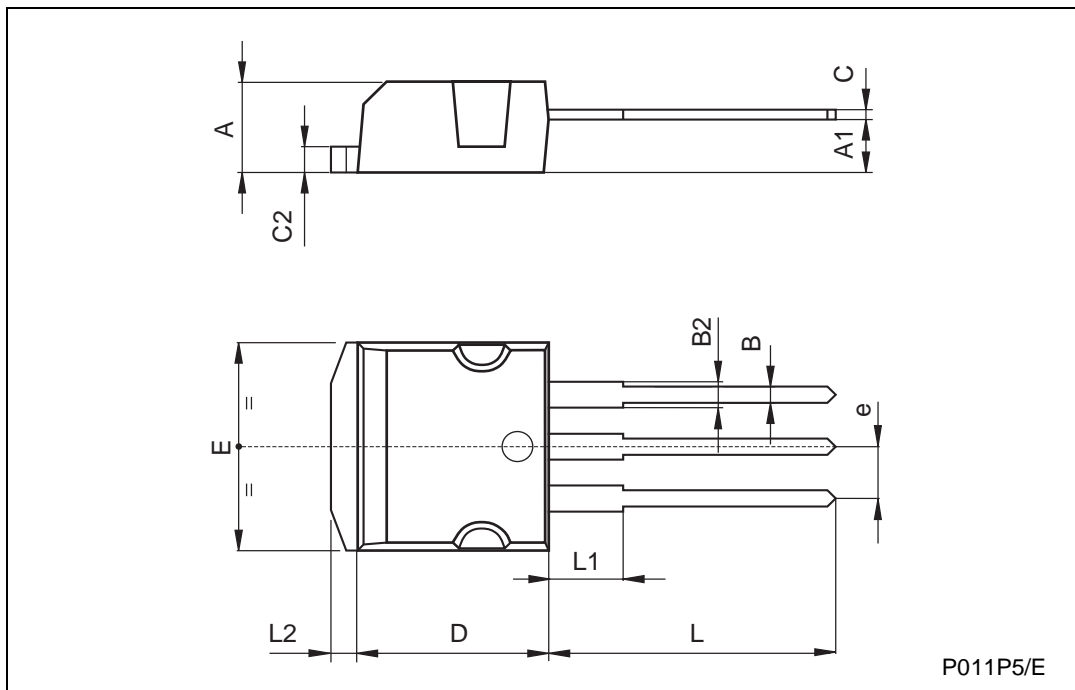
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



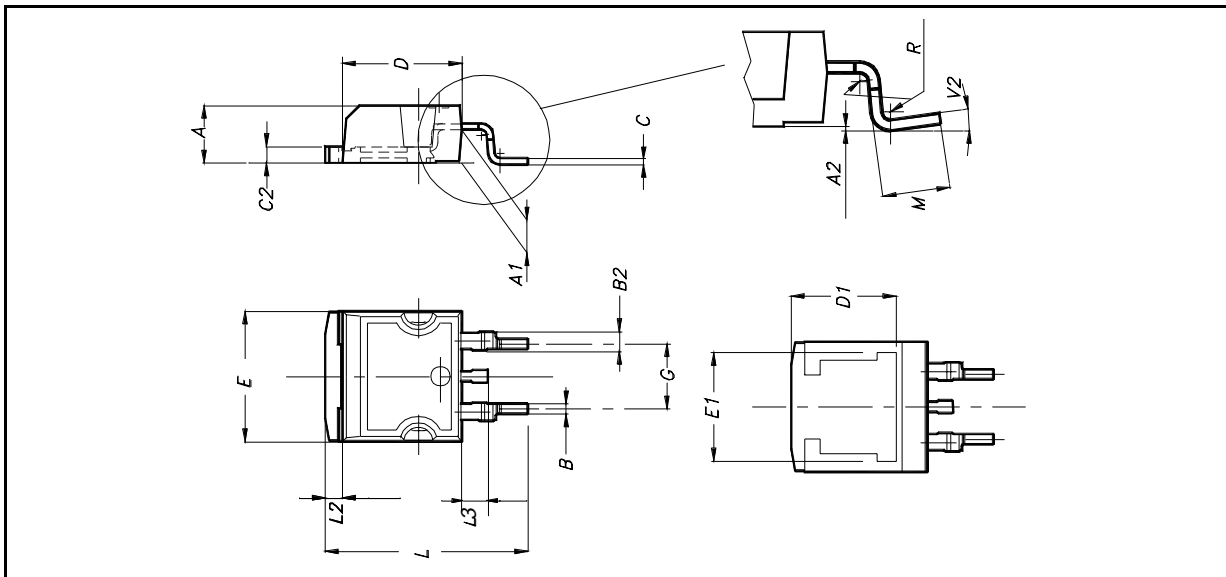
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>