SUMMIT MICROELECTRONICS, Inc.

SMD1102 / 1103 / 1113

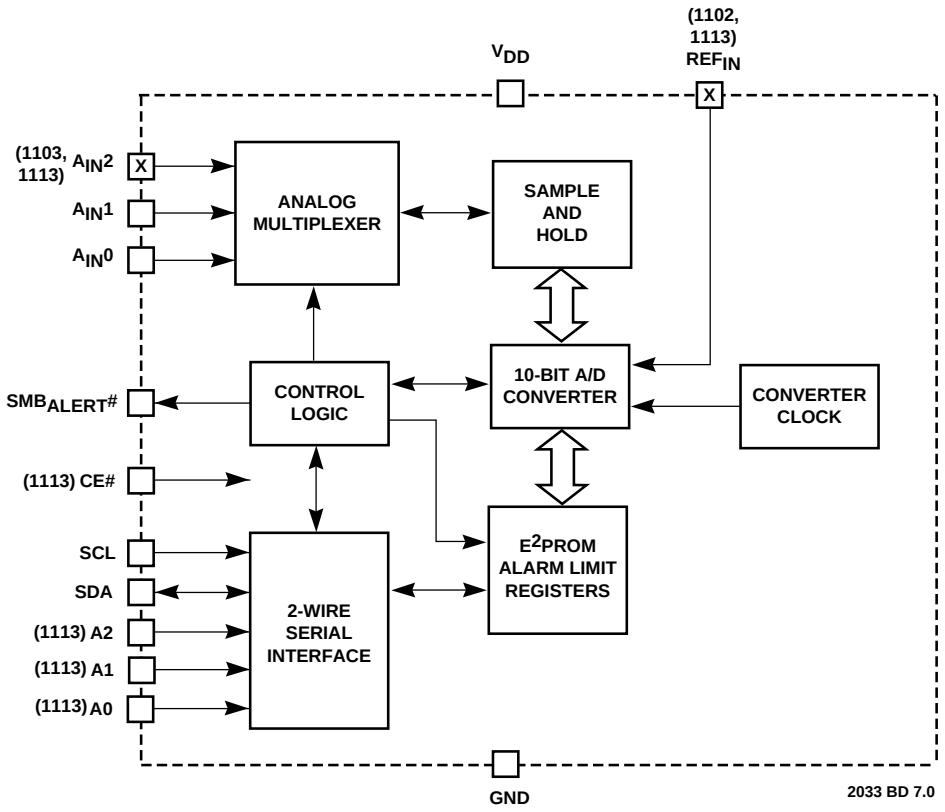
10-Bit Data Acquisition System for Autonomous Environmental Monitoring

Preliminary

FEATURES

- Complete Data Acquisition System
  - 10-Bit A/D Converter Resolution
  - 75µs Acquisition plus Conversion Time
  - Alarm Limits for Each Input Channel
  - Auto-Increment of Input Channels
  - Two Wire I^2C Serial Data Interface
  - System Management Bus (SMBus) Compatible
  - Auto-Monitor with SMB_{ALERT} Output
  - Low Quiescent Current of 50µA
  - Wide Supply Voltage Range: 2.7V to 5.5V
- SMD1102
  - 2-Channel Analog Input
  - External Voltage Reference Input Provided for Absolute Measurements
- SMD1103
  - 3-Channel Analog Input
  - Reference Voltage Input for the A/D Converter is Connected to V_{DD} for Ratiometric Measurements
- SMD1113
  - Extended I^2C Operation
  - 3-Channel Analog Input
  - External Voltage Reference Input Provided for Absolute Measurements

FUNCTIONAL BLOCK DIAGRAM



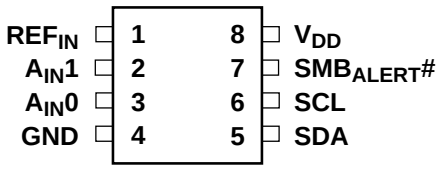
Note: See Pin Configuration drawings for pinouts

INTRODUCTION

The SMD1102, SMD1103 and SMD1113 each contain a 10-Bit data acquisition system (DAS) with dedicated EEPROM alarm limit storage. The three devices communicate with the host µP via a standard two-wire I^2C serial interface. After initialization the SMD1102/1103/1113 can automatically monitor one or more analog input channels. If any input signal moves beyond its user-programmed limits the host is notified by the SMB_{ALERT}# output, enabling fault prediction in telecom line card applications, as an example.

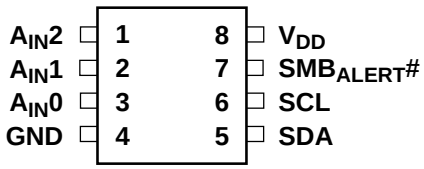
PIN CONFIGURATION

8-Pin PDIP
or 8-Pin SOIC
SMD1102



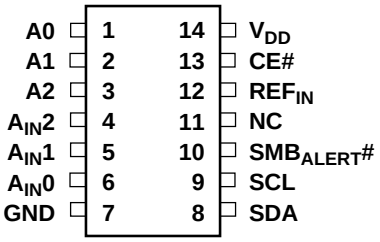
2033 8 PCon-2

8-Pin PDIP
or 8-Pin SOIC
SMD1103



2033 8 PCon-3

14-Pin SOIC
SMD1113



2033 14 PCon

PIN NAMES

1102

$A_{IN}0$, $A_{IN}1$	Analog channel inputs
GND	Power supply return
REF_{IN}	Reference input
SCL	Serial Clock
SDA	Serial Data
SMB_{ALERT}#	Interrupt output
V_{DD}	Power Supply

1103

$A_{IN}0$, $A_{IN}1$, $A_{IN}2$	Analog channel inputs
GND	Power supply return
SCL	Serial Clock
SDA	Serial Data
SMB_{ALERT}#	Interrupt output
V_{DD}	Power Supply

1113

CE#	Chip Enable
A2, A1, A0	I^2C Address select inputs
$A_{IN}0$, $A_{IN}1$, $A_{IN}2$	Analog channel inputs
GND	Power supply return
REF_{IN}	Reference input
SCL	Serial Clock
SDA	Serial Data
SMB_{ALERT}#	Interrupt output
V_{DD}	Power Supply

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 seconds) ..... 300 °C
Terminal Voltage with Respect to GND:
All ..... –2V to 7V

*COMMENT

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Conditions (Note 1)	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.7		5.5	V
I_{CC}	Supply Current	All outputs open			3	mA
I_{SB}	Standby Current	All outputs open, ADC idle, no memory write in process		50		µA
I_{LI}	Input leakage current	V_{IN} = 0V to V_{CC}			2	µA
I_{LO}	Output leakage current	V_{OUT} = 0V to V_{CC}			10	µA
V_{OL}	Output low voltage	V_{CC} = 5V, I_{OL} = 2.1mA			0.4	V
		V_{CC} < 4.5V, I_{OL} = 1mA			0.2	
V_{OH}	Output high voltage	V_{CC} = 5V, I_{OL} = –400µA	2.4			V
		V_{CC} < 4.5V, I_{OL} = –100µA	V_{CC} – 0.2			
V_{IL}	Input low voltage		–0.1		$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage		$0.7 \times V_{CC}$		V_{CC} + 0.7	V
Analog Inputs						
V_{REFIN}	V_{REF} input voltage		1		V_{CC}	V
V_{IN}	Input voltage on $A_{IN}0$ through $A_{IN}2$		0		5.5	V

2033 Elect Table

RECOMMENDED OPERATING CONDITIONS

Temperature	–40ºC to 85ºC.
Voltage	2.7V to 5.5V

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock data into and out of the device. In the WRITE mode data must remain stable while SCL is HIGH. In the READ mode data is clocked out on the falling edge of SCL.

Serial Data (SDA)

The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except during START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

SMB_{ALERT}#

This interrupt output pin signals the host when an out-of-limit condition is detected by one of the EEPROM limit registers. The SMB_{ALERT} open-drain output is active low.

REF_{IN}

Voltage reference input for 10-Bit A/D converter. This signal is only on the SMD1102 and SMD1113.

$A_{IN}0$, $A_{IN}1$, $A_{IN}2$

Multiplexer input pins for channels 0, 1, and 2, respectively. $A_{IN}2$ is only available on the SMD1103 and SMD1113. These pins may be left unconnected if they are not used. However, the Alert Regions must be set accordingly (see the section "Alert Conditions").

A0, A1, A2

The address inputs are only available on the SMD1113. Multiple SMD1113s can be used on a single bus by setting different device addresses. A2 has a 50kΩ pull-up resistor, and A1 and A0 have 50kΩ pull-down resistors. Do not set the address to all zeroes because it would cause a conflict with the SMB Alert Response.

CE#

Chip Enable/disable input must be held low to enable I^2C communications. It has a 50kΩ pull-down resistor and is only available on the SMD1113.

V_{DD}

Power supply input.

GND

Power supply return.

DEVICE OPERATION

The SMD1102, SMD1103 and SMD1113 Data Acquisition Systems (DAS) are each comprised of: an analog input multiplexer, sample-and-hold circuit, 10-Bit successive approximation Analog-to-Digital (A/D) Converter, and nonvolatile EEPROM memory to store upper and lower alarm-limits for each input channel. The user programs the alarm limits via the industry-standard I^2C interface. An SMB_{ALERT}# interrupt output signals if any of the analog inputs move outside these limits.

DAS Modes of Operation

The SMD1102/1103/1113 have four user-selectable modes of operation. These modes are: a single conversion of one channel, successive conversions on the same channel, sequential conversions on all three channels, or autonomous conversions of the same or all channels.

Sample-and-Hold Operation

The channel switching and sampling architecture of the A/D's comparator is illustrated in the equivalent input circuit diagram in Figure 1. During acquisition the selected channel charges a capacitor in the sample-and-hold circuit. The acquisition interval spans the Acknowledge period following the command byte and ends on the rising edge of the next clock. At the end of the acquisition phase the analog input is disconnected, retaining charge on the hold capacitor as a sample of the signal.

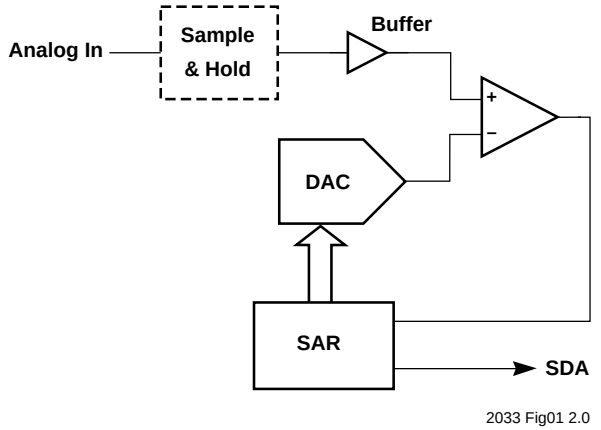


Figure 1. Sample/Hold and SAR

Addressing and Command Sequence

All operations of the DAS are preceded first by the start condition and then by the addressing command sequence. For the SMD1102 & SMD1103 this is 1001_{BIN}. For the SMD1113 it is the binary values of A2, A1, A0, and a one — a four bit number.

The next bit in the addressing sequence is the EEPROM/Conversion (E/C) bit; when set to zero the device is instructed to perform an A/D conversion, and when set to logic one the EEPROM limit register will be addressed. See Table 1A.

The next two bits are the channel select bits. Auto-increment is enabled if the channel select bits are set to 11_{BIN} and the conversion bit is set to zero. In the auto-increment mode conversions are performed on successive channels, starting with channel 0. After channel 2 is converted (channel 1 on the SMD1102) the address will wrap around to channel 0. See Table 1B.

The last bit is the Read/Monitor bit. When the bit is set to logic one, data can be read from a conversion or from one of the EEPROM limit registers, depending on the state of the EEPROM/Conversion bit. When the bit is logic zero either the auto-monitor mode is entered or the EEPROM limit register is programmed, again depending on the state of the EEPROM/Conversion bit. See Table 1C.

DB7	DB6	DB5	DB4	DB3	Function
Device Type Identifier				E/C	
A2 or 1*	A1 or 0*	A0 or 0*	1	0	Perform A/D conversion on selected channel(s)
				1	Address EEPROM limit register

2033 Table01A

* Denotes SMD 1102 & SMD1103. Ax bits are for the SMD1113.

Table 1A. Address Byte — EEPROM/Conversion

DB7	DB6	DB5	DB4	DB2	DB1	Function
Device Type Identifier				CH1	CH0	
A2 or 1*	A1 or 0*	A0 or 0*	1	0	0	Channel 0 selected
				0	1	Channel 1 selected
				1	0	Channel 2 selected
				1	1	Auto-increment if E/C = 0

2033 Table01B

* Denotes SMD 1102 & SMD1103. Ax bits are for the SMD1113.

Table 1B. Address Byte — Channel Select

DB7	DB6	DB5	DB4	DB0	Function
Device Type Identifier				R/M	
A2 or 1*	A1 or 0*	A0 or 0*	1	0	Enable auto-monitor or write EEPROM limit register (E/C state)
				1	Read A/D conversion or EEPROM limit register (E/C state)

2033 Table01C

* Denotes SMD 1102 & SMD1103. Ax bits are for the SMD1113.

Table 1C. Address Byte — Read/Monitor

Single Channel Conversions

This command sequence is composed of: the Device Type Identifier, followed by the E/C bit set to zero, then the channel select bits set to the desired value, and the R/M bit set to logic one. After the R/M bit is clocked in the host releases the SDA line and monitors the SDA line for an acknowledge bit (ACK) from the SMD1102/1103/1113. The device will drive the SDA line low indicating it received the command and that it has initiated the acquisition and conversion on the selected channel. The clock source for the acquisition and conversion is an internal clock. After the ACK the SMD1102/1103/1113 will output four dummy zeros on SDA followed by an echo of the channel's 2 address bits. The remaining bits in this first byte are the two MSBs of the conversion. Refer to Figure 2 for a detailed illustration of this sequence, and for that of retrieving the remaining conversion byte. The host can issue a stop condition after retrieving the conversion data and place the SMD1102/1103/1113 in a low power standby mode.

Successive Single Channel Conversions

If the host does not issue a stop command after receiving the last bit of the previous conversion, but instead issues an ACK and continues clocking, then the SMD1102/1103/1113 will begin another acquisition and conversion process on the same channel.

Auto-Increment

In the auto-increment mode, the DAS starts a conversion and then automatically advances to the next channel. The auto-increment mode always starts at channel 0 and switches the channel input in the sequence 0, 1, 2, 0, 1, 2, *etc.* after each successive conversion. The SMD1102, SMD1103, and SMD1113 independently repeat this process so long as the host continues clocking the device, supplies ACK bits at the appropriate clock interval, and issues no stop conditions. Refer to Figure 4 for a detailed illustration of the sequence.

Programming the Limit Registers

Programming the nonvolatile limit registers of the SMD1102/1103/1113 for use with the auto-monitor function is straightforward. Associated with each channel is an 11-bit lower limit register and an 11-bit upper limit register. Ten bits correspond to the 10-bit data, and the MSB represents the monitor option bit. The monitor option bits of the upper and lower limit combine to define the alert region for each channel (described more fully in the section labeled Alert Conditions). Each limit register must be programmed separately with a three byte command sequence. To program the limit register the host first issues a start condition, followed by the device type identifier, the EEPROM/Conversion (E/C) bit (set to one), the channel select bits, and the Read/Monitor bit (set to zero). The second byte consists of four zeroes followed by the limit select bit (zero = lower limit, one = upper limit), the monitor option bit, and the two most significant bits of the limit data. The third byte consists of the remaining eight bits of limit data. After receiving a stop condition, the SMD1102/1103/1113 initiates its internal program sequence. Refer to Figure 5 for details. Six such sequences are required to set the upper and lower limits for all three channels. However, once programmed the data remains stored in EEPROM until reprogrammed.

For example, when a device has both V_{DD} and V_{REF} at 5.00V, and an alert must be generated if the voltage on any channel is ≤2.00V or >3.00V, then the monitor option bits are set to 10_{BIN}, the upper limit is set to 266_{HEX}, and the lower limit is set to 199_{HEX}.

Reading the Limit Registers

The timing diagram for reading the limit register data of a particular channel is shown in Figure 6. The five byte sequence commences with a start condition, followed by the device type identifier, the EEPROM/Conversion bit (set to one), the channel select bits, and the Read/Monitor bit (set to one). After acknowledging the slave byte the device outputs a one, followed by an echo of the channel select bits, a zero, another zero (representing the lower limit data), the monitor option bit and the two most significant bits of the limit data. The third byte consists of the remaining eight bits of the lower limit data. The fourth byte of the output sequence is the same as the second byte except the fifth bit is a one (to indicate upper

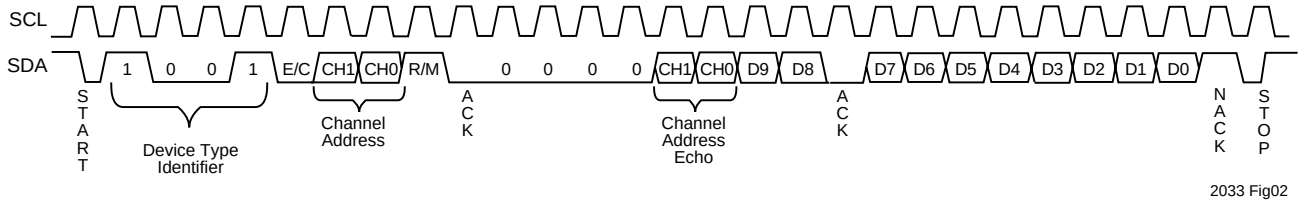


Figure 2. Single Channel Read Sequence

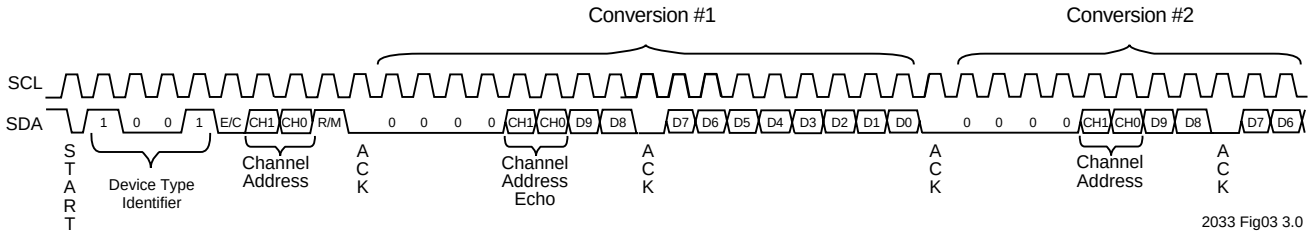


Figure 3. Single Channel Continuous Read Sequence

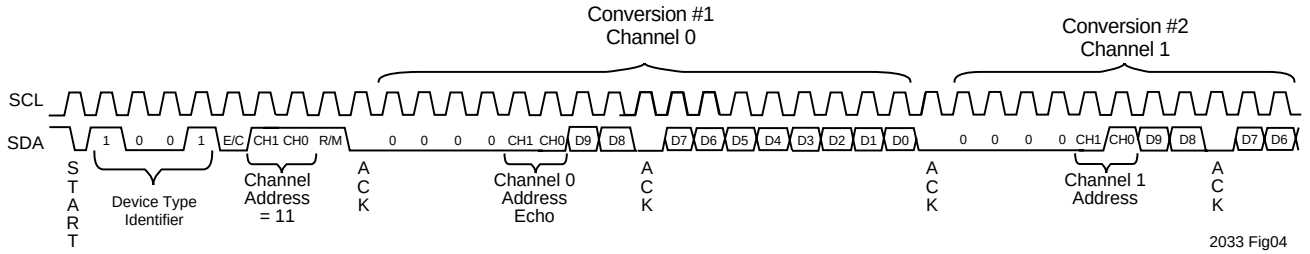


Figure 4. Auto-Increment Continuous Read Sequence

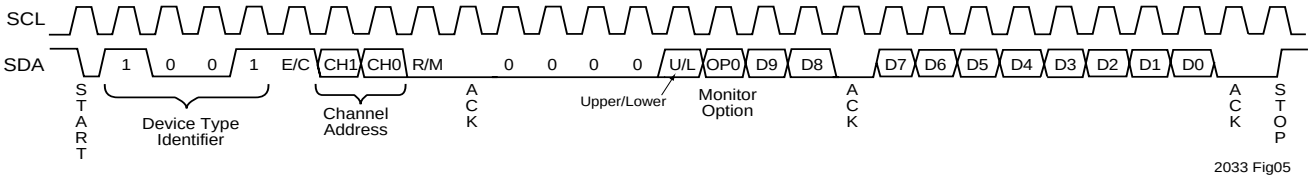


Figure 5. Programming the Auto-Monitor Limit Registers

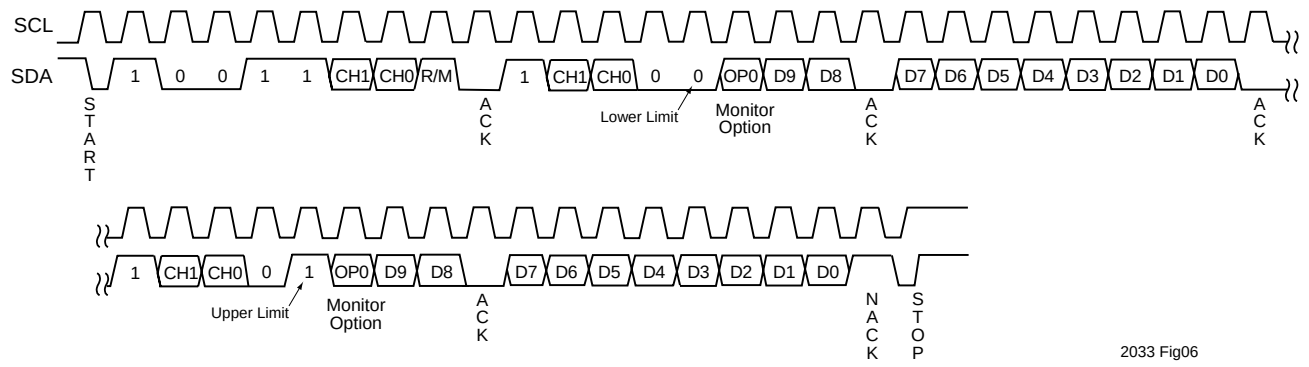


Figure 6. Reading the Auto-Monitor Limit Registers

limit data is forthcoming), and the data bits are from the upper limit. The fifth and final byte represents the remaining eight bits of the upper limit data.

Auto-Monitor

Auto-Monitor operation takes full advantage of the unique capabilities of the SMD1102/1103/1113. Each device can autonomously monitor the analog channels, compare the conversion data against stored, nonvolatile limit registers, and, if necessary, alert the host to out-of-limit conditions. The command string to enter the Auto-Monitor mode is shown in Figure 7. It consists of a start condition followed by the device type identifier (slave address), the EEPROM/Conversion bit set to zero, the channel select bits, and the Read/Monitor bit set to zero. After Acknowledge the host issues a Stop condition in order to initiate the Auto-Monitor process. Setting the channel select bits to a particular channel limits the monitoring to that channel. Setting the channel select bits to "11" allows all three inputs to be monitored in succession (auto-increment). In the case of the 1102 the limit registers for channel 2 should be set so that the alert cannot be generated from this channel (see the following section "Alert Conditions"). The Auto-Monitor operation must be terminated before further communication with the device. The Auto-Monitor function is automatically shut down when an alert is asserted. Any Read operation will also halt Auto-Monitor, and, if an alert has occurred, it will clear the alert along with the stored information of the channel that prompted the alert.

Note: a Read operation that is used to halt the Auto-Monitor function will not return valid data.

Alert Conditions

For each channel the host can select one of four conditions that will generate an alert while Auto-Monitor is active. These conditions are determined by the option bits stored with the upper and lower limits in the NV registers. Figure 8 details these conditions. If an out-of-limit condition is detected the SMD1102/1103/1113 will temporarily remove itself from the auto-increment mode (if that was selected), and monitor the channel that caused the alert. There must be five successive conversions resulting in an out-of-limit condition before the SMD1102/1103/1113 will signal an alert. If at any time during the verify routine the out-of-limit condition is negated the SMD1102/1103/1113 will re-enter its Auto-Monitor routine. If a valid alert condition has been detected the device will halt the Auto-Monitor function and await instructions from the host.

If any one of the channels is not being used while the Auto-Monitor function is enabled that channel must have its alert conditions as well as its limit registers set so that it does not cause an alert. This is accomplished by first setting the alert region inside the limits (*i.e.*, set monitor option bits to either 10_{BIN} or 11_{BIN}), and then setting the lower limit above the upper limit.

Alert Response

The SMD1102, SMD1103 and SMD1113 are considered slave devices. They do not generate clocks on the SCL pin or take control of bus activity. However, the SMBus specification, an extension of the I^2C specification, does allow slave devices the ability to generate interrupts to get the attention of the host by pulling SMB_{ALERT}# low.

After the SMD1102/1103/1113 has issued an alert by pulling SMB_{ALERT}# low the alert can only be reset by addressing the device. If there is more than one device on the SMBus capable of generating an alert, the host may determine the offending device by issuing an Alert Response Address (ARA). The ARA is a general call to all devices, but only an SMBus compatible device will recognize the call, and only a device that generated an interrupt will respond to the call. The DAS responds by acknowledging the ARA, and then by sending its device address on the SDA line, as shown in Figure 9. Embedded in the device address is the channel that caused the alert. If more than one SMBus compliant device has responded to the ARA, standard I^2C bus arbitration allows the device with the lowest address to be serviced first.

Note: The device address of an SMD1113 should not be set with A2, A1 and A0 all equal to zero. This would create an address conflict with the SMB_{ALERT}# broadcast message.

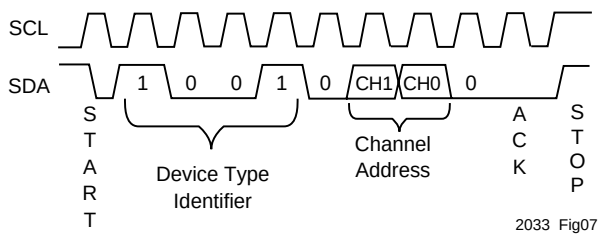


Figure 7. Begin Auto-Monitor Command

Once the SMB_{ALERT}# signal has been asserted it must be reset before further communication with the device, with the exception of the SMB_{ALERT}# response sequence. Resetting the SMB_{ALERT}# is accomplished by performing a read operation.

Figure 10 shows the SMB_{ALERT}# signal being reset by a Read operation.

Note: a Read operation that is used to reset the SMB_{ALERT}# will not return valid data.

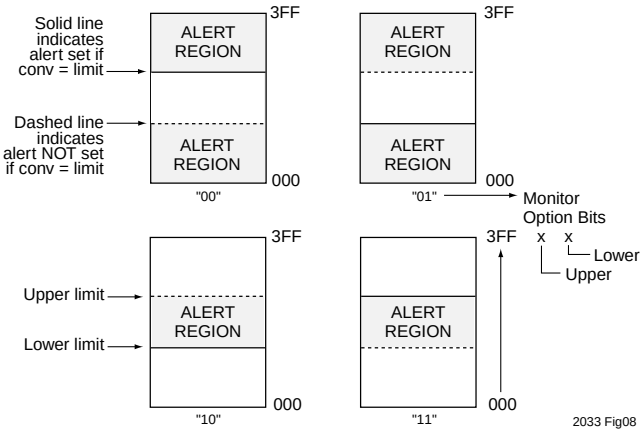


Figure 8. Four Alert Conditions

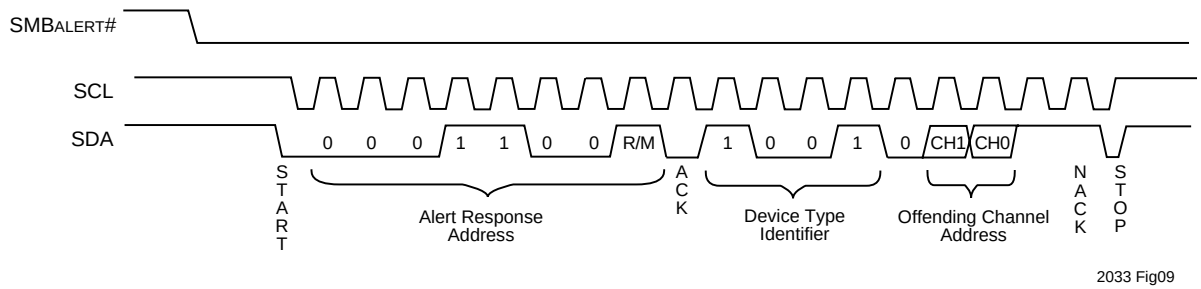


Figure 9. SMB_{ALERT}# Response Sequence

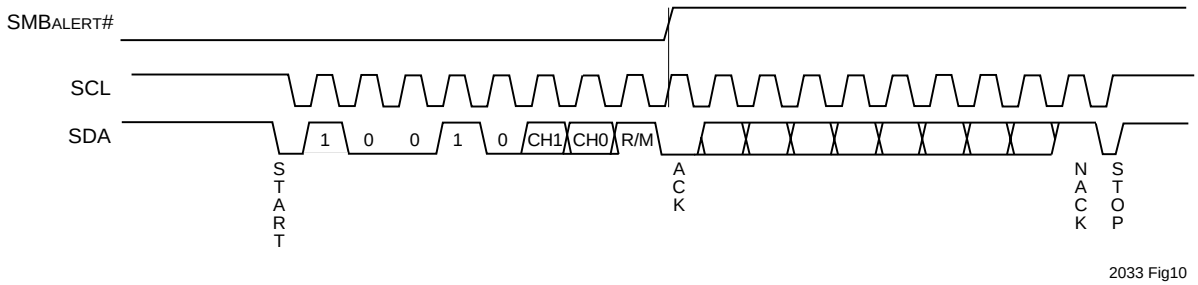


Figure 10. Resetting SMB_{ALERT}#

BUS INTERFACE

GENERAL DESCRIPTION

The I^2C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial Data line (SDA) and a serial Clock line (SCL). All Summit Microelectronics parts support a 100kHz clock rate, and some support the alternative 400kHz clock. Check Table 2 for the value of f_{SCL}. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. Summit parts have a Schmitt input on both lines. See Figure 11 and Table 2 for waveforms and timing on the bus. One bit of Data is transferred during each Clock pulse. The Data must remain stable when the Clock is high.

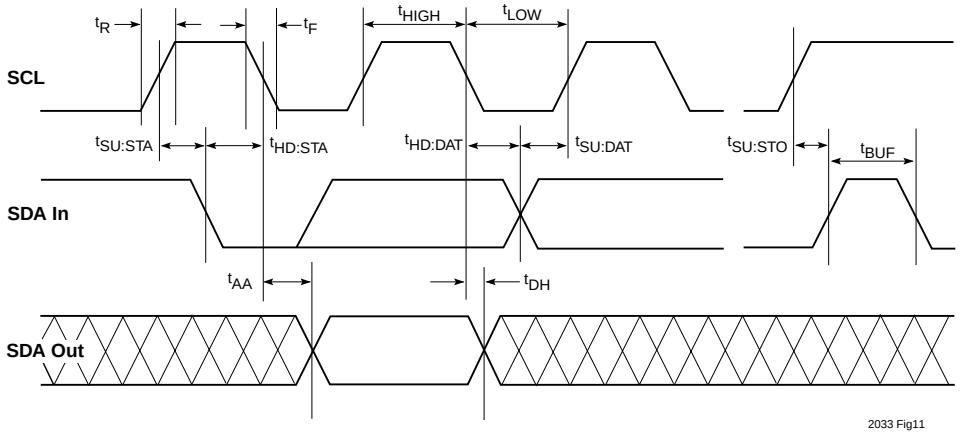


Figure 11. Interface Bus Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time (1)	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time (1)		250		ns
$t_{HD:DAT}$	Data In hold time (1)		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2033 Table02

Note (1) These values are guaranteed by design.

Table 2. Register Read/Write AC Operating Characteristics

Start and Stop Conditions

Both Data and Clock lines remain high when the bus is not busy. Data transfer between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the Data line while the Clock line is high is defined as a Start condition. A low-to-high transition of the Data line while the Clock line is high is defined as a Stop condition. See Figure 12.

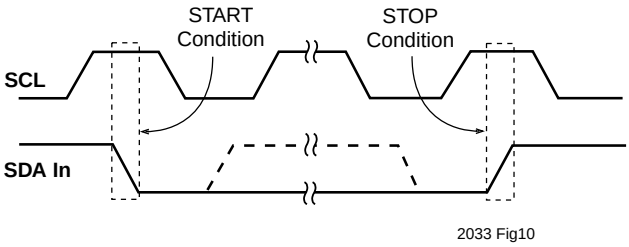


Figure 12. Start and Stop Conditions

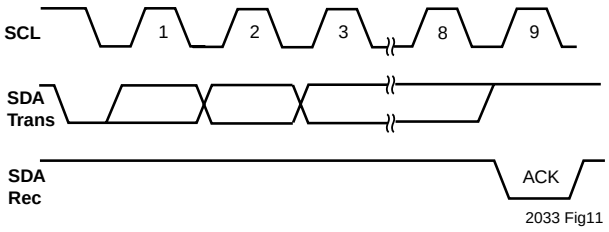


Figure 13. Acknowledge Timing

Protocol

The protocol defines any device that sends data onto the bus as a Transmitter, and any device that receives data as a Receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the Summit Microelectronic devices are slave devices, since they never initiate any data transfers.

Acknowledge

Data is always transferred in 8-Bit bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The Transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the Receiver will pull the SDA line low to Acknowledge that it received the eight bits of data (See Figure 13). The termination of a Master Read sequence is indicated by a non-Acknowledge (NACK), where the Master will leave the Data line high.

In the case of a Read from a Summit part, when the last byte has been transferred to the Master, the Master will leave the Data line high for a NACK. This will cause the Summit part to stop sending data, and the Master will issue a Stop on the clock pulse following the NACK.

In the case of a Write to a Summit part the Master will send a Stop on the clock pulse after the last Acknowledge. This will indicate to the Summit part that it should begin its internal nonvolatile write cycle.

Read and Write

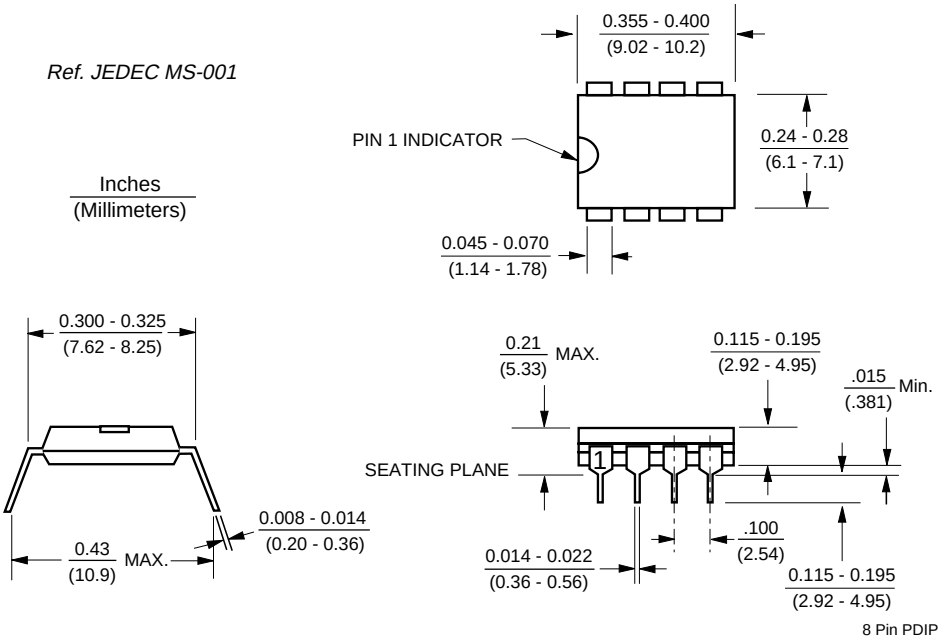
The first byte from a Master is always made up of the eight bits illustrated in Table 1.

In the read mode the SMD1102/1103/1113 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no STOP condition is generated by the Master, the device will continue to transmit data. If an Acknowledge is not detected (NACK), the device will terminate further data transmission.

In the write mode the SMD1102/1103/1113 receives eight bits of data, then generates an Acknowledge signal. It will continue to generate ACKs until a STOP condition is generated by the Master.

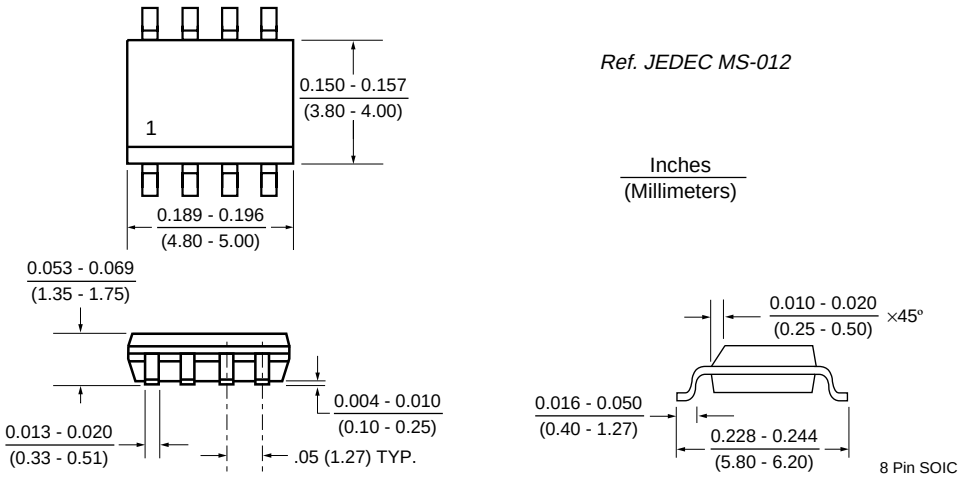
PACKAGES

8 PIN PDIP PACKAGE



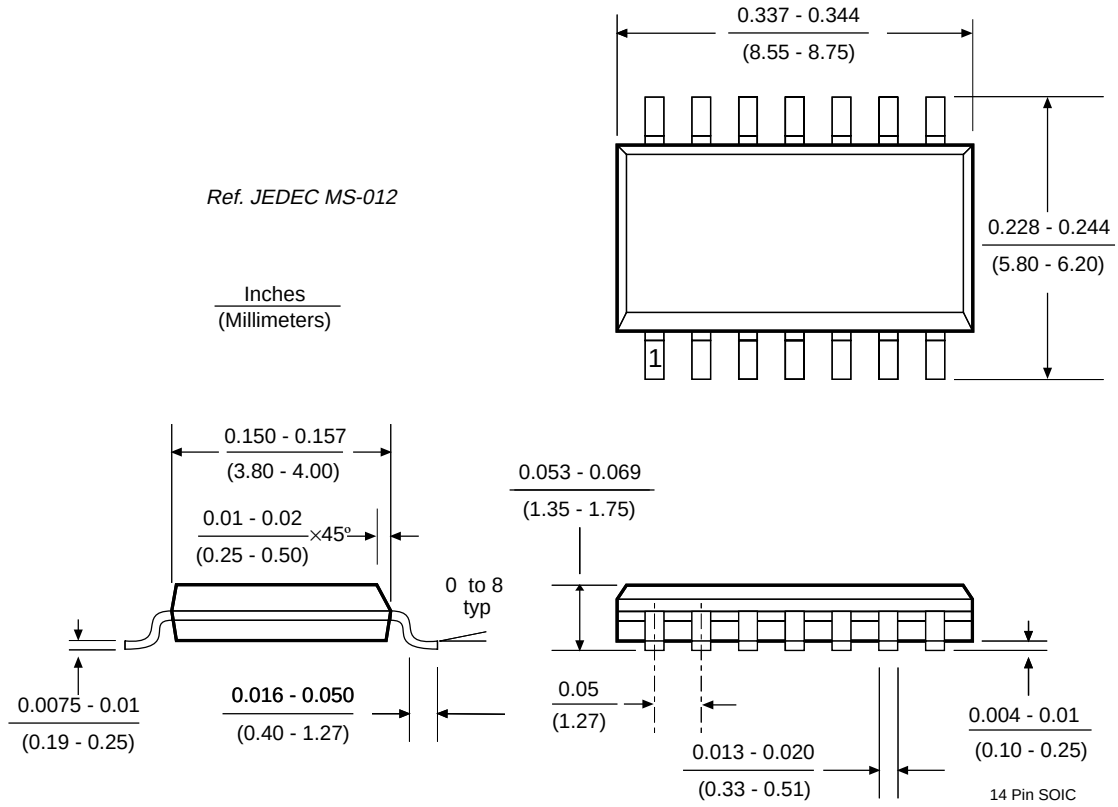
8 Pin PDIP

8 PIN SOIC PACKAGE



8 Pin SOIC

14 PIN SOIC PACKAGE



ORDERING INFORMATION

SMD110 2 S

Base Part Number

Type
2 = REF_{IN}
3 = $A_{IN}2$

Package
S = SOIC
P = PDIP

2033 Tree 8

SMD1113 S

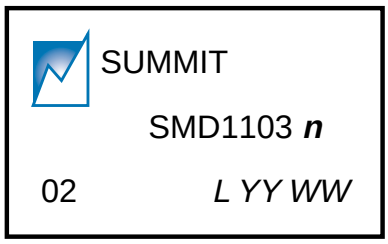
Base Part Number

Package
S = SOIC

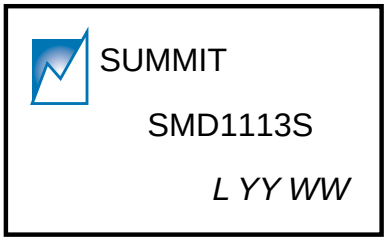
2033 Tree 14

PART MARKING

SMD1102

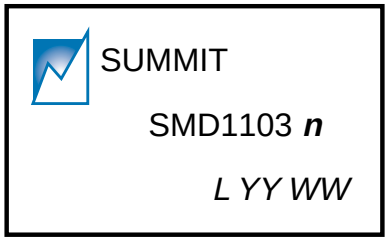


SMD1113



Package type - SOIC (S)
L = Lot number
YY = Year
WW = Work Week

SMD1103



n = Package type (P or S)
L = Lot number
YY = Year
WW = Work Week

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