SUMMIT MICROELECTRONICS, Inc.

SMH4804

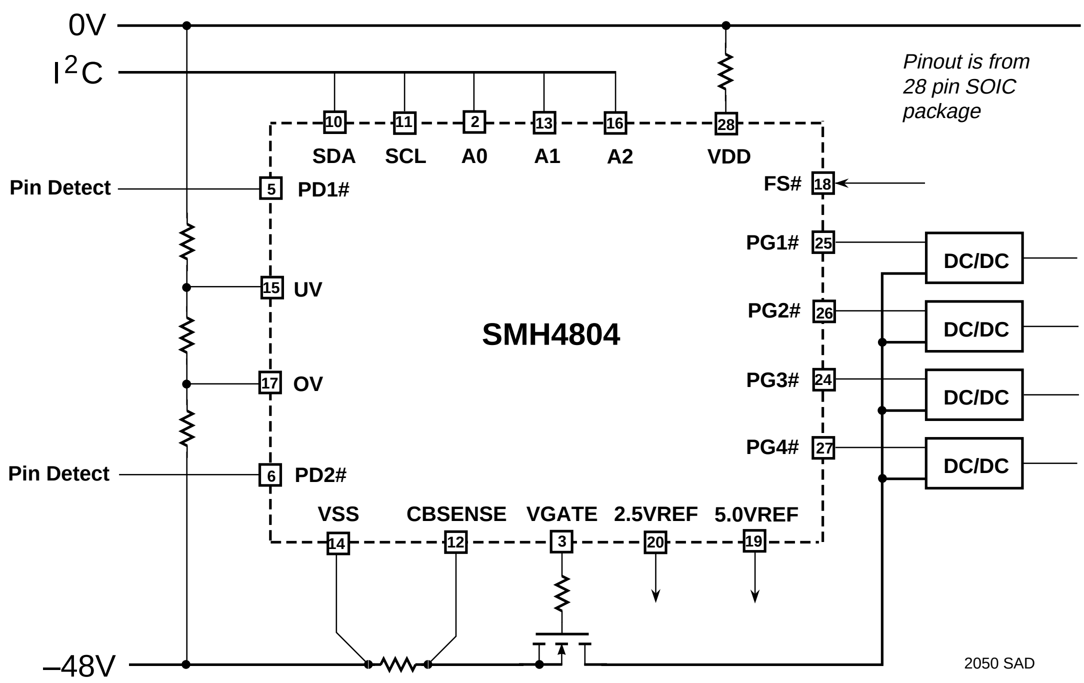
Preliminary

User-Programmable Nonvolatile Distributed Power Hot Swap Controller with Forced Shutdown

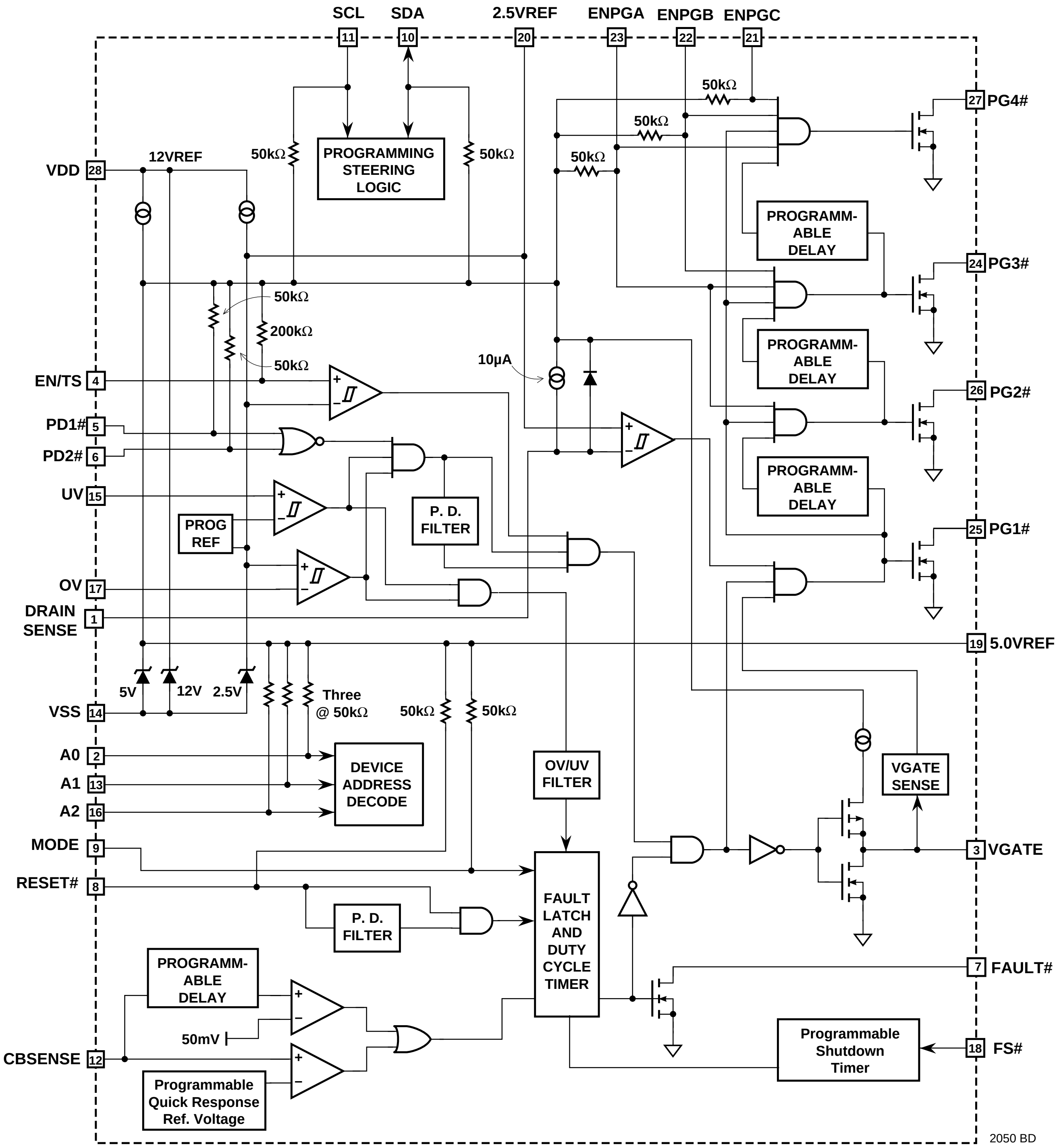
FEATURES

- Soft Starts Main Power Supply on Card Insertion or System Power Up
- Senses Card Insertion via Short Pins or Ejector Switches
- Master Enable to Allow System Control of Power Up or Down
  - Can be used as a Temperature Sense Input
- Programmable Independent Controls of 4 DC/DC Converters
  - Not Enabled until Host Supply Fully Soft Started
  - Programmable Time Delay Between each Enable Signal
  - Available Input to hold off Dependant Enables until Conditions are Satisfied
- Highly Programmable Circuit Breaker
  - Programmable Quick-Trip™ Values
  - Programmable Current Limiting
  - Programmable Circuit Breaker Mode: Latched (Volatile or Nonvolatile)
  - Programmable Duty Cycle Times
  - Programmable Over-current Filter
- Programmable Host Voltage Fault Monitoring
  - Programmable Under- voltage Hysteresis
  - Programmable UV/OV Voltage Filter
  - Programmable Fault Mode: Latched or Duty Cycle
- Programmable Forced Shutdown Timer
- 2.5V and 5.0V Reference Outputs
  - Eliminates the Need or Other Primary Voltages
  - Easy Expansion of External Monitor Functions
- Internal Shunt Regulator Allows a Wide Supply Range

SIMPLIFIED APPLICATION DRAWING



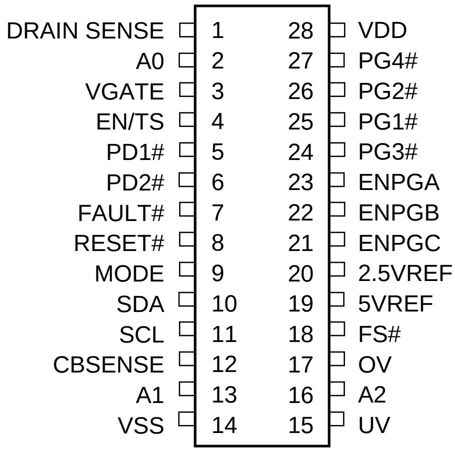
FUNCTIONAL BLOCK DIAGRAM



Pinout is from the 28 pin SOIC package.

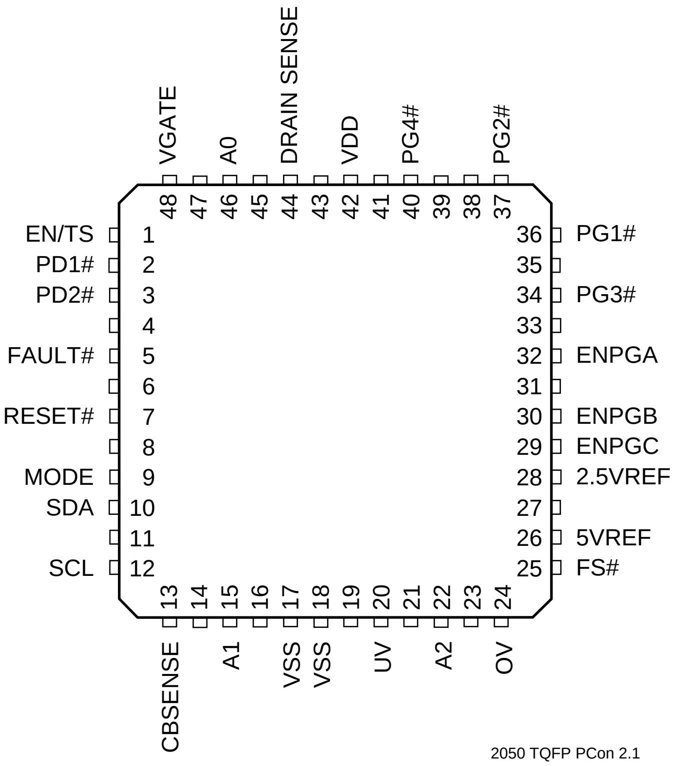
PIN CONFIGURATIONS

28-Pin SOIC



2050 SOIC PCon 2.1

48-Pin TQFP



2050 TQFP PCon 2.1

Note: TQFP pins left blank are all no connect.

DESCRIPTION

The SMH4804 is designed to control hot swapping of plug-in cards operating in a distributed power environment. The distributed power rail can range from 20V to 500V. The SMH4804 hot-swap controller provides under-voltage and over-voltage monitoring of the host power supply. It also drives an external power MOSFET switch that connects the supply to the load and protects against over-current conditions that might disrupt the host supply. When the source and drain voltages of the external MOSFET are within specification the SMH4804 provides Power Good logic outputs that may be used to enable DC-DC converters. The four separate Power Good outputs activate loads in a timed sequence. Additional features of the device include: temperature sense or master enable input, 2.5V and 5V reference outputs for expanding monitor functions, two Pin-Detect enable inputs for card insertion verification, and duty-cycle or latched over-current protection modes. All of these features can be programmed through the two-wire interface.

Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

PIN DESCRIPTIONS

PD1# & PD2#

These are logic level active low inputs that can optionally be employed to enable VGATE and the PG outputs when they are at V_{SS}. These pins each have an internal 50kΩ pull-up to 5V.

UV

The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if UV is less than 2.5V. Programmable internal hysteresis is available on the UV input, adjustable in increments of 62.5mV. Also available is a filter delay on the UV input.

OV

The OV pin is used as an over-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if OV is greater than 2.5V. A filter delay is available on the OV input.

MODE

The state of the MODE signal determines how fault conditions are cleared. The device is in the latched mode when the signal is held at V_{SS}, and the cycle mode when held at 5V or left floating. This pin has an internal 50kΩ pull-up to 5V.

RESET#

RESET# is used to clear latched fault conditions. When this pin is held low the VGATE and PG outputs are disabled. Refer to the Circuit Breaker Operation and the associated timing diagrams for detailed characteristics. This pin has an internal 50kΩ pull-up to 5V.

CBSENSE

The circuit breaker sense input is used to detect over-current conditions across an external, low value sense resistor (R_S) tied in series with the Power MOSFET. A voltage drop of greater than 50mV across the resistor for longer than t_{CBD} will trip the circuit breaker. A programmable ***Quick-Trip***™ sense point is also available.

DRAIN SENSE

The DRAIN SENSE input monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. An internal 10µA source pulls the DRAIN SENSE signal towards the 5V reference level. DRAIN SENSE must be held below 2.5V to enable the PG outputs.

EN/TS

The Enable/Temperature Sense input is the master enable input. If EN/TS is less than 2.5V, VGATE will be disabled. This pin has an internal 200kΩ pull-up to 5V.

5VREF

This is a precision 5V output reference voltage that may be used to expand the logic input functions on the SMH4804. The reference output is with respect to V_{SS}.

2.5VREF

This is a precision 2.5V output reference voltage that may be used to expand the logic input functions on the SMH4804. The reference output is with respect to V_{SS}.

FAULT#

FAULT# is an open-drain, active-low output that indicates the fault status of the device.

VGATE

The VGATE output activates an external power MOSFET switch. This signal supplies a constant current output (100µA typical), which allows easy adjustment of the MOSFET turn on slew rate.

ENPGA

This is an active high input that controls the PG2#, PG3# and PG4# outputs. When ENPGA is pulled low the PG2#, PG3# and PG4# outputs are immediately placed in a high impedance state. When ENPGA is driven high or left floating PG2# will be driven low at a time period of t_{PGD} after PG1# has been active. This pin has an internal 50kΩ pull-up to 5V.

ENPGB

This is an active high input that controls the PG3# and PG4# outputs. When ENPGB is pulled low the PG3# and PG4# outputs are immediately placed in a high impedance state. When ENPGB is driven high or left floating PG3# will be driven low at a time period of t_{PGD} after PG2# has been active. This pin has an internal 50kΩ pull-up to 5V.

ENPGC

This is an active high input that controls the PG4# output. When ENPGC is pulled low the PG4# output is immediately placed in a high impedance state. When ENPGC is driven high or left floating PG4# will be driven low at a time period of t_{PGD} after PG3# has been active. This pin has an internal 50kΩ pull-up to 5V.

PG1# / PG2# / PG3# / PG4#

The PGn# pins are open-drain, active-low outputs with no internal pull-up resistor. They can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches $V_{DD} – V_{GT}$ and the DRAIN SENSE voltage is less than 2.5V. Each successive PG output is enabled t_{PGD} after its predecessor, provided also that the appropriate ENPGx input(s) are high. Voltage on these pins cannot exceed 12V, as referenced to V_{SS}.

FS#

The Forced Shutdown (FS#) pin is an active low input that causes VGATE and PG outputs to be shut down at any time after an internal hold-off timer has expired. The hold-off timer allows supervisory circuits on the secondary side (which are not powered up initially) to control shut down of the SMH4804 via an opto-isolator. This input has no pull-up resistor.

A0 / A1 / A2

These are logic level inputs used for decoding multiple devices on the serial bus. These pins each have an internal 50kΩ pull-up to 5V.

SDA

SDA is a bidirectional serial data I/O port. This pin has an internal 50kΩ pull-up to 5V.

SCL

SCL is the serial clock input. This pin has an internal 50kΩ pull-up to 5V.

V_{DD}

This is the positive supply input. An internal shunt regulator limits the voltage on this pin to approximately 12V with respect to VSS. A resistor must be placed in series with the V_{DD} pin to limit the regulator current (R_D in the application illustrations).

V_{SS}

This is connected to the negative side of the supply.

Note: The pin numbers for each signal are different on the two packages.

RECOMMENDED OPERATING CONDITIONS

Temperature –40°C to 85°C.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... –55°C to 125°C
Storage Temperature .... –65°C to 150°C
Lead Solder Temperature (10 seconds)............. 300 °C
Terminal Voltage with Respect to V_{SS}:

VGATE .... VDD + 0.7V

A0, A1, A2, MODE, RESET, ENPGA, ENPGB, ENPGC, FS# SDA, and SCL 7V

PD1#, PD2#, VDD, UV, OV, CBSENSE, DRAIN SENSE, EN/TS, FAULT#, PG1#, PG2#, PG3#, and PG4# 15V

*Comment

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to V_{SS}, except V_{GT}**)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	I_{DD} = 3mA	11	12	13	V
$5V_{REF}$	5V reference output	I_{DD} = 3mA	4.75	5.00	5.25	V
I_{LOAD5}	5V reference output current	I_{DD} = 3mA	–1		1	mA
$2.5V_{REF}$	2.5V reference output	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
$I_{LOAD2.5}$	2.5V reference output current	I_{DD} = 3mA	–0.2		1	mA
I_{DD} (2)	Power supply current		2		10	mA
V_{UV}	Under-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
V_{UVHYST}	Under-Voltage hysteresis	I_{DD} = 3mA		63		mV
V_{OV}	Over-Voltage threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
V_{OVHYST}	Over-Voltage hysteresis	I_{DD} = 3mA		10		mV
V_{GATE}	V_{GATE} output voltage				V_{DD}	V
I_{GATE}	V_{GATE} current output			100		µA
V_{SENSE}	DRAIN SENSE threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
I_{SENSE}	DRAIN SENSE current output	V_{SENSE} = V_{SS} (1)	9	10	11	µA
V_{CB}	Circuit breaker threshold	I_{DD} = 3mA	40	50	60	mV
V_{QCB}	Programmable Quick Trip circuit breaker threshold			200		mV
				100		mV
				60		mV
			Off			—
V_{ENTS}	EN/TS threshold	I_{DD} = 3mA (1)	2.475	2.500	2.525	V
$V_{ENTSHYST}$	EN/TS hysteresis	I_{DD} = 3mA		10		mV
V_{IH}	Input voltages: ENPGA/B/C, MODE, RESET#, PD1#, PD2#		3		$5V_{REF}$	V
V_{IL}			0		2	V
V_{OL}	Output low voltage: FAULT#	I_{OL} = 3mA	0		0.4	V
	Output low voltage: PG1#/2#/3#/4#	I_{OL} = 3mA	0		0.4	V
I_{IL}	Input current: PD1#, PD2#, EN/TS	V_{IL} = V_{SS}		100		µA
V_{GT}	Gate threshold		0.7	1.8	3.0	V

Note: (1) TA = 25ºC.
(2) This value is set by the R_D resistor.

2050 Elect Table

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The SMH4804 is an integrated power controller for hot swappable add-in cards. The device operates from a wide supply range and generates the signals necessary to drive isolated output DC/DC converters. A physical connection must first be made with the chassis to discharge any electrostatic voltage potentials when a typical add-in board is inserted into the powered backplane. The board then contacts the long pins on the backplane that provide power and ground. As soon as power is applied the device starts up, but does not immediately apply power to the output load. Under-voltage and over-voltage circuits inside the controller verify that the input voltage is within a user-specified range, and pin detection signals determine whether the card is seated properly.

These requirements must be met for a Pin Detect Delay period of t_{PDD}, after which time the hot-swap controller enables VGATE to turn on the external power MOSFET switch. The VGATE output is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the drain sense input. When drain sense drops below 2.5V, and VGATE gets above $V_{DD} - V_{GT}$, the power good outputs can begin turning on the DC/DC controllers. Power Good Enable inputs may be used to activate or deactivate specific output loads.

Steady state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controllers by shutting down the power MOSFET: an under-voltage or over-voltage condition on the host power supply; an over-current event detected on the CBSENSE input; a failure of the power MOSFET sensed via the DRAIN SENSE pin; the pin detect signals becoming invalid; the master enable (EN/TS) falling below 2.5V; the FS# input being driven low by events on the secondary side of the DC/DC controllers. The SMH4804 may be configured so that after any of these events occur the VGATE output shuts off and either latches into an off state or recycles power after a cooling down period, t_{CYC}.

Powering V_{DD}

The SMH4804 contains a shunt regulator on the V_{DD} pin that prevents the voltage from exceeding 12V. It is necessary to use a dropper resistor (R_D) between the host power supply and the V_{DD} pin in order to limit current into the device and prevent possible damage. The dropper resistor allows the device to operate across a wide range of system supply voltages, and also helps protect the device against common-mode power surges. Refer to the Applications Section for help on calculating the R_D resistance value.

System Enables

There are several enabling inputs, which allow a host system to control the SMH4804. The Pin Detect pins (PD1# & PD2#) are two active low enables that are generally used to indicate that the add-in circuit card is properly seated. These inputs must be held low for a period of t_{PDD} before a power-up sequence may be initiated. This is typically done by clamping the inputs to V_{SS} through the implementation of an injector switch, or alternatively through the use of a staggered pins at the card-cage interface. Two shorter pins arrayed at opposite ends of the connector force the card to be fully seated (not canted) before both pin detects are enabled. Care must be taken not to exceed the maximum voltage rating of these pins during the insertion process. Refer to details in the Applications Section for proper circuit implementation.

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input. This input signal must exceed 2.5V (nominal) for proper operation.

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistive divider ladder to sense whether or not the host supply voltage is within the user-defined limits. The power-up sequence will be initiated if the input to the UV pin rises above 2.5V or if the input to the OV pin falls below 2.5V for a period of at least t_{PDD}. The t_{PDD} filter helps prevent spurious start-up sequences while the card is being inserted. If UV falls below 2.5V or OV rises above 2.5V, the PG and VGATE outputs will be shut down immediately.

Under-/Over-Voltage Filtering

The SMH4804 may also be configured so that an out of tolerance condition on UV/OV will not shut off the output immediately. Instead, a filter delay may be inserted so that only sustained under-voltage or over-voltage conditions will shut off the output. An out of tolerance condition on UV/OV for longer than the filter delay time (t_{UOFLTR}) causes the VGATE and PG outputs to shut off when the UV/OV filter option is enabled. The Under-/Over-Voltage Filtering feature is disabled in the default configuration of the device.

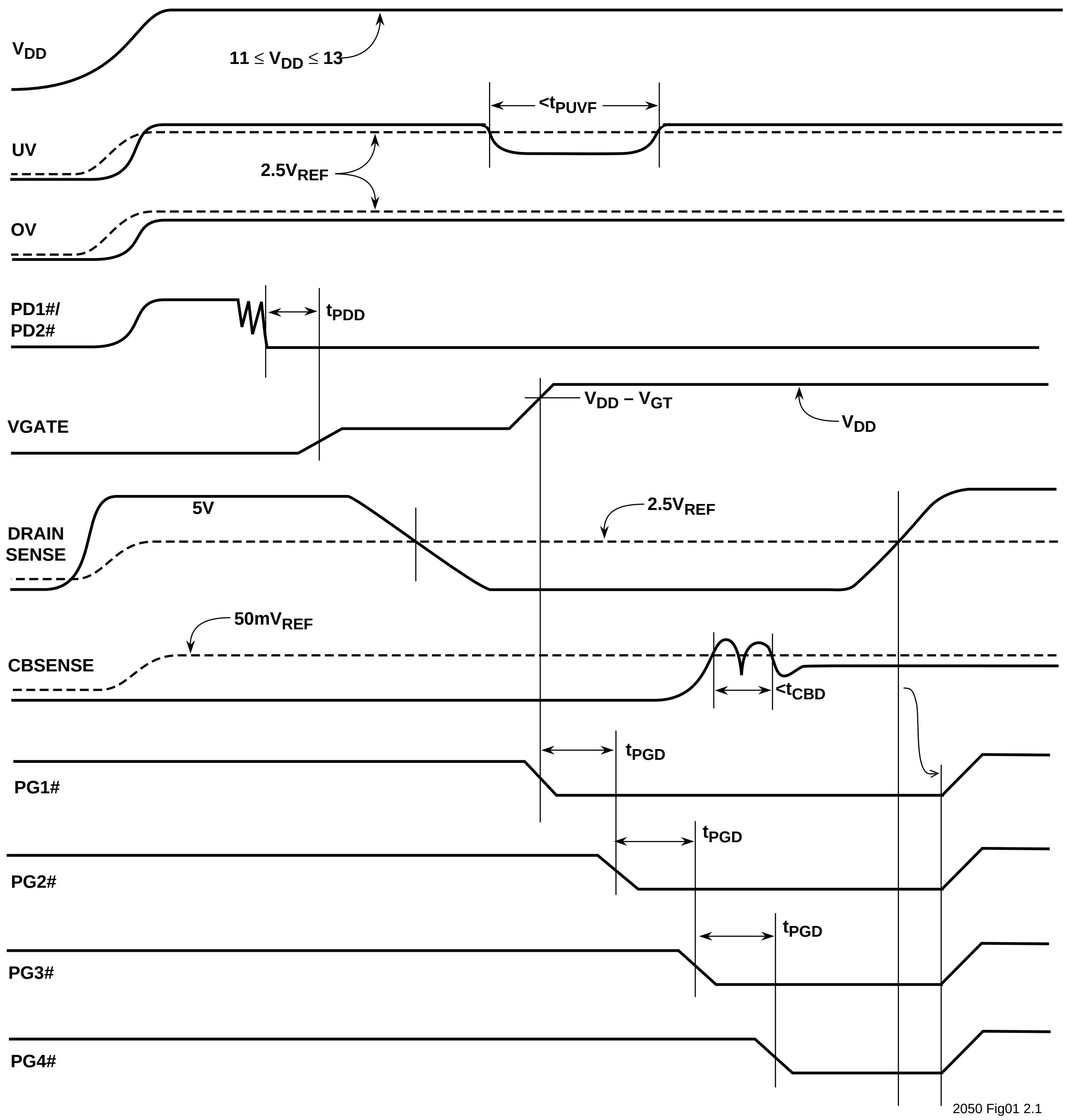


Figure 1. Power On Timing Sequence

TIMING RELATIONSHIPS

Figure 1 illustrates some of the power on sequences, including the UV and OV differentials to their reference, and Power Good cascading.

Figures 2, 3, 4, and 5 indicate the affect on the VGATE signal caused by different Circuit Breaker inputs. In Figure 2 RESET# and MODE are high; in Figure 3 MODE is high; in Figure 4 MODE is low. Figure 5 shows the Quick Trip mode.

Under-/Over-Voltage Latching

An additional option for an out of tolerance condition on UV/OV is to latch the VGATE and PG outputs off such that a return to normal UV/OV operation will not turn them back on. The FAULT# output will be set. Refer to the following section titled "Resetting FAULT#".

Under-Voltage Hysteresis

The Under-Voltage comparator input may be configured with a programmable level of hysteresis. The falling voltage compare level may be set in steps of 62.5mV below 2.5V. The rising voltage compare level is fixed at 2.5V. The default under-voltage hysteresis level is set to 62.5mV. In default conditions the SMH4804 is not in an under-voltage state once the UV voltage rises above 2.5V; and after that an under-voltage occurrence is not recognized until the UV voltage falls below 2.4375V (2.5V – 62.5mV).

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC controllers have been met, the SMH4804 provides a means to soft start the external power FET. It is important to limit in-rush current to prevent damage to the add-in card or disruptions to the host power supply. For example, charging the filter capacitance (normally required at the input of the DC/DC controllers) too quickly may generate very high current. The VGATE output of the SMH4804 is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. The slew rate may be found by dividing I_{VGATE} by the gate-to-drain capacitance placed on the external FET. A complete design example is given in the Applications Section.

Load Control — Sequencing the Secondary Supplies

Once power has been ramped to the DC/DC controllers, two conditions must be met before the PG*n*# outputs can be enabled: the Drain Sense voltage must be below 2.5V, and the VGATE voltage must be greater than $V_{DD} – V_{GT}$. The Drain Sense input helps ensure that the power MOSFET is not absorbing too much steady state power from operating at a high V_{DS}. This sensor remains active at all times (except during the current regulation period). The VGATE sensor makes sure that the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches V_{DD} – V_{GT} this sensor is latched.

When the external MOSFET is properly switched on the PG*n*# outputs may be enabled (if ENPGA, ENPGB, and ENPGC are all high). Output PG1# is activated first, followed by PG2# after a delay of t_{PGD}, PG3# after another t_{PGD} delay, and PG4# after a final t_{PGD} delay. The delays built into the SMH4804 allow timed sequencing of power to the loads. The delay times are programmable from 50µs to 160ms.

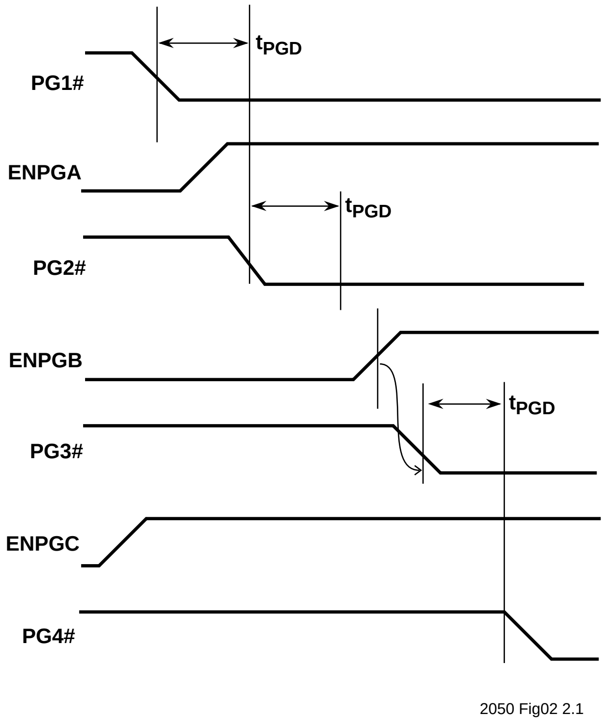


Figure 2. PG Output and ENPG Input Relationship

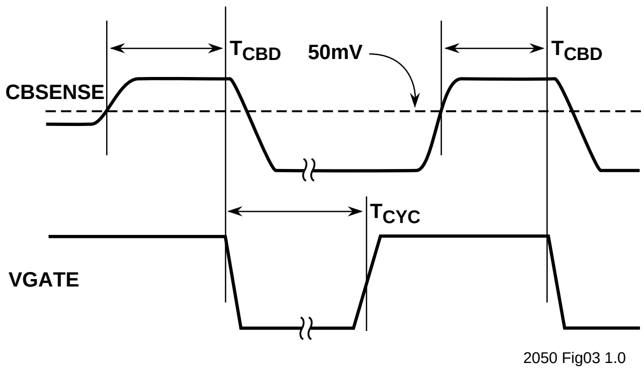


Figure 3. Circuit Breaker Cycle Mode, RESET# High

PG2#, PG3#, and PG4# can be disabled by bringing ENPGA low. Likewise PG#3 and PG4# are disabled when ENPGB is low. Finally, PG4# alone will be shut off if ENPGC is low. This cascaded control is useful for enabling supplies that have dependencies based on the other voltages in the system.

The PG*n*# outputs have a 12V withstand capability, so high voltages must not be connected to these pins. Bipolar transistors or optoisolators can be used to boost the withstand voltage to that of the host supply. See Figure 19 for connections.

Forced Shutdown — Secondary Feedback

The Forced Shutdown signal (FS#) is an active low input that provides a method of receiving feedback from the secondary side of the DC/DC controllers. A built-in holdoff timer allows the SMH4804 to ignore the state of the FS# input until the timer period expires. The FS# input must be driven high by the end of this timer period. A low level on this input will cause a Fault condition, driving FAULT# low and shutting off the VGATE and PG*n*# outputs. Refer to the following section titled "Resetting FAULT#".

The purpose of the holdoff timer is to allow enough time for devices on the secondary side of the DC/DC controllers to power up and stabilize. This unique feature of the SMH4804 allows supervisory circuits such as an SMS44 to control the shutdown of the primary side soft start circuit, even though the secondary side initially has no power.

Alternatively, the FS# input can be programmed to act as a fourth ENPG input controlling the PG1# output. This is combined with an option to independently enable PG1# with no affect on the other PG*n*# outputs, or it can be

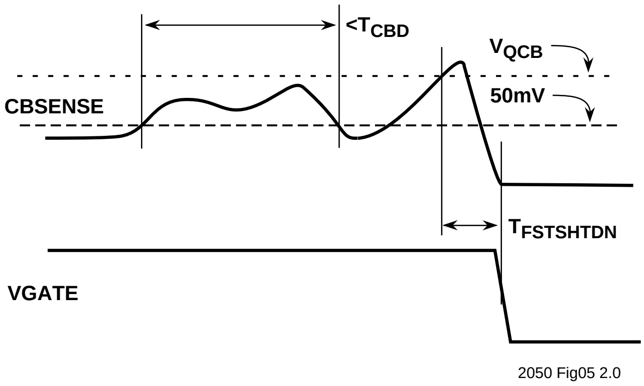


Figure 5. Circuit Breaker Quick Trip Response

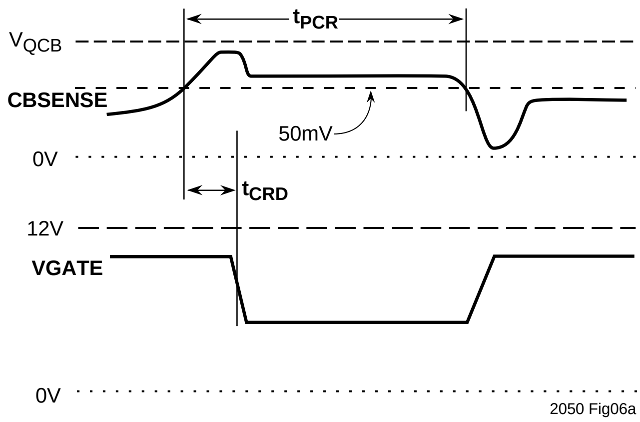


Figure 6.a Current Regulation With Recovery

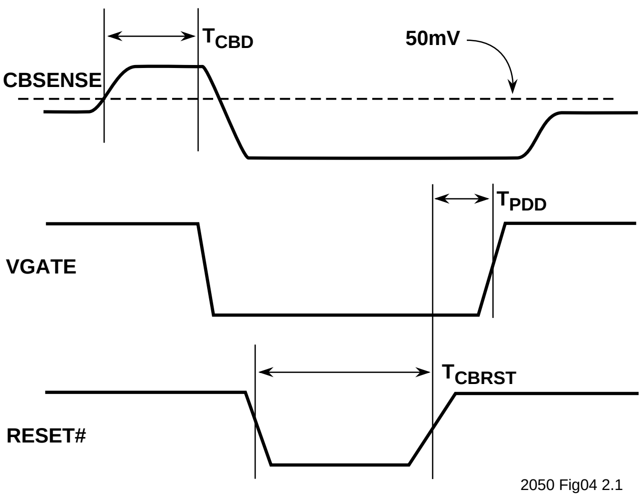


Figure 4. Circuit Breaker Reset Mode

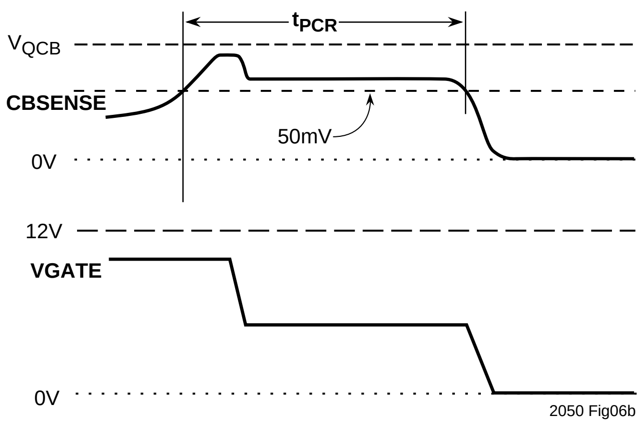


Figure 6.b Current Regulation Without Recovery

programmed so PG1# is the enabling output for the other outputs.

Circuit Breaker Operation

The SMH4804 provides a number of circuit breaker functions to protect against over current conditions. A sustained over-current event could damage the host supply and/or the load circuitry. The board's load current passes through a series resistor (R_S) connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}.

The breaker trips whenever the voltage drop across R_S is greater than 50mV for more than t_{CBD} (a programmable filter delay ranging from 10µs to 500µs).

Quick-Trip™ Circuit Breaker

Additionally, the SMH4804 provides a Quick-Trip feature that will cause the circuit breaker to trip immediately if the voltage drop across R_S exceeds V_{QCB}. The Quick-Trip level may be set to 60mV, 100mV (default), 200mV, or the feature may be disabled.

AC TIMING CHARACTERISTICS

(Over Recommended Operating Conditions)

Reference Figures 1 through 5

Symbol	Description	Min.	Typ.	Max.	Units
t_{CBD}	Programmable 50mV Circuit Breaker delay (filter)		5		µs
			50 *		µs
			150		µs
			400		µs
t_{PGD}	Programmable Power Good delay (PG1/PG2, PG2/PG3, PG3/PG4)		50		µs
			250		µs
			500		µs
			1500		µs
			5 *		ms
			20		ms
			80		ms
			160		ms
$t_{FSTSHTDN}$	Fast shutdown delay from Fault to V_{GATE} off		200		ns
t_{CYC}	Circuit breaker cycle mode cycle time		2.5 *		s
			5		s
t_{CBRST}	CB_{RESET} pulse width	200			ns
t_{PUVF}	Programmable Under-Voltage filter		OFF *		—
			5		ms
			80		ms
			160		ms
t_{PDD}	Programmable Pin Detect		0.5		ms
			5		ms
			80 *		ms
			160		ms

Note: * Denotes default configuration setting

2050 Table01 2.2

Current Regulation

The current regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time. It is generally enabled in applications that have switched dual (A and B) distributed power sources. By using the current regulation function, unwarranted shutdowns can be avoided if one of the dual supplies is switched in when it is at a more negative potential the currently operating supply.

When current regulation is selected it will be enabled during softstart (power on period) and during normal operation after the PG*n*# outputs are enabled. If the voltage monitored at the CBSENSE pin is grate than 50mV, but less than V_{QCB}, the SMH4804 will reduce the VGATE voltage in order to maintain a CBSENSE potential less than 60mV, effectively regulating the current through the MOSFET.

Figures 6a and 6b illustrate the current regulation function. The time period t_{PCR} — selectable at 5, 80, or 320ms — is the maximum time during which regulation will be enforced. If either V_{QCB} or t_{PCR} are exceeded the VGATE and PG*n*# outputs will immediately be de-asserted. However, if CBSENSE drops below 50mV before the timer ends, the timer is reset and VGATE resumes normal operation (see Figure 6A). If the Quick-Trip level is exceeded then the device will bypass the current regulation timer and shut down immediately. The Current Regulation feature is disabled in the default configuration.

Nonvolatile Fault Latch

The SMH4804 also provides an optional nonvolatile fault latch (NVFL) circuit breaker feature. The nonvolatile fault latch essentially provides a programmable fuse on the circuit breaker. When enabled the nonvolatile fault latch will be set whenever the circuit breaker trips. Once set, it cannot be reset by cycling power or through the use of the RESET# pin.

> NOTE: THE DEVICE REMAINS DISABLED UNTIL REGISTER C IS REPROGRAMMED.

As long as the NVFL is set, the FAULT# output will be driven active. The Nonvolatile Fault Latch feature is disabled in the default configuration.

Resetting FAULT#

When the circuit breaker trips the VGATE output is turned off and FAULT# is driven low. There are two methods to reset the circuit breaker which are selectable with the MODE pin. When MODE is held high or left floating the circuit breaker is in the duty-cycle mode, and the breaker resets automatically after a time of t_{CYC}. When the MODE pin is held low (or disabled in the Configuration Register) FAULT# can be reset by bringing RESET# low. The VGATE output will attempt to restart the MOSFET slew control circuitry t_{PDD} after bringing RESET# back high again. In either case, cycling power to the board will also reset the circuit breaker. If the over current condition still exists after the MOSFET switches back on the circuit breaker will re-trip.

Access to the Registers

The SMH4804 2-wire bus interface is highly configurable while maintaining the industry standard protocol. The SMH4804 will respond to one of two selectable Device Type Addresses: 1010_{BIN}, generally assigned to NV-memories, or 1011_{BIN}, which is the default address for the SMH4804.

Register access is also programmable: access can be denied (no reads or writes); access can be read only; or access for both reads and writes can be enabled, which is the default state.

The SMH4804 has three address pins associated with the 2-wire bus. The part can be configured to respond only to the proper serial data string of Device Type Address and Bus Address, or, alternatively, it can be programmed to respond to the Device Type Address and any Bus Address.

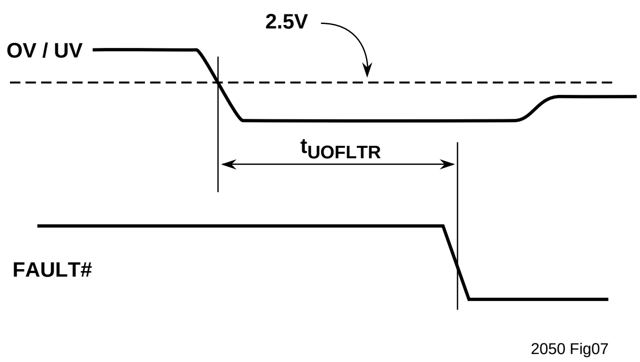


Figure 7. Under-/Over-Voltage Filter Timing

PROGRAMMING THE SMH4804

PROGRAMMING CONNECTION

The end user can use the summit SMX3200 programming cable and software that have been developed to operate with a standard personal computer. See Figure 8 for board connections. The programming cable interfaces directly between a PC's parallel port and the target application. The application's values are entered via an intuitive graphical user interface employing drop-down menus.

> *Caution: Damage may occur when connecting the dongle to a system utilizing an earth-connected positive terminal.*

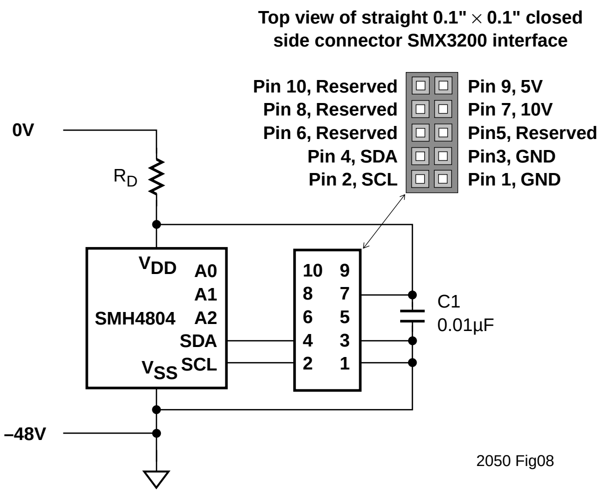


Figure 8. Programming Connection

After the desired settings for the application are determined the software will generate a hex file that can be transferred to the target device or downloaded to Summit. If it is downloaded to Summit a customer part number will be assigned and the file will be used to customize the devices during the final electrical test operations.

The following detailed information is supplied for those wanting to develop their own programming algorithms.

USER CONFIGURATION REGISTERS

The SMH4804 has eight user programmable, nonvolatile, configuration registers. Each can be written or read using the 2-wire serial interface, comprised of SDA (bidirectional data line) and SCL (Serial Clock input). Reading and writing the registers follows the industry standard protocol.

Input Data Protocol

The protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. The SMH4804 is always a Slave device, since it never initiates any data transfers. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because a change on the data line while SCL is high is interpreted as either a Start or a Stop condition.

START and STOP Conditions

When both the data and clock lines are high, the bus is said to be not busy. When the clock is high a high-to-low transition on the data line is defined as the Start condition. When the clock is high a low-to-high transition on the data line is defined as the Stop condition.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the Master or the Slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to Acknowledge that it received the eight bits of data. The SMH4804 will respond with an Acknowledge after recognition of a Start condition and its Slave address byte. If both the device and a Write operation are selected, the SMH4804 will respond with an Acknowledge after the receipt of each subsequent 8-Bit word. In the Read mode the SMH4804 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal (the line is pulled low). If an Acknowledge is detected, and there is no STOP condition generated by the master, the SMH4804 will continue to transmit data. If a NACK (the line is pulled high) is detected the SMH4804 will terminate further data transmissions and await a Stop condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the Slave it is accessing. The most significant four bits of the slave address are the device type identifier.

Device Identifier				Bus Address			R / W
1	0	1	1	A2	A1	A0	1 / 0
1	0	1	0	A2	A1	A0	1 / 0

2050 Table02 1.0

Table 2. Address Byte

For the SMH4804 this is either 1010_{BIN} or 1011_{BIN}, depending upon the state of the Slave Address Bit in Register 8. The next three bits must match the address setting for signals A2, A1, and A0.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to 1 a Read operation is selected; when set to 0 a Write operation is selected.

WRITE OPERATIONS

Only one register can be read or written per sequence (*i.e.*, no page Write or sequential register Reads).

Write

After the device address is transmitted and an Acknowledge has been received the Master transmits the register address. The four MSBs are don't care and the register address is contained in the four LSBs. Upon receipt of the register address the SMH4804 responds with an Acknowledge. The next byte to be transmitted is the configuration information. The four MSBs are don't care and the configuration information is contained in the four LSBs. The Master then terminates the transfer by generating a Stop condition, at which time the SMH4804 begins the internal write cycle. While the internal write cycle is in process the SMH4804 inputs (SDA and SCL) are disabled, and the device will not respond to any requests from the Master.

READ OPERATIONS

Register Read operations allow the Master to read current contents of individual registers. This operation involves a two step process. First, the Master issues a Write command that includes the Start condition and the device address field (with the R/W bit set to 0) followed by the register address. This procedure sets the internal address counter of the SMH4804 to the desired address. After the word address acknowledge is received by the Master it immediately reissues a Start condition followed by another device address field with the R/W bit set to 1. The SMH4804 will respond with an Acknowledge and then transmit the data byte stored at the addressed location. At this point the Master sets a NACK and generates the Stop condition.

REGISTER BIT MAPS

The SMH4804 has eight user programmable, nonvolatile, configuration registers. Although 8-Bit data transfers are used for reading and writing the registers, only the 4 LSBs are utilized by the device.

Register 2

This register is used to select both the over-current delay and the quick trip threshold for the electronic circuit breaker.

MSB	Bits						LSB
x	x	x	x	3	2	1	0
Over-current delay: 400µs				0	0	x	x
Over-current delay: 150µs				0	1		
Over-current delay: 50µs				1 *	0 *		
Over-current delay: 5µs				1	1		
Quick Trip Ref.: 200mV				x	x	0	0
Quick Trip Ref.: 100mV						0 *	1 *
Quick Trip Ref.: 60mV						1	0
Quick Trip Ref.: OFF						1	1

2050 Table03 2.0

Note: * Denotes default configuration setting

Table 3. Register 2, Address 0010

MSB Bits				LSB
Precondition: R9 Bit 3 = 0	3	2	1	0
PG Sequencing Delay: 1500µs	0	0	x	x
PG Sequencing Delay: 50µs	0	1		
PG Sequencing Delay: 250µs	1	0		
PG Sequencing Delay: 500µs	1	1		
Precondition: R9 Bit 3 = 1	–	–		
PG Sequencing Delay: 5ms	0 *	0 *		
PG Sequencing Delay: 20ms	0	1		
PG Sequencing Delay: 80ms	1	0		
PG Sequencing Delay: 160ms	1	1		
Mode Signal In Disabled	x	x	0	x
Mode Signal In Enabled			1 *	
PD1# and PD2# Disabled			x	0
PD1# and PD2# Enabled				1 *

2050 Table04 2.1

Note: * Denotes default configuration setting

Table 4. Register 3, Address 0011

Register 3

This register controls multiple functions. Bits 3 and 2 work in conjunction with bit 3 in register 9, (it is imperative register 9 is programmed properly) and they control the sequencing delays from PG1# to PG2#, PG2# to PG3#, and PG3# to PG4#. These two bits are effectively concatenated with R9 bit 3, providing 8 programmable delay periods.

Bit 1 controls the effect of the MODE pin. When set to 1 the pin functions as described in the pin descriptions. If the bit is set to 0 the state of the pin will be ignored and the circuit breaker will be in the latch mode.

Bit 0 enables or disables the function of the PDx# inputs.

Register 4

This register bit 3 enables or disables the PG*n*# sequence delays. When set to a 1 the delays will be as defined in registers 3 and 9. If it is set to 0 no delay will be incurred, but sequencing based solely on the state of the ENPG*n*# inputs will be supported. If the ENPG*n*# inputs are tied high, the PG*n*# outputs will turn on simultaneously.

The next two bits select the OV/UV filter value, and bit 0 selects either 2.5s or 5s CB cycle times.

Register 5

This register bit 3 controls the function of the nonvolatile fault latch.

Bits 2, 1 and 0 configure the FS# input. FS# has two basic functions: it can be programmed to act as an auxiliary Enable Input controlling the PG1# output, or it can be programmed to be an event monitor during the power-up sequence.

These bits also control the interrelationship of the PG*n*# outputs. In a cascade operating mode PG1# must be true before PG2# can be true, *etc*. This interrelationship can be disabled so that each PG*n*# output is effectively controlled by its corresponding ENPG*n*# input, so long as the primary supply, VGATE, and DRAIN SENSE are within their operating limits.

When programmed as an enable to PG1# there are two options: 010_{BIN} disables the cascade mode (the PG*n*# outputs can act independently) and FS# effectively becomes the enable input for PG1#; 011_{BIN} enables the cascade mode and makes FS# the enable input for PG1#. In this mode, PG1# must be active before PG2# can be activated, followed by PG3#, then PG4#.

The event monitor mode will generally be implemented in conjunction with a monitoring device on the secondary side of the DC/DC converters, such as the SMS44. If FS# is not pulled high before the programmed condition then the PG*n*# outputs and VGATE will be shut down. As an example, if the binary value is 111_{BIN}, VGATE and PG1# will be shut down if FS# is not pulled high before t_{PGD} has elapsed after PG1# is true. None of the other PG*n*# outputs will be activated. If a failure occurs due to the lapse of the event monitor timer, cycling the power will reset the device.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PG Sequencing: Disabled</td><td>0</td><td rowspan="2">x</td><td rowspan="2">x</td><td rowspan="6">x</td></tr>
<tr><td colspan="4">PG Sequencing: Enabled</td><td>1 *</td></tr>
<tr><td colspan="4">Over-/Under-Voltage Filter: OFF</td><td rowspan="6">x</td><td>0 *</td><td>0 *</td></tr>
<tr><td colspan="4">OV/UV Filter: 5ms</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">OV/UV Filter: 80ms</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">OV/UV Filter: 160ms</td><td>1</td><td>1</td></tr>
<tr><td colspan="4">Circuit Breaker Cycle: 2.5s</td><td rowspan="2">x</td><td rowspan="2">x</td><td>0 *</td></tr>
<tr><td colspan="4">Circuit Breaker Cycle: 5s</td><td>1</td></tr>
</table>

2050 Table05 2.0

Note: * Denotes default configuration setting

Table 5. Register 4, Address 0100

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Non-volatile Fault Latch: Enabled</td><td>0</td><td rowspan="2">x</td><td rowspan="2">x</td><td rowspan="2">x</td></tr>
<tr><td colspan="4">Non-volatile Fault Latch: Disabled</td><td>1 *</td></tr>
<tr><td colspan="4">FS Function: PG4 + t_{PGD} Cascade disabled for simultaneous</td><td rowspan="8">x</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">FS Function: Disabled (=1)</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">FS Function: Active (=1) before PG1 enabled Cascade disabled for simultaneous</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">FS Function: Active before (=1) PG1 Enabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td colspan="4">FS Function: PG4 + t_{PGD}</td><td>1 *</td><td>0 *</td><td>0 *</td></tr>
<tr><td colspan="4">FS Function: PG3 + t_{PGD}</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">FS Function: PG2 + t_{PGD}</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">FS Function: PG1 + t_{PGD}</td><td>1</td><td>1</td><td>1</td></tr>
</table>

2050 Table06 2.0

Note: * Denotes default configuration setting

Table 6. Register 5, Address 0101

One last event mode, 000_{BIN}, disables the cascade effect and sets up PG4# going true as the trigger event. FS# must be pulled high before t_{PGD} elapses, or VGATE and all the PG*n*# outputs will be disabled.

Cascade enabled:
ENPGA enables PG2#, PG3# and PG4#;
ENPGB enables PG3# and PG4#;
ENPGC enables PG4#.

Cascade disabled:
ENPGA enables PG2#;
ENPGB enables PG3#;
ENPGC enables PG4#.

Simultaneous:
PG1#, PG2#, PG3# and PG4# operate independently from one another.

Sequenced:
PG1#, PG2#, PG3# and PG4# are dependent upon activation of PG(N–1) — for N = 2, 3, and 4 — plus a programmable PG delay.

Register 6

This register enables what events are recorded in the nonvolatile fault latch if bit 3 of R5 is set to 0. The two low order bits program the current regulation time period.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Under-Voltage Filtered enabled</td><td>0</td><td rowspan="2">x</td><td rowspan="4">x</td><td rowspan="4">x</td></tr>
<tr><td colspan="4">Under-Voltage Filtered disabled</td><td>1 *</td></tr>
<tr><td colspan="4">Over-Voltage Filtered enabled</td><td rowspan="2">x</td><td>0</td></tr>
<tr><td colspan="4">Over-Voltage Filtered disabled</td><td>1 *</td></tr>
<tr><td colspan="4">Current Regulation: OFF</td><td rowspan="4">x</td><td rowspan="4">x</td><td>0 *</td><td>0 *</td></tr>
<tr><td colspan="4">Current Regulation: 5ms</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">Current Regulation: 80ms</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Current Regulation: 320ms</td><td>1</td><td>1</td></tr>
</table>

2050 Table07

Note: * Denotes default configuration setting

Table 7. Register 6, Address 0110

Register 7

This register controls the UV hysteresis. The values shown are with respect to V_{SS}.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Always set to one</td><td>1 *</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.0V</td><td rowspan="8">1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.063V</td><td>0 *</td><td>0 *</td><td>1 *</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.125V</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.188V</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.250V</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.313V</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.375V</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">UV Hysteresis = 0.438V</td><td>1</td><td>1</td><td>1</td></tr>
</table>

2050 Table08 2.0

Note: * Denotes default configuration setting

Table 8. Register 7, Address 0111

Register 8

This register is used to control the 2-wire bus interface activity. Bit 3 determines the Device Type Address, bits 2 and 1 select the register access capability, and bit 0 determines whether the device must receive a bus address that corresponds to the biasing of the address pins.

Note: If the latch fault option is selected and write access is denied the SMH4804 cannot be cleared of a fault condition.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Device Type Address: 1011</td><td>0 *</td><td rowspan="2">x</td><td rowspan="2">x</td><td rowspan="6">x</td></tr>
<tr><td colspan="4">Device Type Address: 1010</td><td>1</td></tr>
<tr><td colspan="4">Config. Reg. Access: Read & Write</td><td rowspan="6">x</td><td>0 *</td><td>0 *</td></tr>
<tr><td colspan="4">Config. Reg. Access: Read only</td><td>0</td><td>1</td></tr>
<tr><td colspan="4" rowspan="2">Config. Reg. Access: Disabled</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td colspan="4">Slave Address: Responds to all</td><td rowspan="2">x</td><td rowspan="2">x</td><td>0</td></tr>
<tr><td colspan="4">Slave Address: Response limited</td><td>1 *</td></tr>
</table>

2050 Table09

Note: * Denotes default configuration setting

Table 9. Register 8, Address 1000

Register 9

This register bit 3 works in conjunction with Register 3. Refer to the Register 3 description for details. Bit 2 is always programmed to 0. Bits 1 and 0 select the delay from the point where both PDx inputs are low (or initial power up conditions) to when sequencing can commence.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">Power Good sequence fast</td><td>0</td><td rowspan="7">0 *</td><td rowspan="3">x</td><td rowspan="3">x</td></tr>
<tr><td colspan="4">Power Good sequence slow</td><td>1 *</td></tr>
<tr><td colspan="4">Default: bit 2 always 0</td><td rowspan="5">x</td></tr>
<tr><td colspan="4">PD Delay: 0.5ms</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">PD Delay: 80ms</td><td>0 *</td><td>1 *</td></tr>
<tr><td colspan="4">PD Delay: 160ms</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">PD Delay: 320ms</td><td>1</td><td>1</td></tr>
</table>

2050 Table10

Note: * Denotes default configuration setting

Table 10. Register 9, Address 1001

Register C

The last register is not a configuration register, it is the nonvolatile fault latch. If a circuit breaker fault condition is detected, and the NV Fault latch is enabled (Register 5, Bit 3), bit 0 will automatically be written to a '1'. So long as it remains a '1' the SMH4804 will not be able to drive VGATE or the PG*n*# outputs. The host or service center must access the register and write a '0' to bit 0 to clear the fault.

<table>
<tr><th>MSB</th><th colspan="6">Bits</th><th>LSB</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">NV Fault Latch: Reset</td><td rowspan="2">x</td><td rowspan="2">x</td><td rowspan="2">x</td><td>0 *</td></tr>
<tr><td colspan="4">NV Fault Latch: Set</td><td>1</td></tr>
</table>

2050 Table11 1.0

Note: * Denotes default configuration setting

Table 11. Register C, Address 1100

BUS INTERFACE

GENERAL DESCRIPTION

The I^2C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial Data line (SDA) and a serial Clock line (SCL). All Summit Microelectronics parts support a 100kHz clock rate, and some support the alternative 400kHz clock. Check the AC Electrical Table for the value of f_{SCL}. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. Summit parts have a Schmitt input on both lines. See Figure 9 and Table 12 for waveforms and timing on the bus. One bit of Data is transferred during each Clock pulse. The Data must remain stable when the Clock is high.

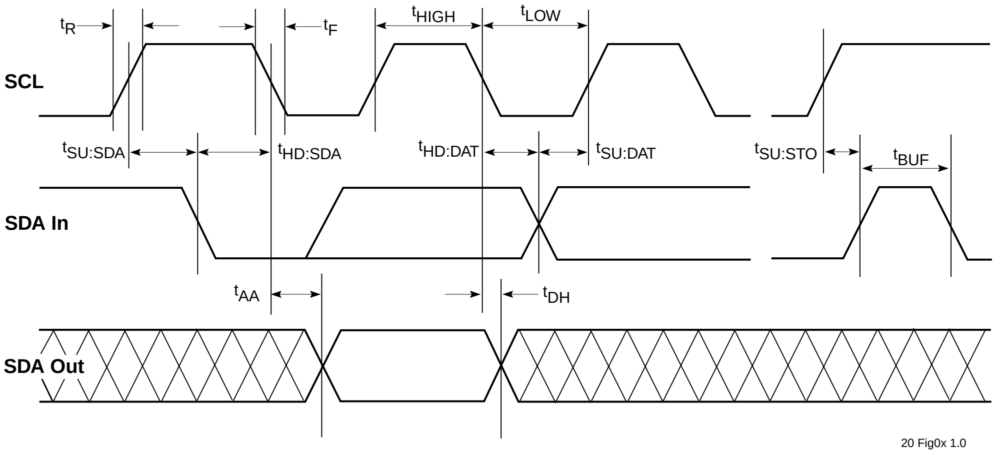


Figure 9. Memory Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time (1)	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time (1)		250		ns
$t_{HD:DAT}$	Data In hold time (1)		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

Note (1) These values are guaranteed by design.

2044 Table12

Table 12. Register Read/Write AC Operating Characteristics

Start and Stop Conditions

Both Data and Clock lines remain high when the bus is not busy. Data transfer between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the Data line while the Clock line is high is defined as a Start condition. A low-to-high transition of the Data line while the Clock line is high is defined as a Stop condition. See Figure 10.

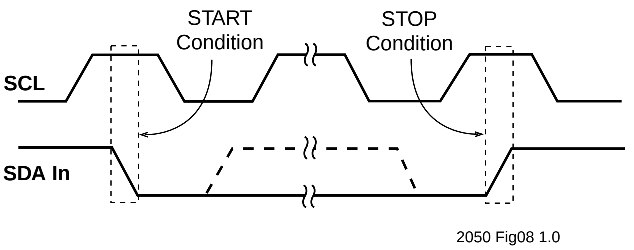


Figure 10. Start and Stop Conditions

Protocol

The protocol defines any device that sends data onto the bus as a Transmitter, and any device that receives data as a Receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the Summit Microelectronic devices are Slave devices, since they never initiate any data transfers.

Acknowledge

Data is always transferred in 8-Bit bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The Transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the Receiver will pull the SDA line low to Acknowledge that it received the eight bits of data (See Figure 11).

In the case of a Read from a Summit part, when the last byte has been transferred to the Master, the Master will leave the Data line high for a NACK. This will cause the Summit part to stop sending data, and the Master will issue a Stop on the clock pulse following the NACK.

In the case of a Write to a Summit part the Master will send a Stop on the clock pulse after the last Acknowledge. This will indicate to the Summit part that it should begin its internal nonvolatile write cycle.

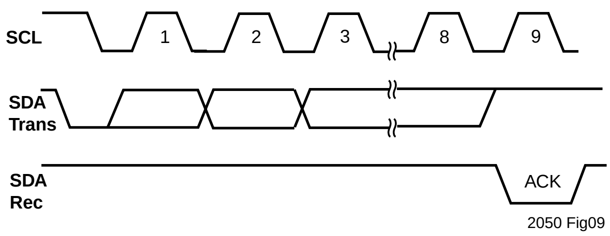


Figure 11. Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a seven bit Slave address and the Read/Write bit. The R/W bit tells the Slave whether the Master is reading Data from the bus or writing Data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SMH4804 is 1010_{BIN}. The next three bits are Address values for A2, A1, & A0 if multiple devices are used. See Figure 12. The SMH4804 will issue an Acknowledge after recognizing a Start condition and its DTI.

In the Read mode the SMH4804 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4804 will continue to transmit data. If an Acknowledge is not detected (NACK), the SMH4804 will terminate further data transmission. See Figure 13.

In the Write mode the SMH4804 receives eight bits of data, then generates an Acknowledge signal. It will continue to generate ACKs until a Stop condition is generated by the Master. See Figure 14.

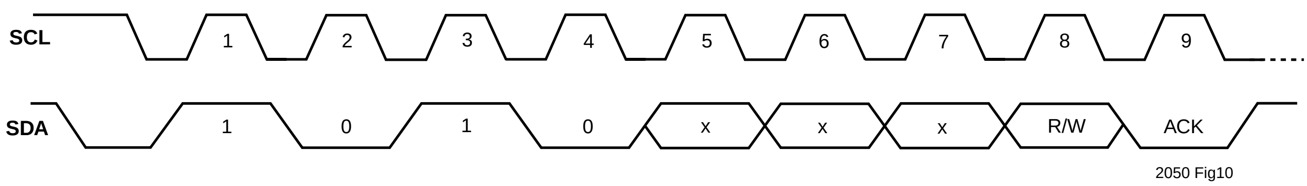


Figure 12. Typical Master Address Byte Transmission

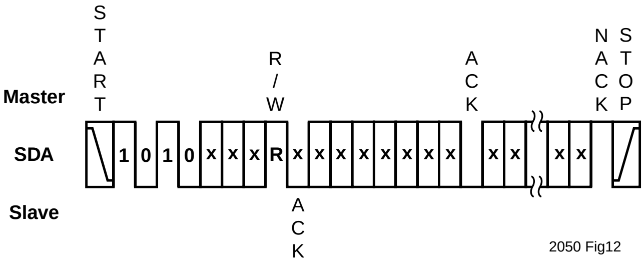


Figure 13. Read

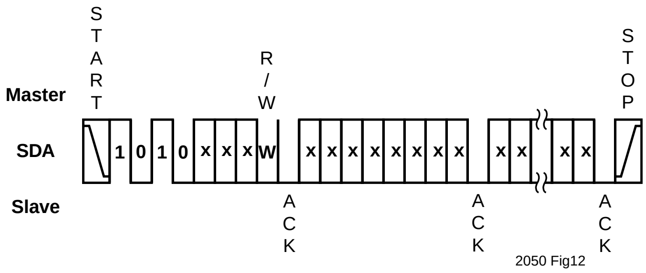


Figure 14. Write

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4804 to the desired address. After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4804 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SMH4804 discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential Reads can be initiated as either a current address Read or a random access Read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4804. The SMH4804 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will roll over and the memory will continue to output data.

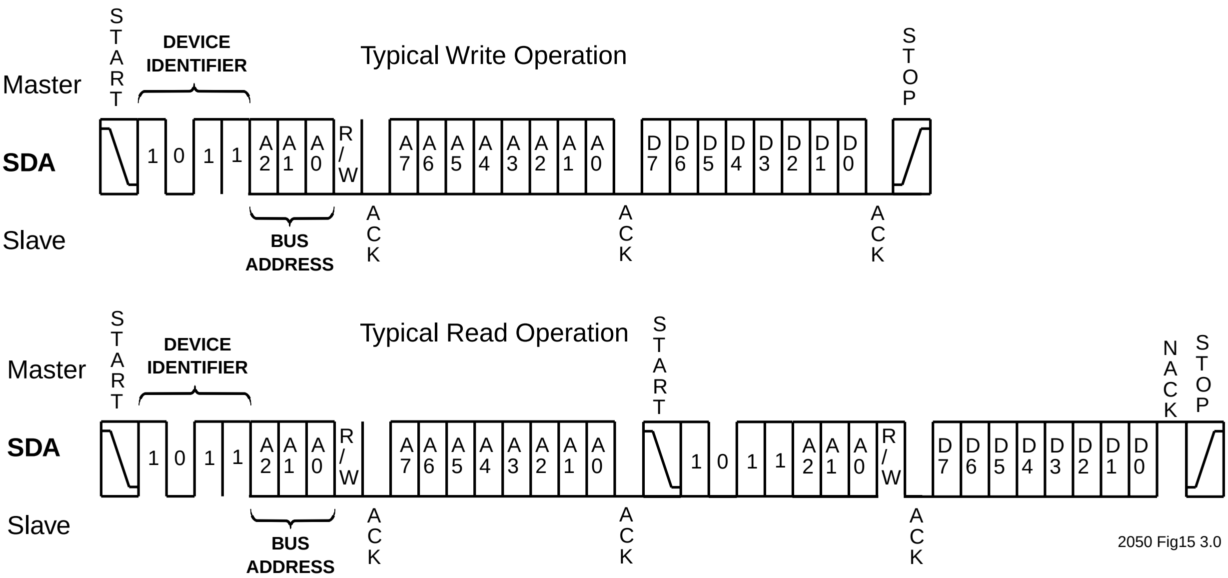


Figure 15. Serial Bus Activity

APPLICATIONS

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4804 hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

Over-Voltage and Under-Voltage Resistors

In the following examples, the three resistors, R1, R2, and R3, connected to the OV and UV inputs, must be capable of withstanding the maximum supply voltage of several hundred volts. The trip voltage of the UV and OV inputs is 2.5V relative to V_{SS}. As the input impedance of UV and OV is very high, large value resistors can be used in the resistive divider. The divider resistors should be high stability, 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (*i.e.*, the 48V supply can vary from 36V to 72V). The formulae for calculating R1, R2, and R3 follow.

First a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it can't be too high (self-heating in R3 will become a problem), or too low (the value of R3 becomes very large, and leakage currents can reduce the accuracy of the OV and UV trip points). The value of ID_{MAX} should be ≥200µA for the best accuracy at the OV and UV trip points. A value of 250µA for ID_{MAX} will be used to illustrate the following calculations.

With V_{OV} (2.5V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}.$$

Substituting:

$$R1 = \frac{2.5V}{250\mu A} = 10k\Omega.$$

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}.$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{72V} = 125\mu A.$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} - V_{UV}}{ID_{MIN}}.$$

V_{UV} is the under-voltage trip point, also 2.5V. Substituting:

$$R3 = \frac{36V - 2.5V}{125\mu A} = 268k\Omega.$$

The closest standard 1% resistor value is 267kΩ

Then R2 is calculated:

$$(R1 + R2) = \frac{V_{UV}}{ID_{MIN}},$$

or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1.$$

Substituting:

$$R2 = \frac{2.5V}{125\mu A} - 10k\Omega = 20k\Omega - 10k\Omega = 10k\Omega.$$

An Excel spread sheet is available on Summit's website (***www.summitmicro.com***) to simplify the resistor value calculations and tolerance analysis for R1, R2, and R3.

Dropper Resistor Selection

The SMH4804 is powered from the high-voltage supply via a dropper resistor, R_D. The dropper resistor must provide the SMH4804 (and its loads) with sufficient operating current under minimum supply voltage conditions, but must not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - V_{DD_{MAX}}}{I_{DD} + I_{LOAD}},$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4804 supply voltage, I_{DD} is minimum current required for the SMH4804 to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

Calculate the minimum wattage required for R_D from:

$$P_{R_D} \geq \frac{\left(VS_{MAX} - V_{DD_{MIN}}\right)^2}{R_D},$$

where V_{DDMIN} is the lower limit of the SMH4804 supply voltage, and VS_{MAX} is the highest operating supply voltage.

In circumstances where the input voltage may swing over a wide range (*e.g.*, from 20V to 100V) the maximum current may be exceeded. In these circumstances it may be necessary to add an 11V zener diode between V_{DD} and V_{SS} to handle the wide current range. The zener voltage should be below the nominal regulation voltage of the SMH4803A so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4804 monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor, R_T, in series with the drain sense protection diode. This protection, or blocking, diode prevents high voltage breakdown of the drain sense input when the MOSFET switch is OFF. A low leakage MMBD1401 diode offers protection up to 100V. For high voltage applications (up to 500V) the Central Semiconductor CMR1F-10M diode should be used. The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} \times R_T) - V_{DIODE},$$

where V_{DIODE} is the forward voltage drop of the protection diode. The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of V_{DIODE} and I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 68kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 68k\Omega) - 0.5V = 1V.$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D(R_S + R_{ON}),$$

where I_D is the MOSFET drain current, R_S is the circuit breaker sense resistor and R_{ON} is the MOSFET on resistance.

The dropper resistor value should be chosen such that the minimum and maximum I_{DD} and V_{DD} specifications of the SMH4804 are maintained across the host supply's valid operating voltage range. First, subtract the minimum V_{DD} of the SMH4804 from the low end of the voltage, and divide by the minimum I_{DD} value. Using this value of resistance as R_D find the operating current that would result from running at the high end of the supply voltage to verify that the resulting current is less than the maximum I_{DD} current allowed. If some range of supply voltage is chosen that would cause the maximum I_{DD} specification to be violated, then an external zener diode with a breakdown voltage of ≈12V should be used across V_{DD}.

As an example of choosing the proper R_D value, assume the host supply voltage will range from 36 to 72V. The largest dropper resistor that can be used is: (36V-11V)/3mA = 8.3kΩ. Next, confirm that this value of R_D also works at the high end: (72V-13V)/8.3kΩ = 7.08mA, which is less than 10mA.

The FS# input can also be used in conjunction with a secondary-side supervisory circuit providing a positive feedback loop during the power up sequence. As an example, assume the SMH4804 is configured to turn on –48V to three DC/DC converters and then sequentially turn on the converters with a 1.6ms delay. Further assume all of the enable inputs are true and PG4# has just been sequenced on. If FS# option 4 (100_{BIN} in register 5) has been selected, then FS# must be driven high within 1.6ms after PG4# goes low, otherwise all of the PG outputs will be disabled. Ideally, there would be a secondary-side supervisor similar to the SMS44 that would have its reset time-out period programmed to be less than 1.6ms. After the last supply turns on the RESET# output of the SMS44 would be released and FS# pulled high. However, if for any reason not all of the supplies turn on, the RESET# will not be released and the SMH4804 will disable the PG outputs. This termination timer function can be programmed to abort the sequence after PG1#, PG2#, PG3# or PG4#.

Soft Start Slew Rate Control

The –48V turn on time is controlled by the SMH4804 and by the values of R4, C1 and C2. The turn on time is approximately 10ms with the component values shown in Figure 16. Increasing the capacitance reduces the output slew rate and increases the turn on time. The capacitors prevent the MOSFET from turning on simultaneously with the application of –48V. Resistor R4 is specified to limit the current into and the rate of charge of C1. The ratio of C1 to C2 (10:1) limits the MOSFETs VGS to approximately 5V once the –48V supply is connected and C1 is fully charged.

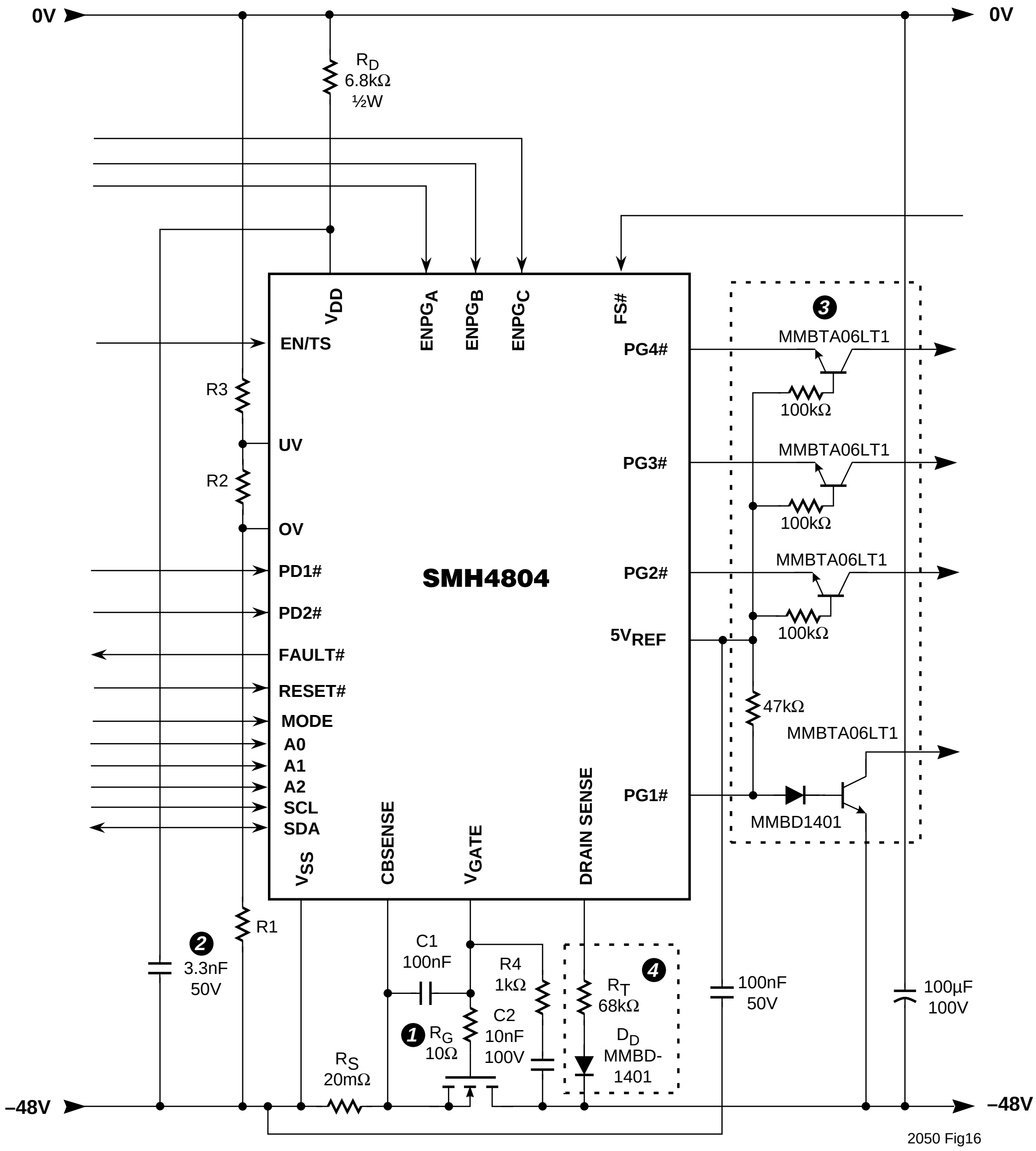


Figure 16. Changing Polarity of Power Good Output PG1#

Notes: ❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V zener must be connected in parallel.

❸ Optional interface circuit. The PG*n*# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG*n*# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

A. Disable the function by connecting the DRAIN Sense pin to V_{SS} directly. The components R_T and D_D are eliminated.

B. Add a capacitor from DRAIN Sense to V_{SS}. The exact capacitance value depends upon the magnitude and duration of the voltage transient appearing at the drain of the MOSFET.

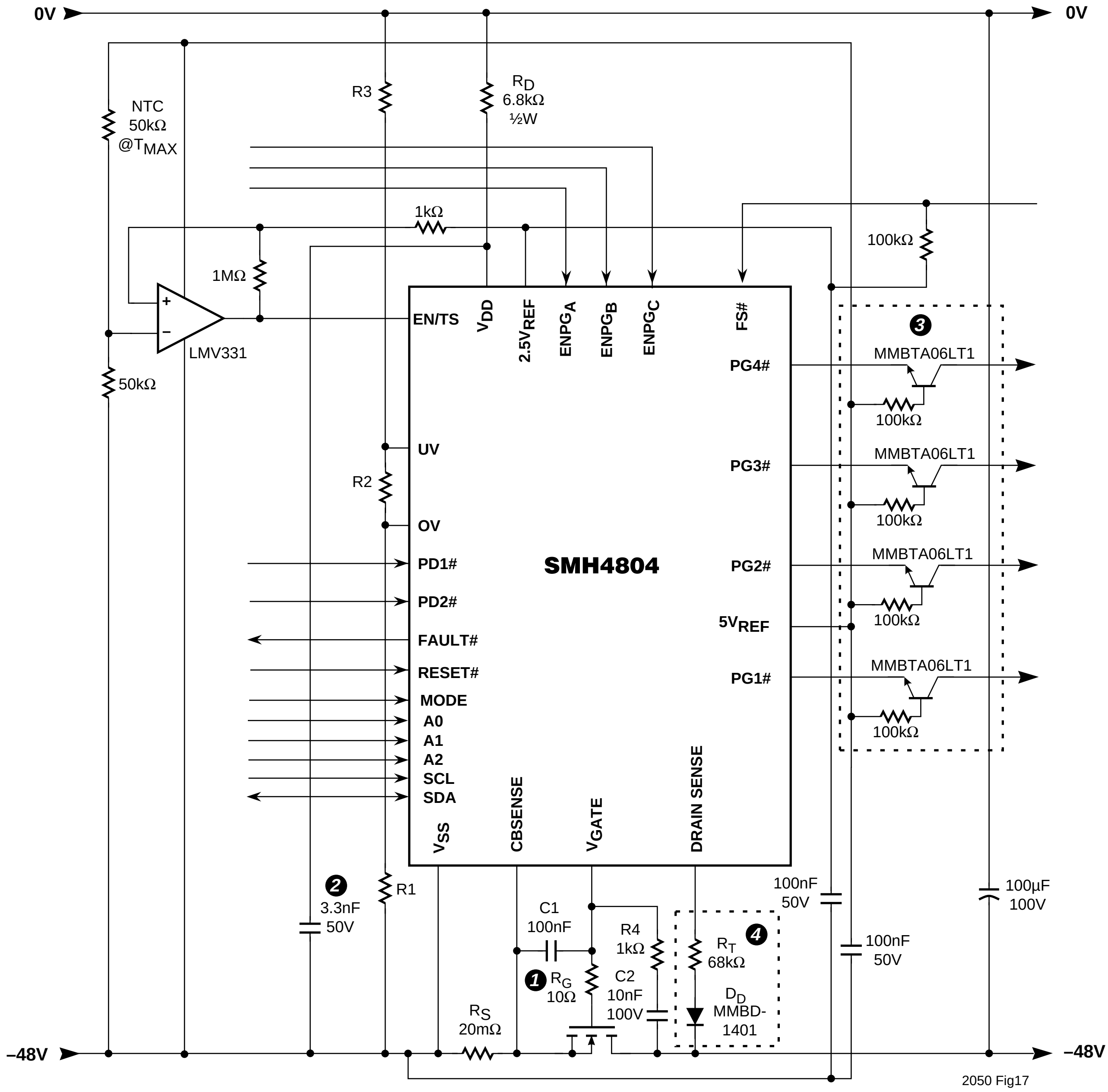


Figure 17. Overtemperature Shutdown

Notes: ❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V zener must be connected in parallel.

❸ Optional interface circuit. The PG*n*# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG*n*# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

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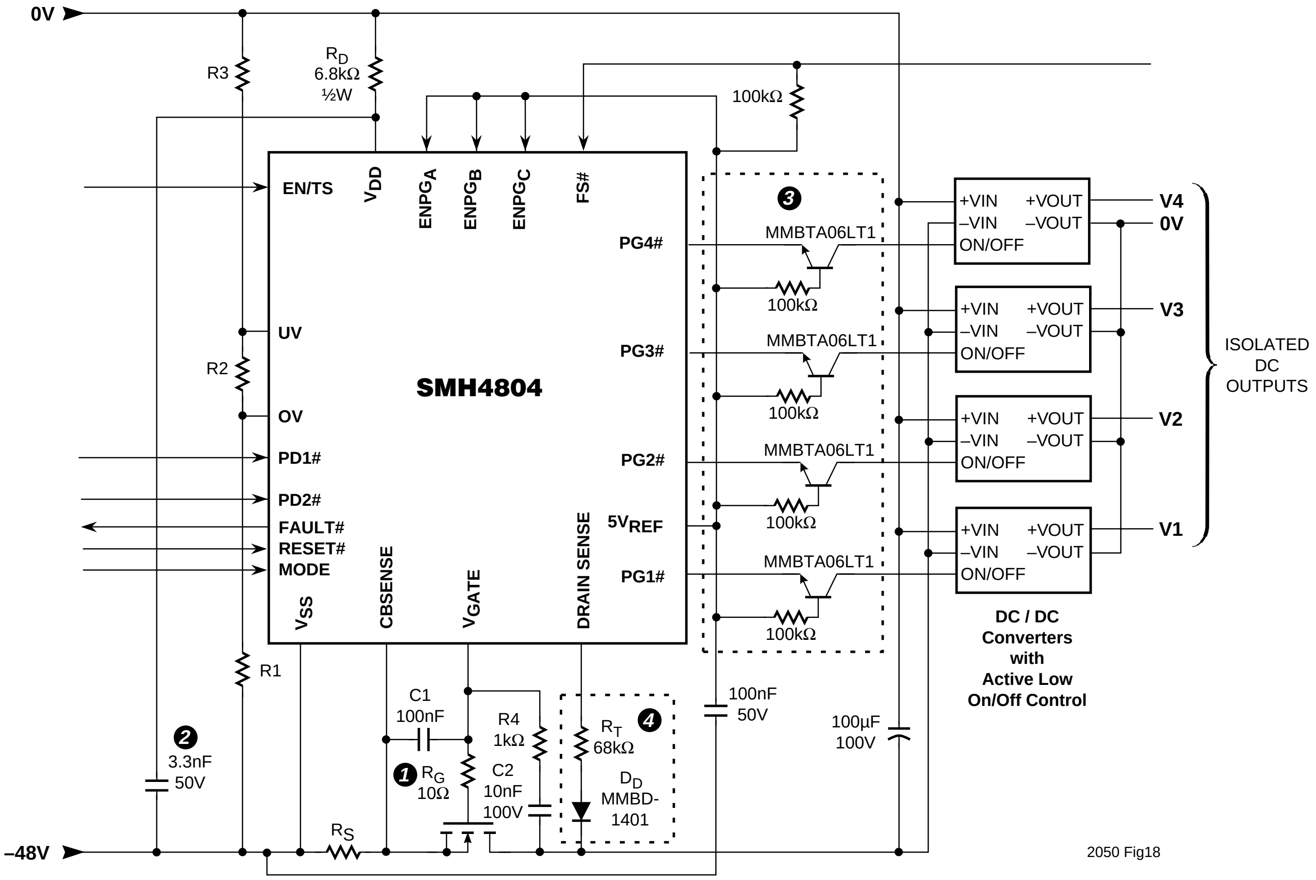


Figure 18. Typical Application Sequencing Four DC/DC Converters

Notes: ❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V zener must be connected in parallel.

❸ Optional interface circuit. The PG*n*# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG*n*# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

A. Disable the function by connecting the DRAIN Sense pin to V_{SS} directly. The components R_T and D_D are eliminated.

B. Add a capacitor from DRAIN Sense to V_{SS}. The exact capacitance value depends upon the magnitude and duration of the voltage transient appearing at the drain of the MOSFET.

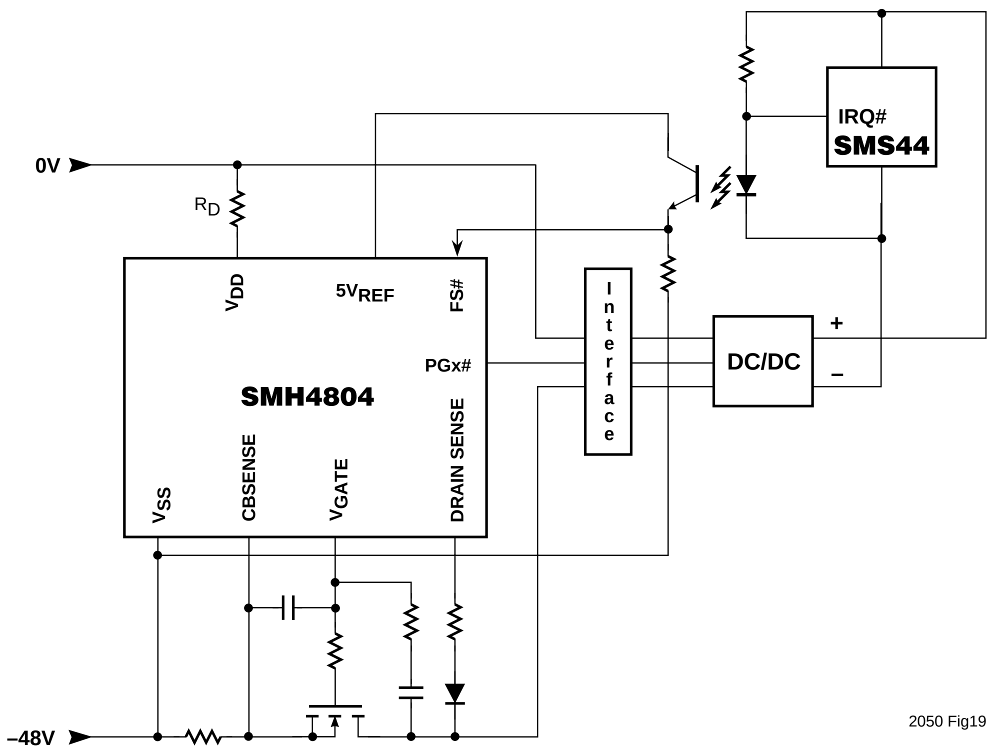


Figure 19. Controlling FS# with Secondary Feedback

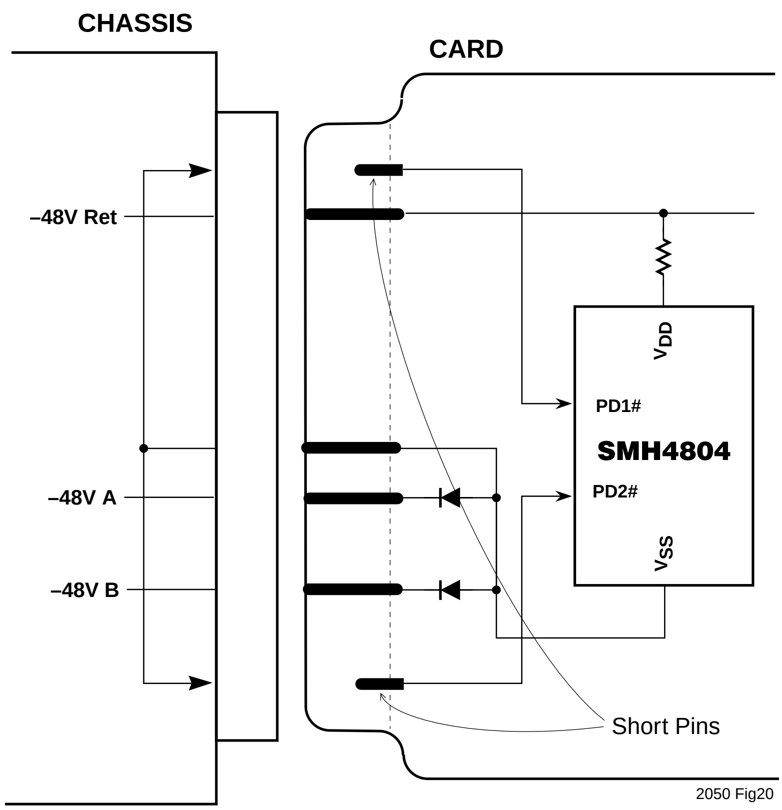
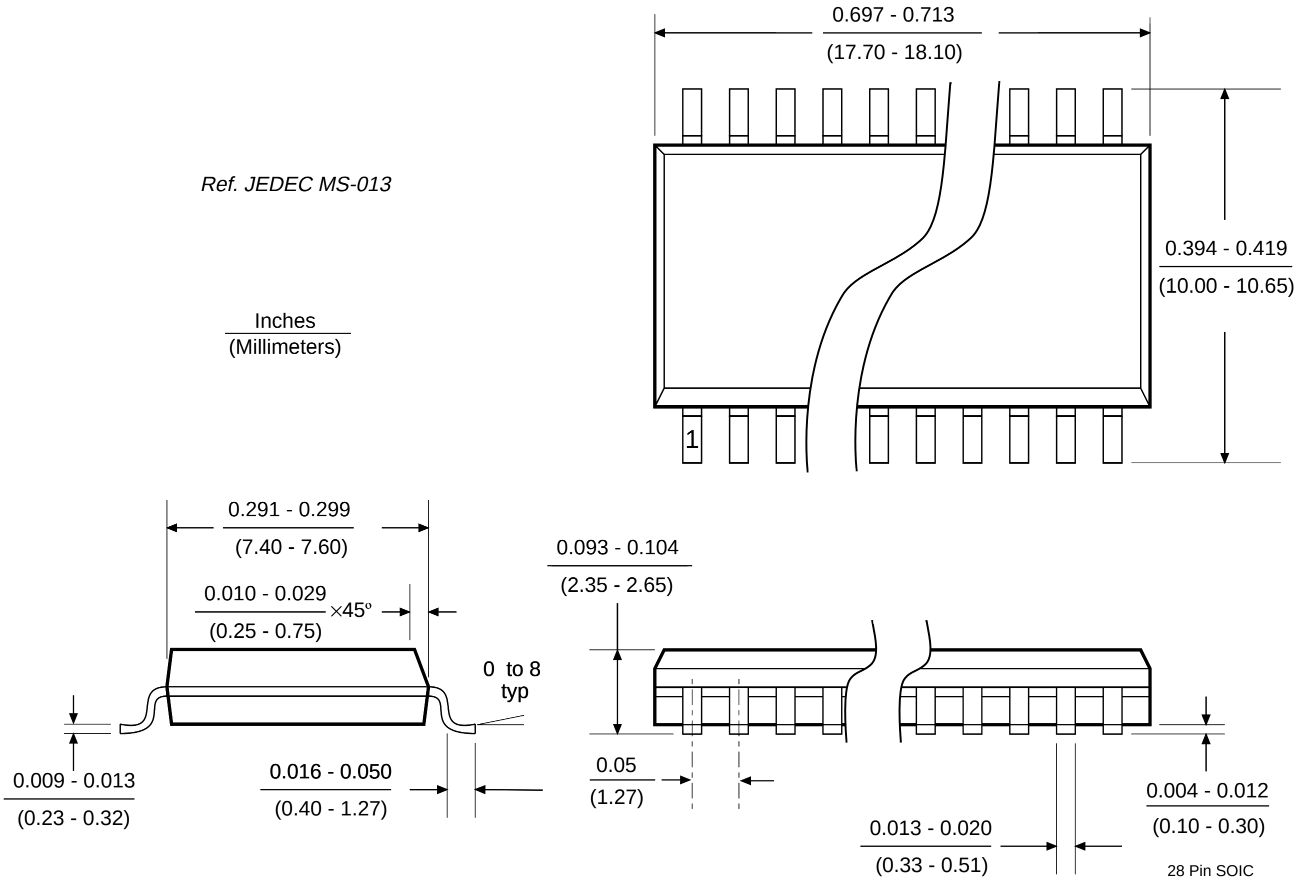


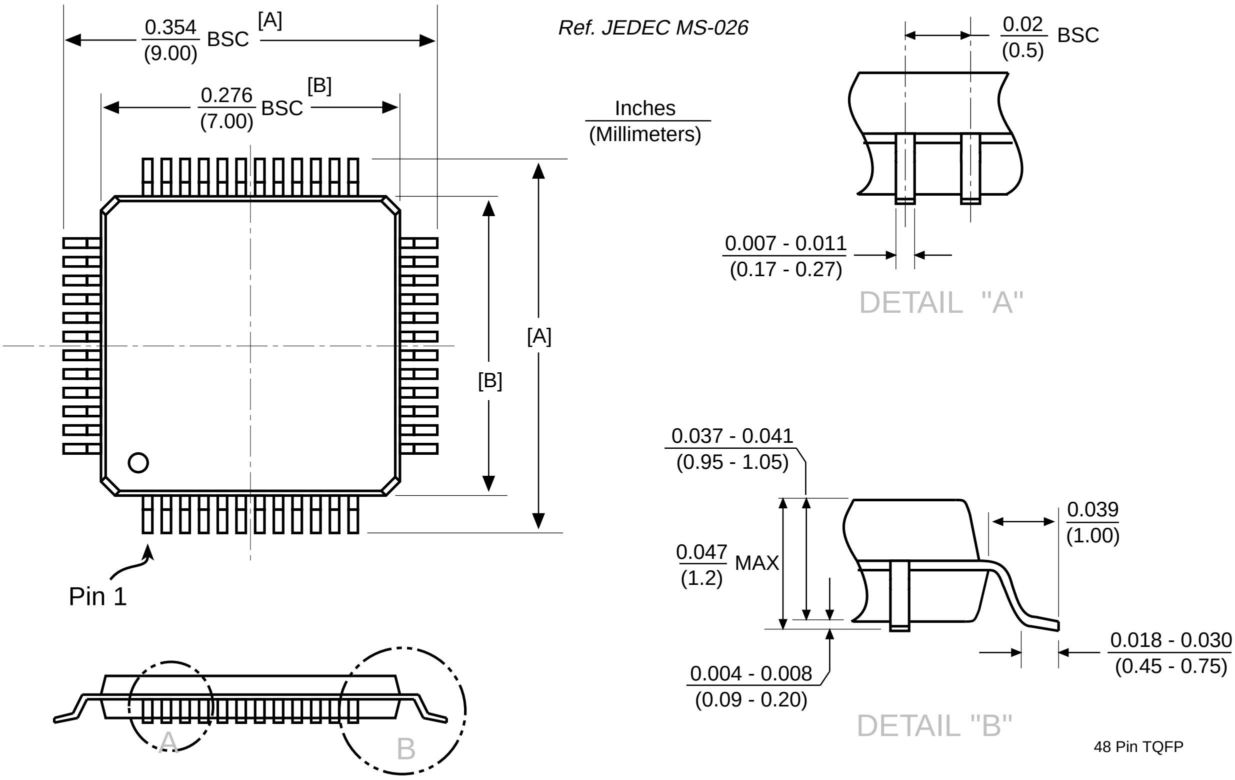
Figure 20. PD Inputs, Physical Offset

PACKAGES

28 PIN SOIC PACKAGE



48 PIN TQFP PACKAGE



ORDERING INFORMATION

SMH4804 F

Base Part Number — SMH4804

Package — F

F = TQFP

S = SOIC

2050 Tree

PART MARKING

SUMMIT

SMH4804 ***n***

L YY WW

n = Package type (F or S)

L = Lot number

YY = Year

WW = Work Week

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