Philips TriMedia™ Processor Companion Supervisor
With a 16K-bit 2-wire Serial Memory

FEATURES

- **Designed to operate with the Philips TriMedia Processor**

- **Coordinating the System Reset Function and Providing the Processor's Configuration Memory**

- **Multiple V_{TRIP} Thresholds**
  - **No External Components Required**
- **Guaranteed Reset Assertion to V_{CC} -1V**

- **Reset is an I/O**
  - **Allows System Reset Clean up**
  - **Provides a De-bounced Manual Reset Function**

- **Industry Standard 2-wire Serial Interface**

- **Hardware Write Lockout Function**

- **High Reliability**
  - **Endurance: 100,000 write cycles**
  - **Data Retention: 100 Years**

OVERVIEW

The SMS8198 is a precision supervisory circuit designed specifically as a companion chip for the Philips TriMedia Processor family. The SMS8198 monitors the power supply and holds the system in reset whenever V_{CC} is below the V_{TRIP} threshold.

In addition to the supervisory function, the SMS8198 has 16K-bits of nonvolatile memory that is used by the TriMedia processor as the boot memory.

The SMS8198 provides 16K-bits of memory that is accessible through the industry standard 2-wire serial interface. By integrating a precision supervisory circuit and the hardware WP input, the SMS8198 becomes the perfect companion chip for the Philips TriMedia processor family. Its functions are integral to the boot hardware operation of the TriMedia processors.

BLOCK DIAGRAM

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Figure 1. Typical Implementation of the SMS8198 and TriMedia Processor

The boot hardware operation begins with the assertion of the reset signal TRI_RESET#. The TRI_RESET# output from the SMS8198 is guaranteed to be valid at V_{CC} -1.0V. The reset output is asserted whenever V_{CC} is less than the V_{TRIP} threshold and will remain asserted after V_{CC} is >V_{TRIP} for the duration of t_{PURST}. Whenever the TRI_RESET# is active the memory will be write protected.

In addition to the reset write protection feature, pin 7 can be tied to a pull-up to disable the write function of the memory. This effectively turns the memory array into an inexpensive boot ROM.

After reset is de-asserted, only the system boot block is allowed to operate. At this point the TriMedia processor takes over and begins to download data from the memory array into its system boot block. The data downloaded contains configuration data to set up the TriMedia processor and to load special ID information into the PCI configuration space register. The ID information is published in the PCI configuration register to provide the 16 bit Subsystem ID and Subsystem Vendor ID.

It should be noted that both the threshold and the t_{PURST} pulse width are programmable. Not only does this provide maximum flexibility to the designer, but, as the processor operating voltage levels migrate downwards, the SMS8198 can be programmed to following this downward trend. The values can be selected from the ordering information table and the devices specified as standard off-the-shelf items.
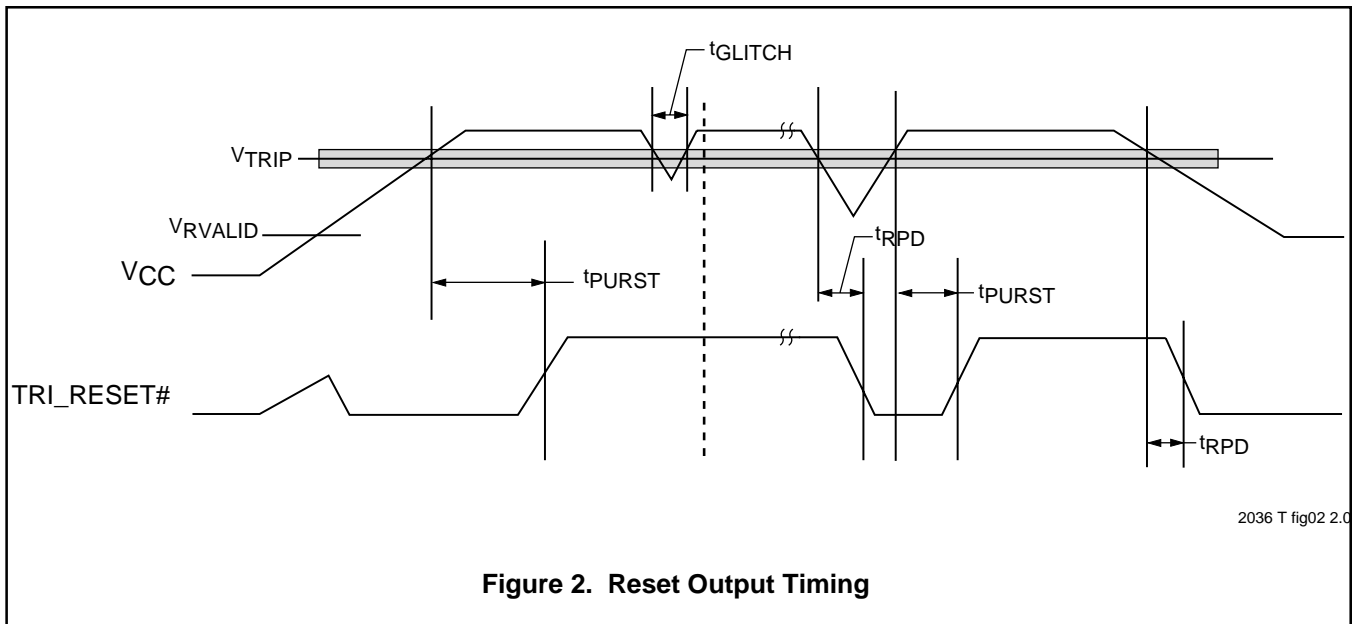
Figure 2. Reset Output Timing

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RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS
T_A = -40°C to +85°C

Symbol	Parameter	Part no. Suffix	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset Trip Point	A (or) Blank	4.250	4.375	4.5	V
		B	4.50	4.625	4.75	V
		2.7	2.55	2.65	2.75	V
t_{PURST}	Reset Timeout			200		ms
t_{RPD}	V_{TRIP} to RESET Output Delay				5	μs
V_{RVALID}	RESET Output Valid to V_{CC} min. Guarantee		1			V
t_{GLITCH}	Glitch Reject Pulse Width note 1			30		ns
V_{OLRS}	RESET Output Low Voltage I_{OL} = 1mA				0.4	V
V_{OHRS}	RESET High Voltage Output I_{OH} = 800μA					

PIN CONFIGURATIONS

8-Pin SOIC

NC	1	8	V_{CC}
TRI_RESET#	2	7	WP
NC	3	6	SCL
GND	4	5	SDA

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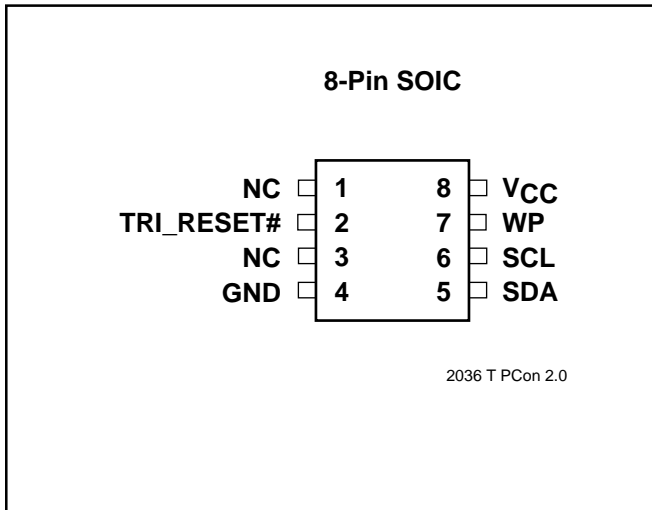
PIN NAMES

SDA	Serial Data I/O
SCL	Serial Clock Input
TRI_RESET#	Reset Output
GND	Ground
V_{CC}	Supply Voltage
WP	Write Protect
NC	No Connect

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

TRI_RESET# - is an active low open drain output. It is driven low whenever V_{CC} is below V_{TRIP}. TRI_RESET# is also an input and can be used to debounce a switch input or perform signal conditioning. The TRI_RESET# pin does have an internal pull-up and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system TRI_RESET# line an external pull-up resistor should be employed.

Write Protect (WP) - All write operations can be disabled by maintaining WP > V_{IH}.

No Connects (NC) - The no connect inputs are unused by the SMS8198; however, to insure proper operation they can be unconnected or tied to ground. They must not be tied to V_{CC}.
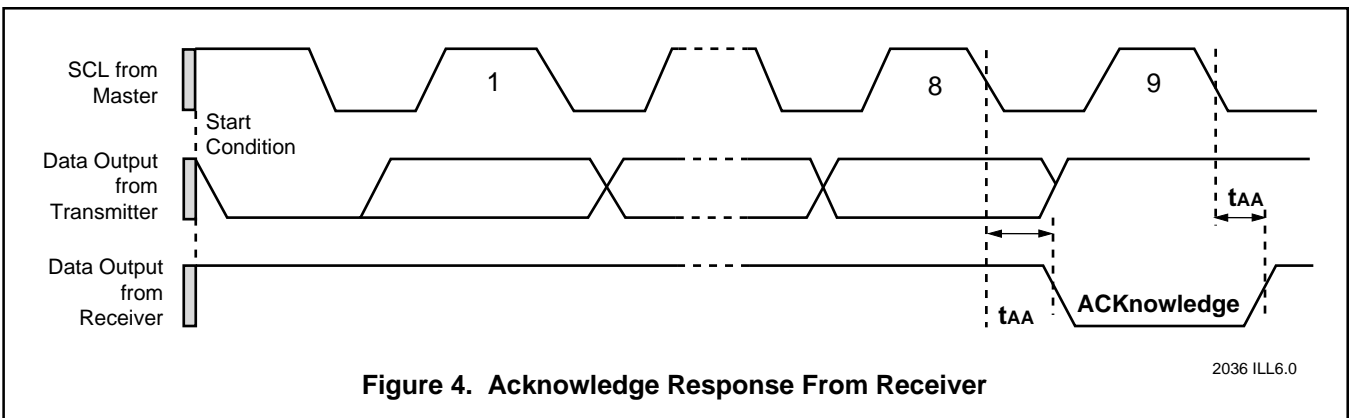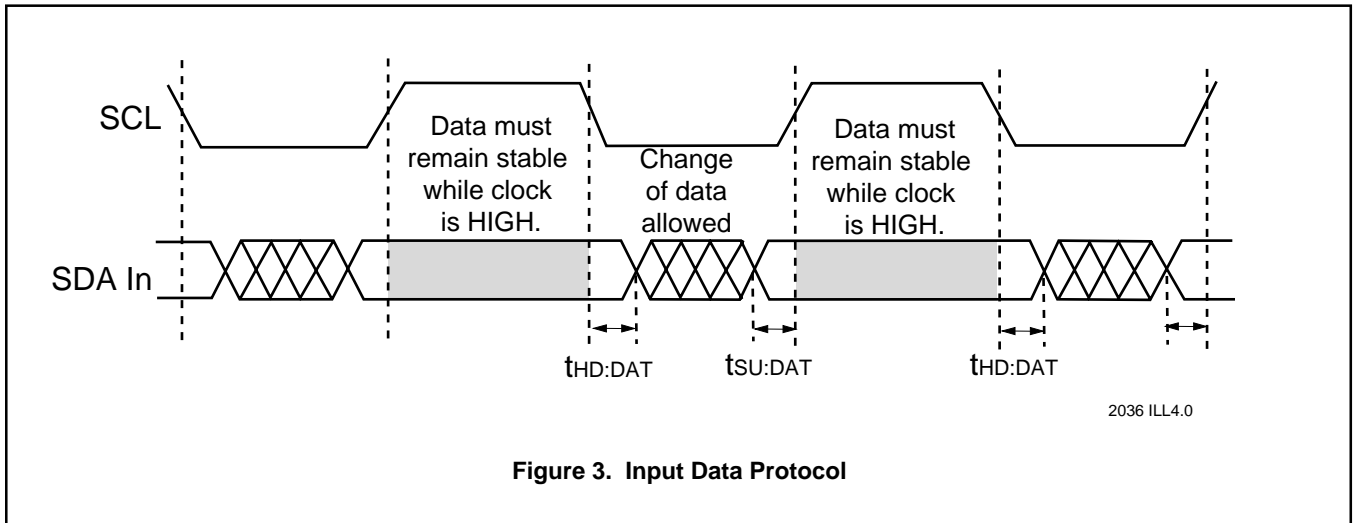
ENDURANCE AND DATA RETENTION

The SMS8198 is designed for applications requiring up to 100,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 erase/write cycles.

RESET CONTROLLER DESCRIPTION

The device provides a precise reset output to a microcontroller and it's associated circuitry ensuring correct system operation during power-up/down conditions and brownout situations. The output is open drain, allowing control of the reset function by multiple devices.

During power-up the reset output remains in a fixed active state until V_{CC} passes through the reset threshold and remains above the threshold for t_{PURST}. The reset output is valid whenever V_{CC} is equal to or greater than 1V. If V_{CC} falls below the threshold for more than t_{GLITCH} the device will immediately generate a reset and drive the output.

The reset pin is an I/O; therefore, forcing the pin to the active state can also manually reset the device. Because the I/O needs to be an open drain, the internal timer can only be triggered by the leading edge of the input. The resulting reset output will either be t_{PURST}, or the externally applied reset signal, whichever is longer. This can provide an affective debounce or reset signal extender solution.

Figure 3. Input Data Protocol

SCL

Data must remain stable while clock is HIGH.

Change of data allowed

Data must remain stable while clock is HIGH.

SDA In

$t_{HD:DAT}$ $t_{SU:DAT}$ $t_{HD:DAT}$

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SCL from Master

Start Condition

1   8   9

Data Output from Transmitter

t_{AA}

Data Output from Receiver

t_{AA} **ACKnowledge**

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Figure 4. Acknowledge Response From Receiver

CHARACTERISTICS OF THE I²C BUS

General Description
The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions
When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The SMS8198 is a 16,384-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the SMS8198 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmit-ting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The SMS8198 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS8198 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS8198 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS8198 will continue to transmit data. If an ACKnowledge is not detected, the SMS8198 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the SMS8198 this is fixed as 1010_{bin}.

Word Address
The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.

Read/Write Bit
The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

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Figure 5. Slave Address Byte
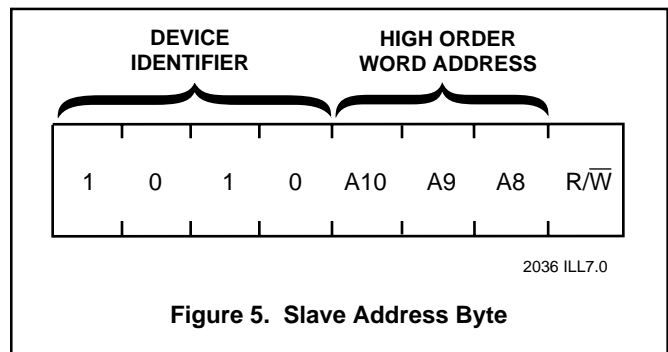
WRITE OPERATIONS

The SMS8198 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the SMS8198 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS8198 begins the internal write cycle.

While the internal write cycle is in progress, the SMS8198 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The SMS8198 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the SMS8198 will respond with an ACKnowledge.

The SMS8198 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.
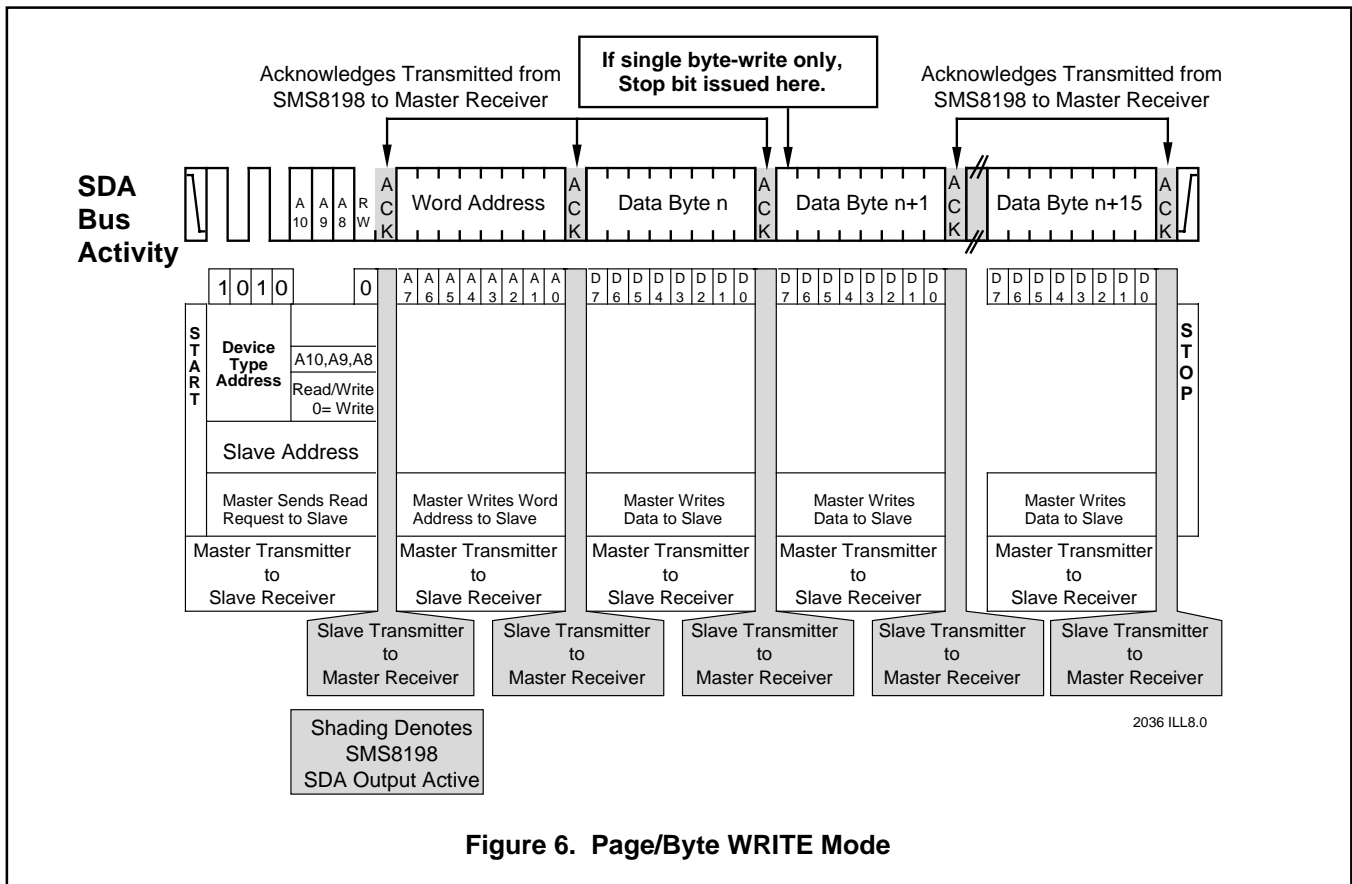

Figure 6. Page/Byte WRITE Mode

Acknowledge Polling

When the SMS8198 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

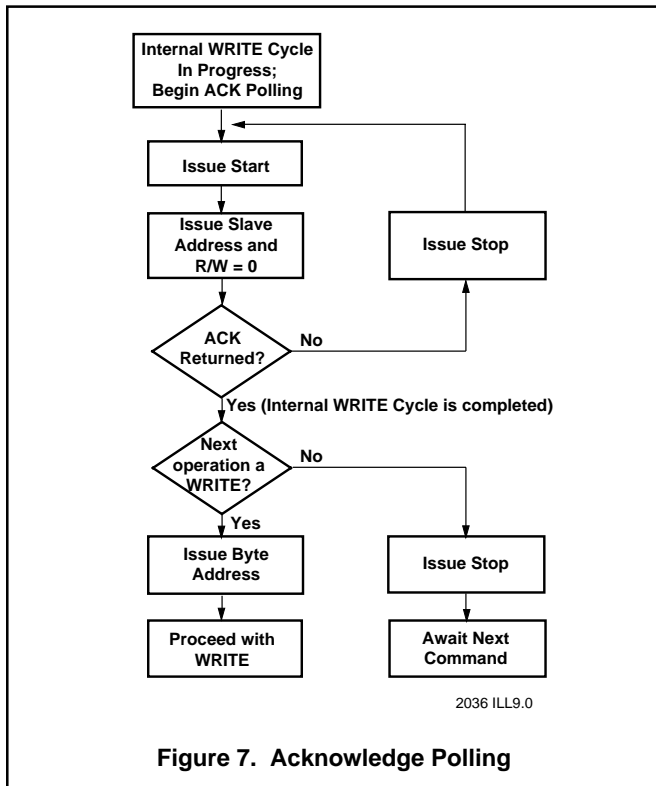To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

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Figure 7. Acknowledge Polling

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The SMS8198 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS8198 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS8198 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.
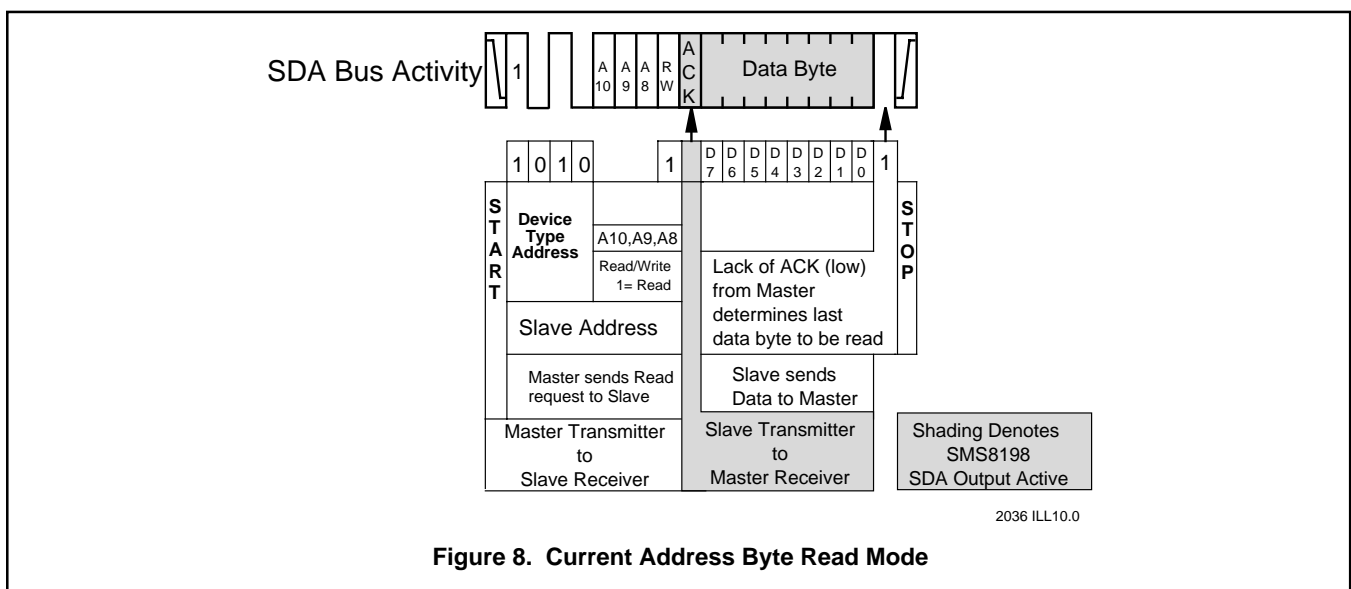
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Figure 8. Current Address Byte Read Mode

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS8198 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS8198 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS8198 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.
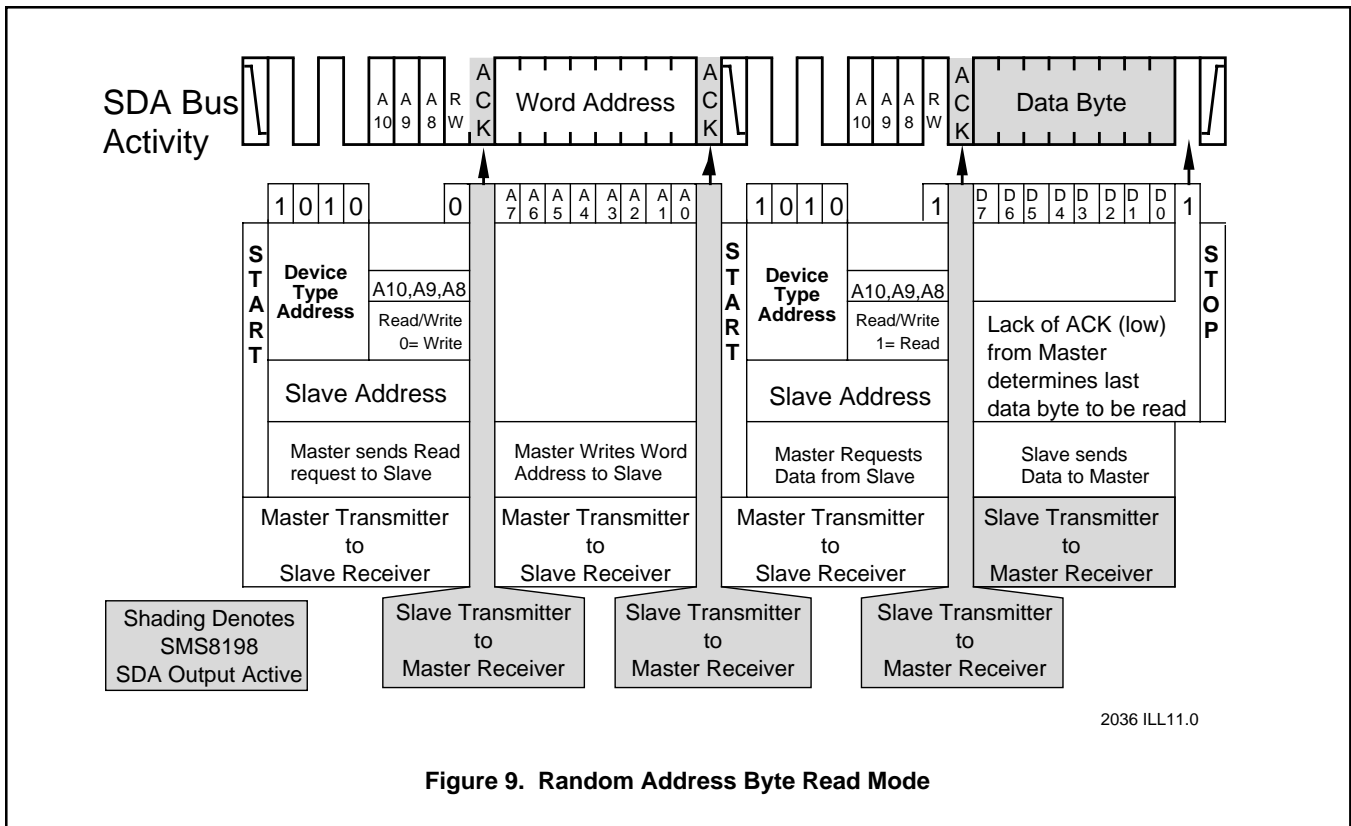

Figure 9. Random Address Byte Read Mode

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Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS8198. The SMS8198 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.
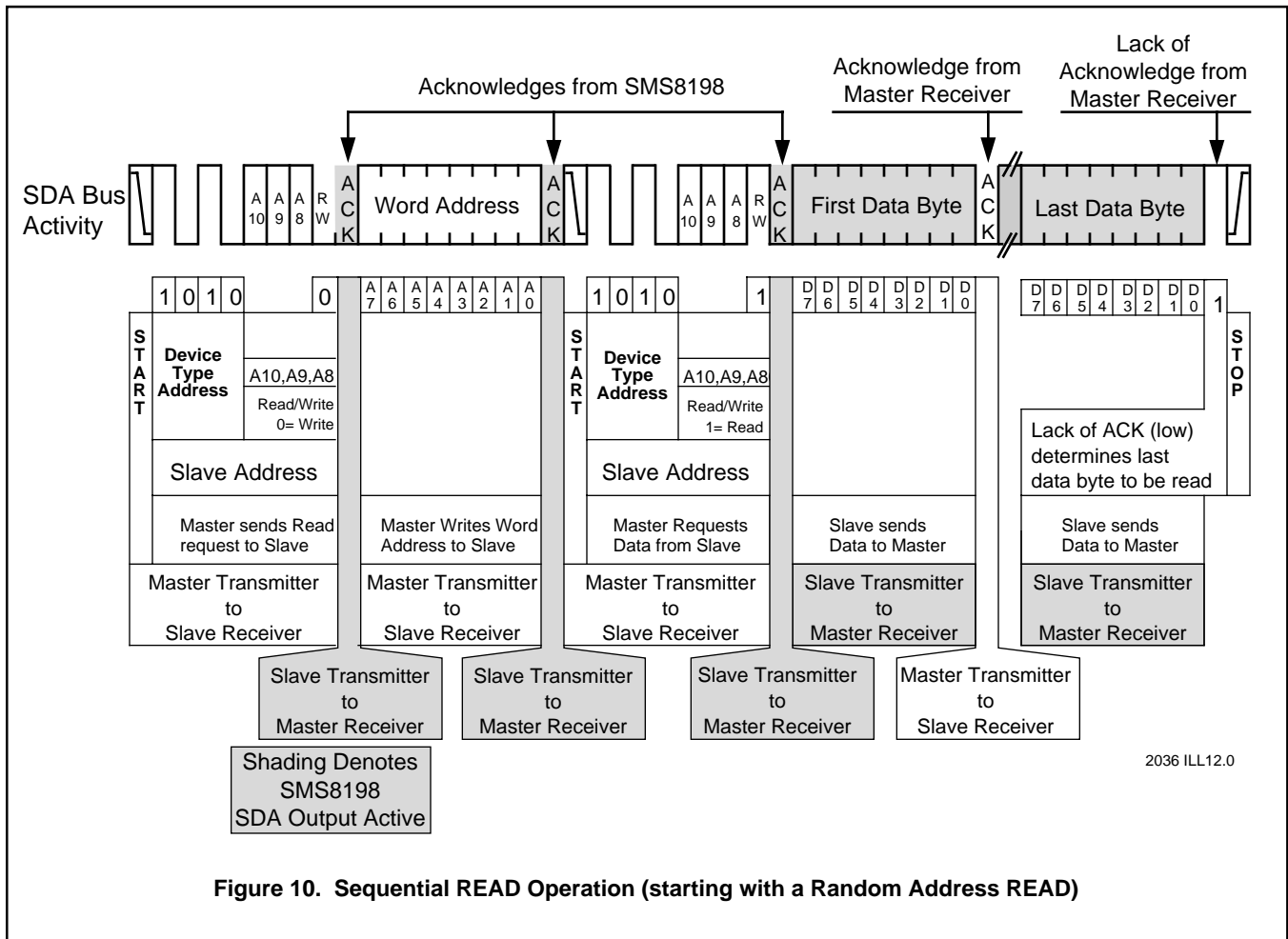

Figure 10. Sequential READ Operation (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... -40°C to +85°C
Storage Temperature .... -65°C to +125°C
Soldering Temperature (less than 10 seconds) .... 300°C
Supply Voltage .... 0 to 6.5V
Voltage on Any Pin .... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

SMS8198, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =3.3V		2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		50	µA
			V_{CC} =3.3V		25	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET			0.3xV_{CC}	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V
V_{ROL}	RESET Low Output	V_{CC} = 1.0V, I_{OL} = 100µA V_{CC} = 2.7V, I_{OL} = 400µA V_{CC} = 4.5V, I_{OL} = 1mA			0.3 0.3 0.4	V V V

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AC ELECTRICAL CHARACTERISTICS

SMS8198, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency		0	100		400	kHz
t_{LOW}	Clock low period		4.7		1.3		µs
t_{HIGH}	Clock high period		4.0		0.6		µs
t_{BUF}	Bus free time	Before new transmission	4.7		1.3		µs
$t_{SU:STA}$	Start condition setup time		4.7		0.6		µs
$t_{HD:STA}$	Start condition hold time		4.0		0.6		µs
$t_{SU:STO}$	Stop condition setup time		4.7		0.6		µs
t_{AA}	Clock to output	SCL low to SDA Data Out valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out hold time	SCL low to SDA Data Out change	0.3		0.2		µs
t_R	SCL and SDA rise time			1		0.3	µs
t_F	SCL and SDA fall time			0.3		0.3	µs
$t_{SU:DAT}$	Data In setup time		250		100		ns
$t_{HD:DAT}$	Data In hold time		0		0		ns
t_I	Noise spike width @ SCL & SDA inputs	Noise suppresion time constant		100		100	ns
t_{WR}	Write cycle time			10		10	ms

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CAPACITANCE

$T_A = 25°C$, f = 100KHz

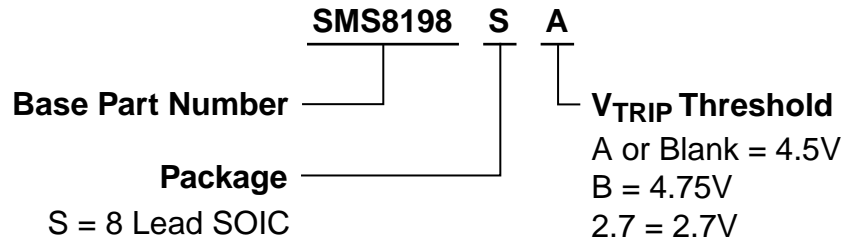| Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2036 PGM T3.0
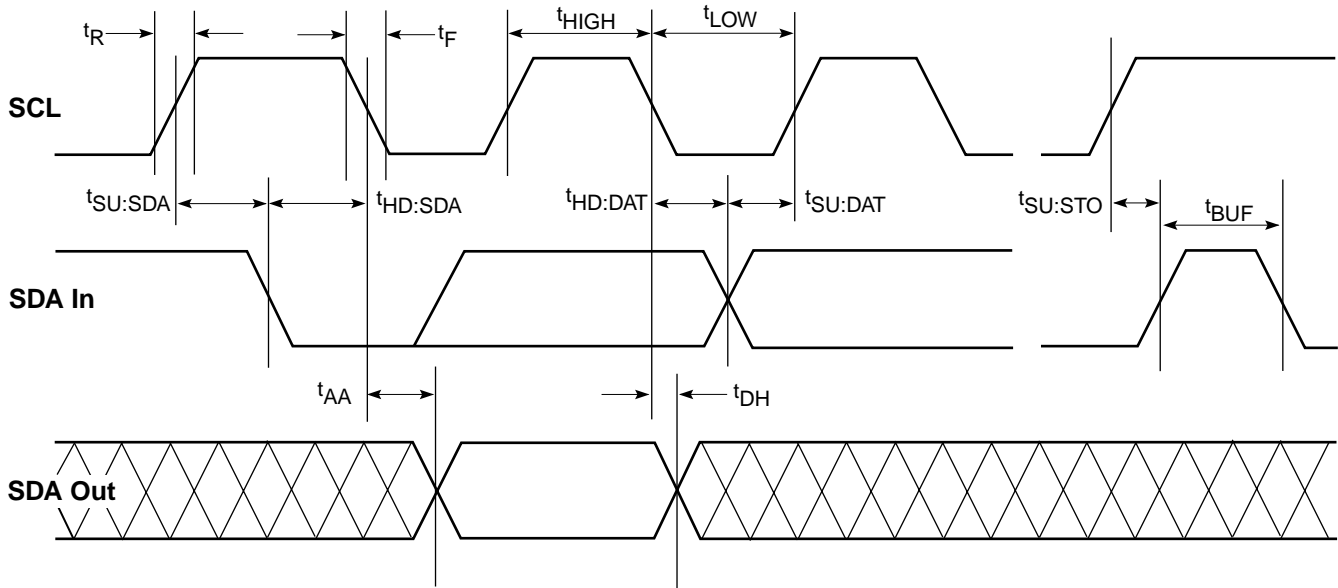
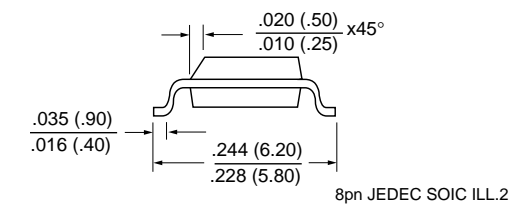2047 Fig07 1.0

Figure 11. Bus Timing

ORDERING INFORMATION

SMS8198   S   A

Base Part Number ——————

Package ——————
S = 8 Lead SOIC

V$_{TRIP}$ Threshold
A or Blank = 4.5V
B = 4.75V
2.7 = 2.7V

2036 Tree 2.0

2036 5.0 4/18/00

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)

.157 (4.00)
.150 (3.80)

1 .196 (5.00)
.189 (4.80)

.061 (1.75)
.053 (1.35)

.0192 (.49)
.0138 (.35)

.0098 (.25)
.004 (.127)

.05 (1.27) TYP.

.050 (1.27) TYP.

.050 (1.270) TYP.
8 Places

.275 (6.99) TYP.

.030 (.762) TYP.
8 Places

FOOTPRINT

.020 (.50) x45°
.010 (.25)

.035 (.90)
.016 (.40)

.244 (6.20)
.228 (5.80)

8pn JEDEC SOIC ILL.2
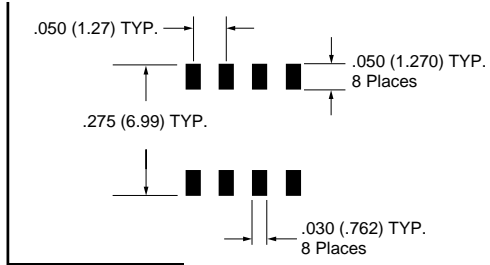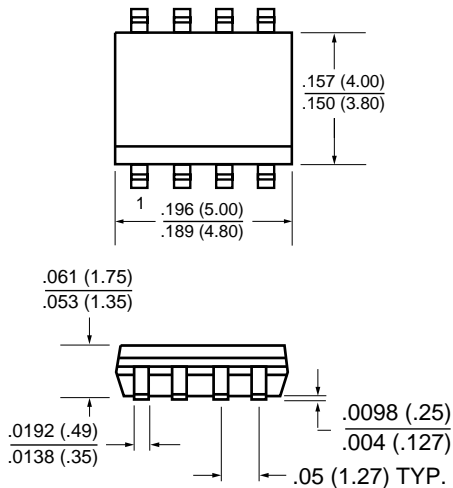
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