Initial Release

250V Low Charge Injection 8-Channel High Voltage Analog Switch

Features

- ❏ HVCMOS® technology for high performance
- ❏ Very low quiescent power dissipation – 10μA
- ❏ Low parasitic capacitances
- ❏ DC to 10MHz analog signal frequency
- ❏ -60dB typical output off isolation at 5MHz
- ❏ CMOS logic circuitry for low power
- ❏ Excellent noise immunity
- ❏ On-chip shift register, latch and clear logic circuitry
- ❏ Flexible high voltage supplies
- ❏ Surface mount package available

Applications

- ❏ Medical ultrasound imaging
- ❏ Piezoelectric transducer drivers
- ❏ Inkjet printer heads
- ❏ Optical MEMS modules

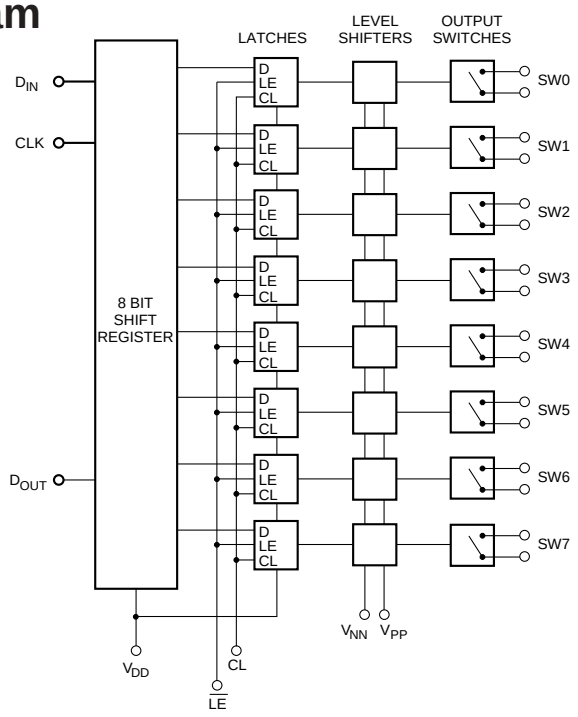
General Description

The Supertex HV214 is a low charge injection 8-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, inkjet printer heads and optical MEMS modules.

Input data is shifted into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS® technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-210V, +125V/-125V, +210V/-40V.

Block Diagram



Ordering Information

$V_{PP} - V_{NN}$	Package Options		
	28-lead plastic chip carrier	48-lead TQFP	Die
250V	HV214PJ	HV214FG	HV214X

Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
DC Electrical Characteristics (T_A=25° C, over recommended operating conditions unless otherwise noted)							
R_{ONS}	Small signal switch on-resistance			55	Ω	I_{SIG}=5.0mA	V_{PP} = +40V, V_{NN} = -210V
				49		I_{SIG}=200mA	
				42		I_{SIG}=5.0mA	V_{PP} = +125V, V_{NN} = -125V
				36		I_{SIG}=200mA	
				38		I_{SIG}=5.0mA	V_{PP} = +210V, V_{NN} = -40V
				32		I_{SIG}=200mA	
ΔR_{ONS}	Small signal switch on-resistance			20	%	I_{SIG} = 5mA, V_{PP} = +125V, V_{NN} = -125V	
R_{ONL}	Large signal switch on-resistance		23		Ω	V_{SIG} = V_{PP}-10V, I_{SIG} = 1A	
I_{SOL}	Switch off leakage per switch			10	μA	V_{SIG} = V_{PP}-10V and V_{NN}+10V	
	DC offset switch off			300	mV	R_{LOAD} = 100KΩ	
	DC offset switch on			500	mV	R_{LOAD} = 100KΩ	
I_{PPQ}	Quiescent V_{PP} supply current			50	μA	All switches off	
I_{NNQ}	Quiescent V_{NN} supply current			-50	μA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current			50	μA	All switches on, I_{SW} = 5mA	
I_{PPQ}	Quiescent V_{NN} supply current			-50	μA	All switches on, I_{SW} = 5mA	
	Switch output peak current			2.0	A	V_{SIG} duty cycle 0.1%	
f_{SW}	Output switch frequency			50	KHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current			7.0	mA	V_{PP}=+40V, V_{NN}=-210V	All output switches are turning On and Off at 50Khz with no load.
				5.0		V_{PP}=+125V, V_{NN}=-125V	
				5.0		V_{PP}=+210V, V_{NN}=-40V	
I_{NN}	Average V_{NN} supply current			-7.0		V_{PP}=+40V, V_{NN}=-210V	
				-5.0		V_{PP}=+125V, V_{NN}=-125V	
				-5.0		V_{PP}=+210V, V_{NN}=-40V	
I_{DDQ}	Quiescent V_{DD} supply current			10	μA		
I_{DD}	Average VDD supply Current			4.0	mA	f_{CLK} = 5MHz, V_{DD} = 5.0V	
I_{SOR}	Data out source current	0.45			mA	V_{OUT} = V_{DD}-0.7V	
I_{SINK}	Data out sink current	0.45			mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance			10	pF		
T_A	Ambient temperature range	0		70	° C		

Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
AC Electrical Characteristics (V_{DD}=5V, T_A=25° C, over recommended operating conditions unless otherwise noted)						
t_{SD}	Set up time before LE* Rises	150			ns	
t_{WLE}	Time width of LE*	150			ns	
t_{DO}	Clock delay time to data out			150	ns	
t_{WCL}	Time width of CL	150			ns	
t_{SU}	Set up time data to clock	15	8.0		ns	
t_H	Hold time data from Clock	35			ns	
f_{CLK}	Clock frequency			5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
t_R, t_F	Clock rise and fall times			50	ns	
T_{ON}	Turn on time			5.0	µs	$V_{SIG} = V_{PP}$-10V, R_{LOAD} =10kΩ
T_{OFF}	Turn off time			5.0	µs	$V_{SIG} = V_{PP}$-10V, R_{LOAD} =10kΩ
dv/dt	Maximum V_{SIG} slew rate			20	V/ns	V_{PP} = +40V, V_{NN} = -210V
				20		V_{PP} = +125V, V_{NN} = -125V
				20		V_{PP} = +210V, V_{NN} = -40V
KO	Off isolation	-30			dB	f = 5.0MHz, 1KΩ/15pF load
		-58				f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60			dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current			300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to Gnd	5.0	12	17	pF	0V, f = 1MHz
$C_{SG(ON)}$	On capacitance SW to Gnd	25	38	50	pF	0V, f = 1MHz
$+V_{SPK}$	Output Voltage Spike			200	mV	V_{PP} = +40V, V_{NN} = -210V, R_{LOAD} = 50Ω
$-V_{SPK}$				200		
$+V_{SPK}$				200	mV	V_{PP} = +125V, V_{NN} = -125V, R_{LOAD} = 50Ω
$-V_{SPK}$				200		
$+V_{SPK}$				200	mV	V_{PP} = +210V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$				200		

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage		-0.5V to +15V
V_{PP} - V_{NN} Supply voltage		260V
V_{PP} Positive high voltage supply		-0.5V to V_{NN} +250V
V_{NN} Negative high voltage supply		+0.5V to -260V
Logic input voltages		-0.5V to V_{DD} +0.3V
Analog Signal Range		V_{NN} to V_{PP}
Peak analog signal current/channel		2.5A
Storage temperature		-65°C to +150°C
Power dissipation	28-pin PLCC	1.2W
	48 lead TQFP	1.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Operating Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	4.5V to 13.2V
V_{PP}	Positive high voltage supply	40V to V_{NN}+ 250V
V_{NN}	Negative high voltage supply	-40V to -210V
V_{IH}	High-level input voltage	V_{DD} -1.5V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak to peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Power Up/Down Sequence:

1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.

2 V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transistion.

3 Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.

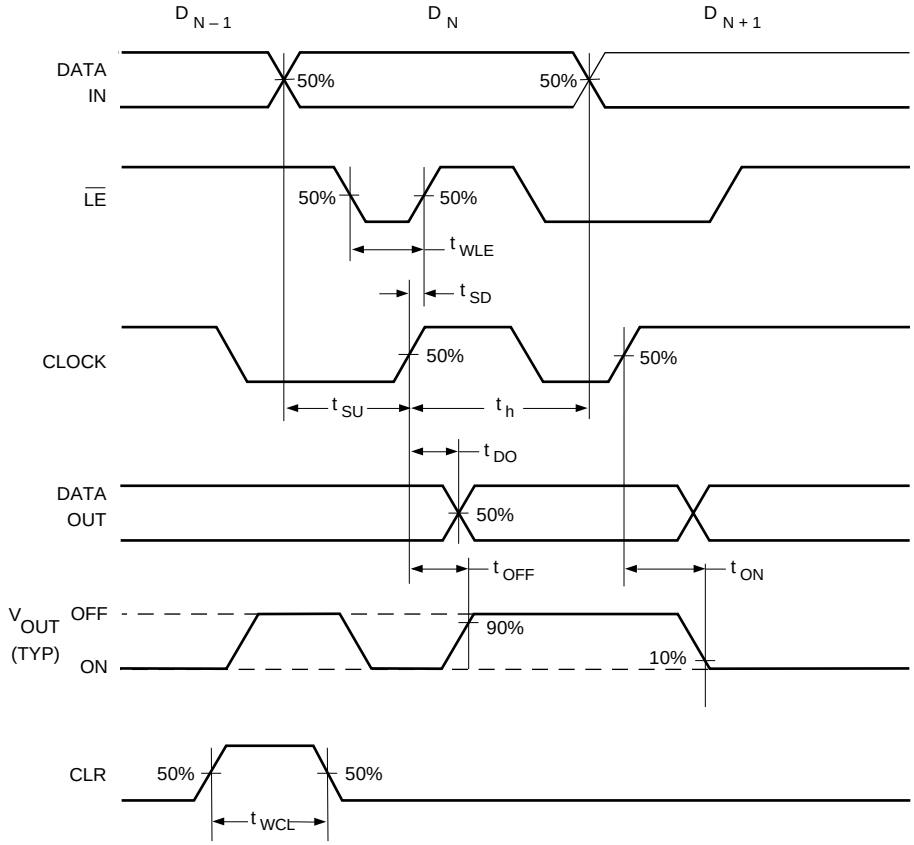
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

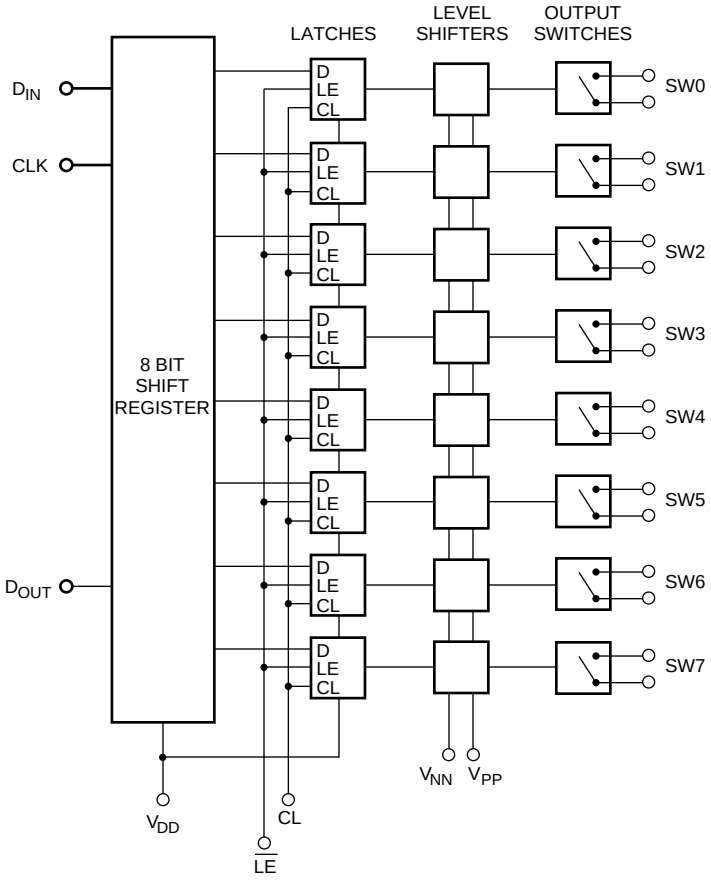
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

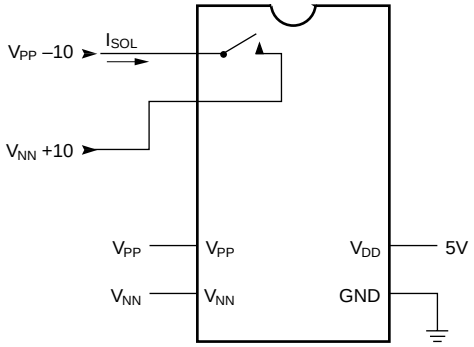
Logic Timing Waveforms



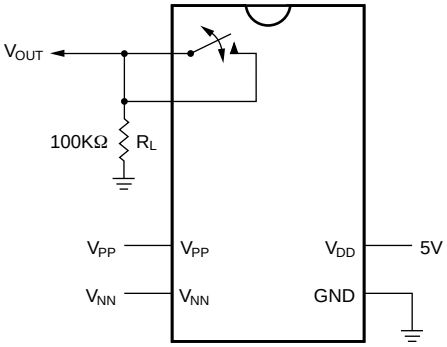
Block Diagram



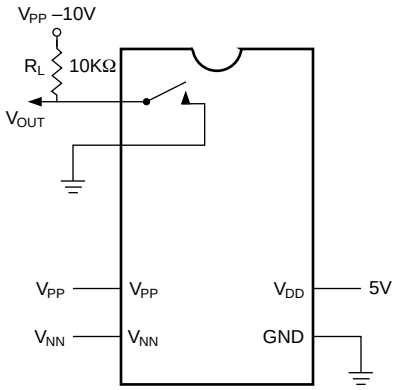
Test Circuits



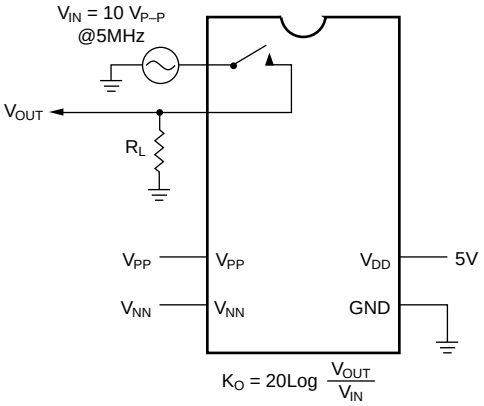
Switch OFF Leakage



DC Offset ON/OFF

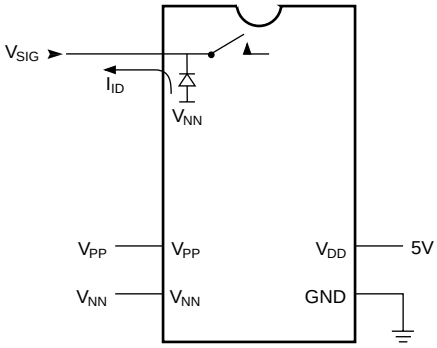


T_{ON}/T_{OFF} Test Circuit

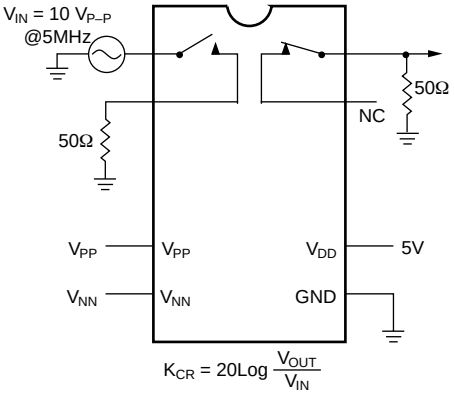


$K_O = 20Log \frac{V_{OUT}}{V_{IN}}$

OFF Isolation

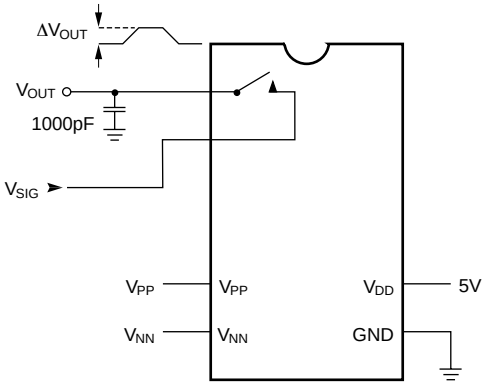


Isolation Diode Current



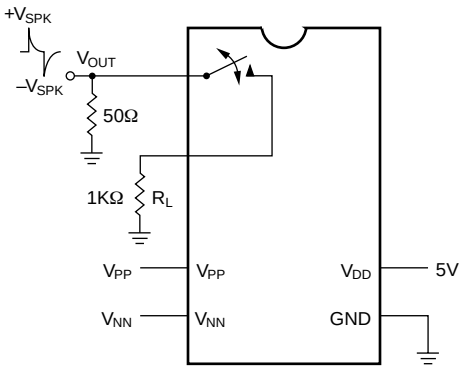
$K_{CR} = 20Log \frac{V_{OUT}}{V_{IN}}$

Crosstalk



$Q = 1000pF \times \Delta V_{OUT}$

Charge Injection



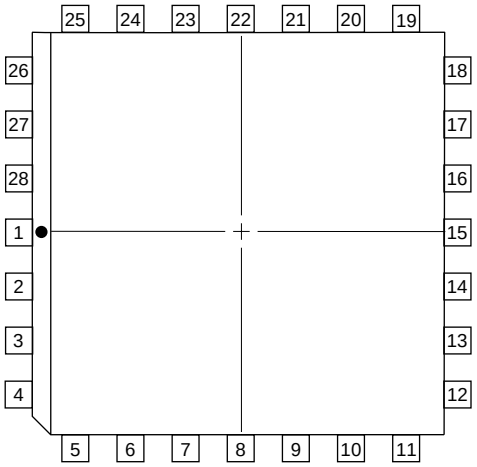
Output Voltage Spike

Pin Configurations

HV214 28 Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	V_{PP}	24	SW6
11	N/C	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

Package Outlines



top view

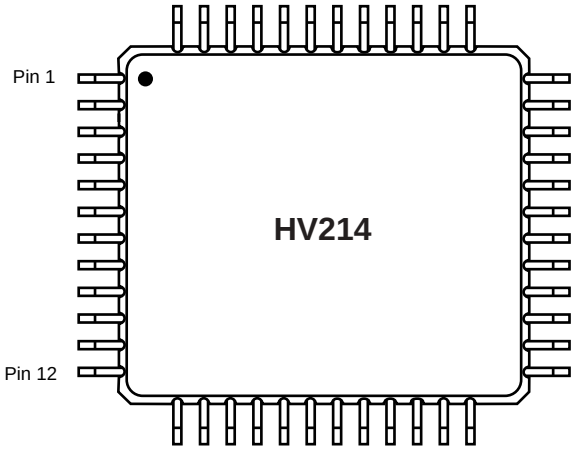
28-pin J-Lead Package

Pin Configurations

HV214 48-Pin TQFP

Pin	Function	Pin	Function
1	SW5	25	V_{NN}
2	N/C	26	N/C
3	SW4	27	N/C
4	N/C	28	GND
5	SW4	29	V_{DD}
6	N/C	30	N/C
7	N/C	31	N/C
8	SW3	32	N/C
9	N/C	33	D_{IN}
10	SW3	34	CLK
11	N/C	35	$\overline{LE}$
12	SW2	36	CLR
13	N/C	37	D_{OUT}
14	SW2	38	N/C
15	N/C	39	SW7
16	SW1	40	N/C
17	N/C	41	SW7
18	SW1	42	N/C
19	N/C	43	SW6
20	SW0	44	N/C
21	N/C	45	SW6
22	SW0	46	N/C
23	N/C	47	SW5
24	V_{PP}	48	N/C

Package Outlines



top view

48-pin TQFP

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