N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-92	TO-243AA*	Die**
500V	13Ω	0.5A	VN2450N3	VN2450N8	VN2450NW

* Same as SOT-89 Product Supplied on 2000 piece carrier tape reels.
** Die in wafer form.

Product marking for TO-243AA:

VN4E✳

Where ✳ = 2-week alpha date code

Features

- ❑ Free from secondary breakdown
- ❑ Low input and output leakage
- ❑ Low C_{ISS} and fast switching speeds
- ❑ High input impedance and high gain

Applications

- ❑ Motor controls
- ❑ Converters
- ❑ Amplifiers
- ❑ Switches
- ❑ Power supply circuits
- ❑ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Advanced DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

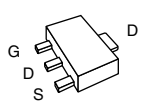
Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Package Options



TO-243AA
(SOT-89)

TO-92

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	0.25A	0.75A	1.6W†	15	78 †	0.25A	0.75A
TO-92	0.2A	0.65A	1W	125	170	0.2A	0.65A

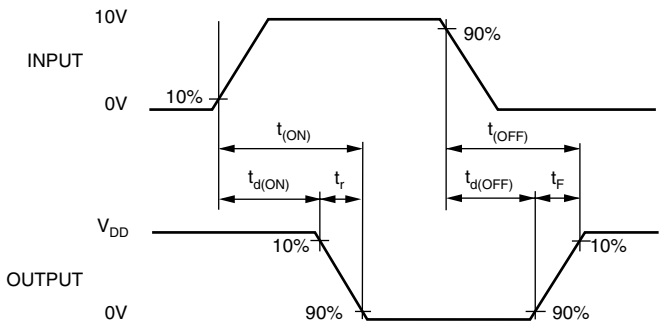
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

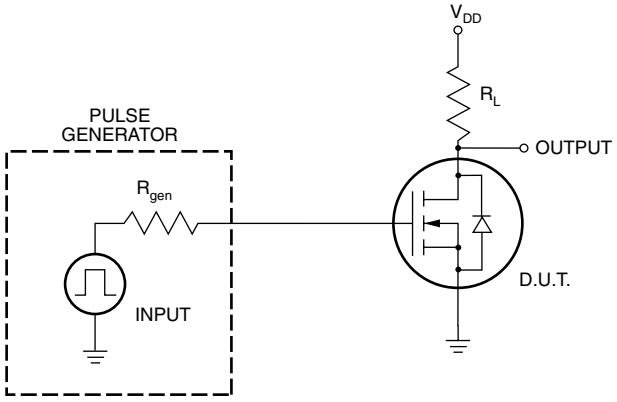
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500			V	V_{GS} = 0V, I_D = 2.0mA
$V_{GS(th)}$	Gate Threshold Voltage	1.5			V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	V_{GS} = 0V, V_{DS} = Max Rating
				1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	0.5			A	V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	Ω	V_{GS} = 4.5V, I_D = 100mA
				13		V_{GS} = 10V, I_D = 400mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/°C	V_{GS} = 10V, I_D = 400mA
G_{FS}	Forward Transconductance	50			m℧	V_{DS} = 25V, I_D = 200mA
C_{ISS}	Input Capacitance			150	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0 MHz
C_{OSS}	Common Source Output Capacitance			50		
C_{RSS}	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = 25V, I_D = 250mA, R_{GEN} = 25Ω
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.5	V	V_{GS} = 0V, I_{SD} = 400mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

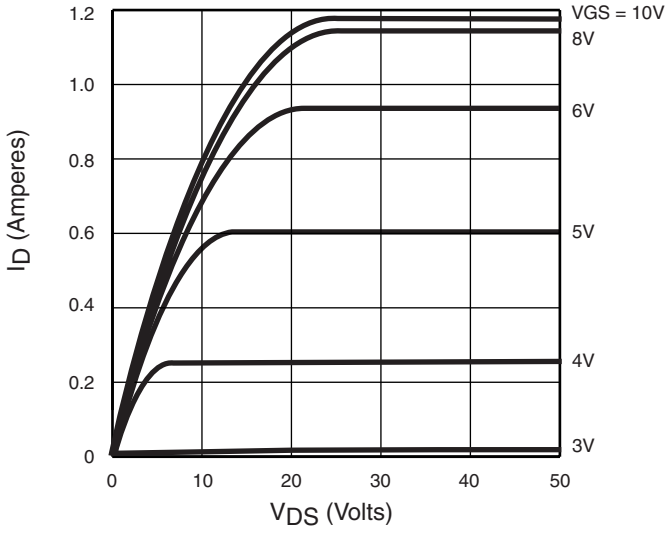
Switching Waveforms and Test Circuit



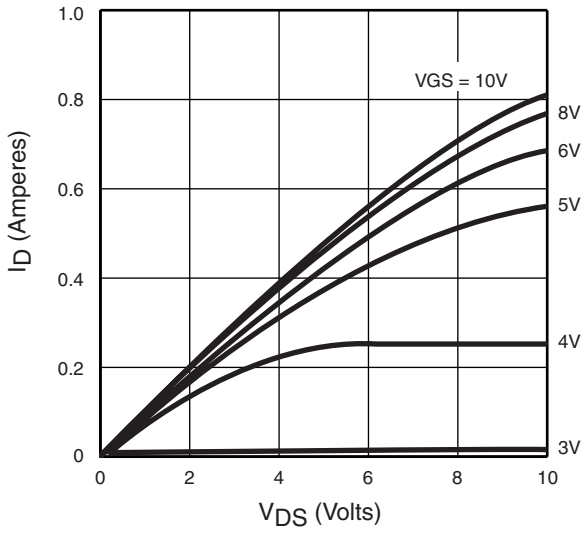


Typical Performance Curves

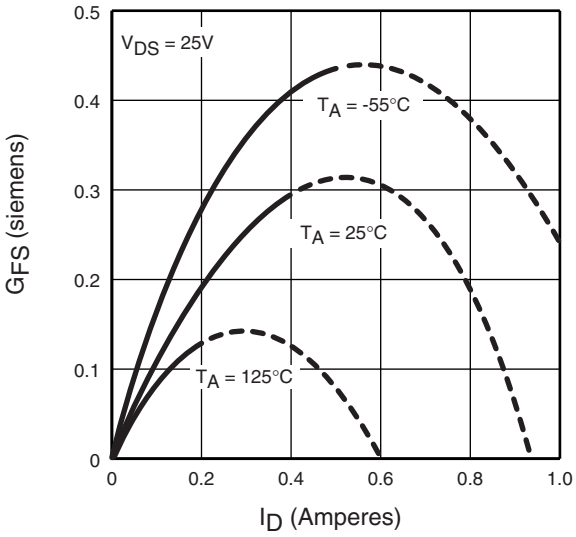
Output Characteristics



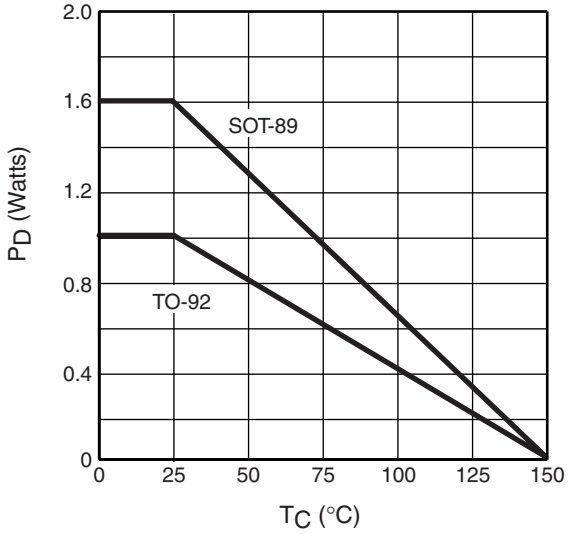
Saturation Characteristics



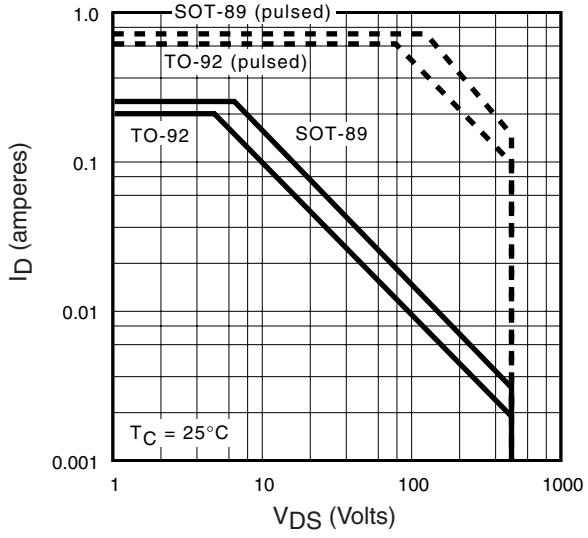
Transconductance vs. Drain Current



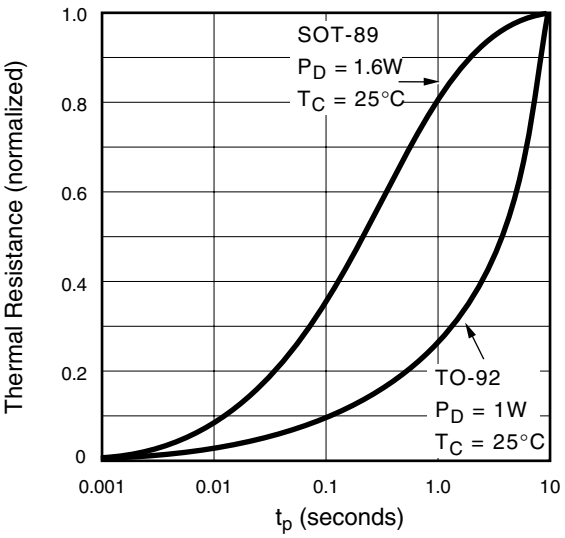
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

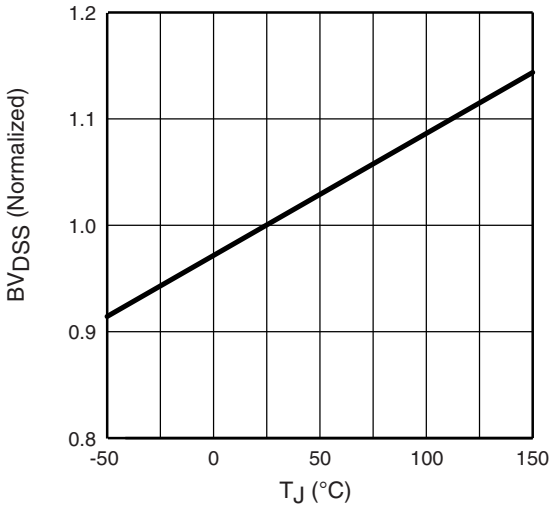


Thermal Response Characteristics

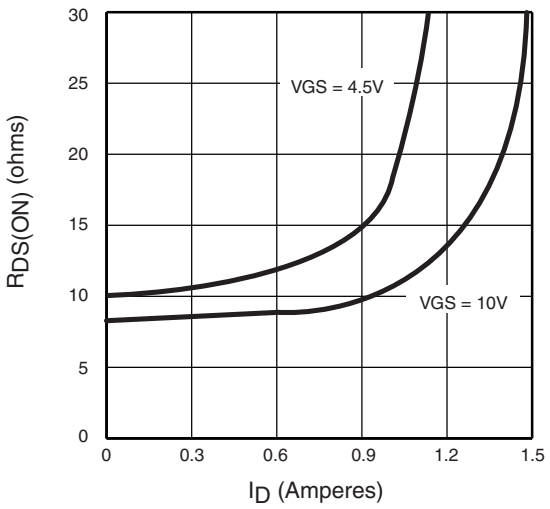


Typical Performance Curves

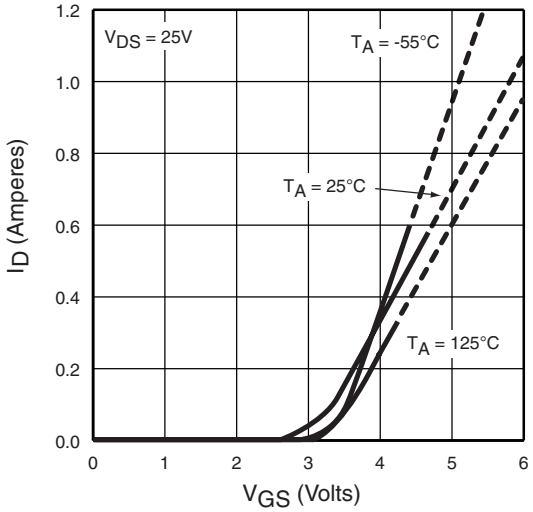
BV_{DSS} Variation with Temperature



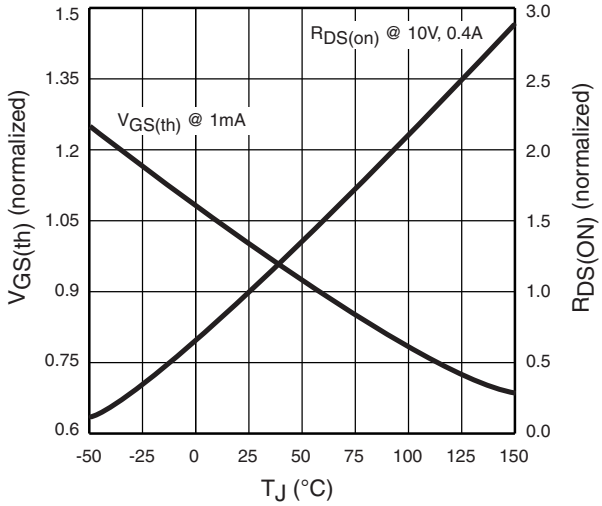
On Resistance vs. Drain Current



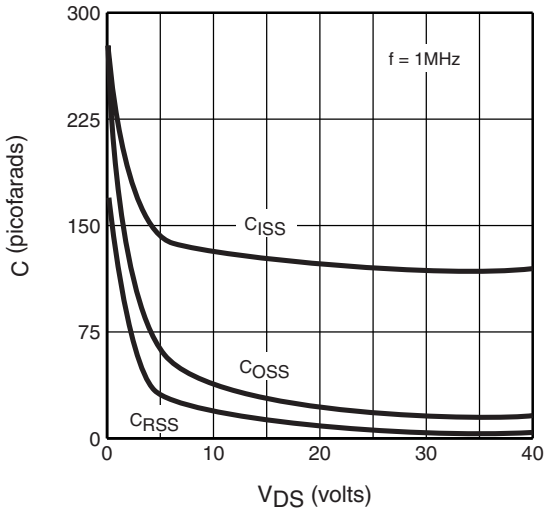
Transfer Characteristics



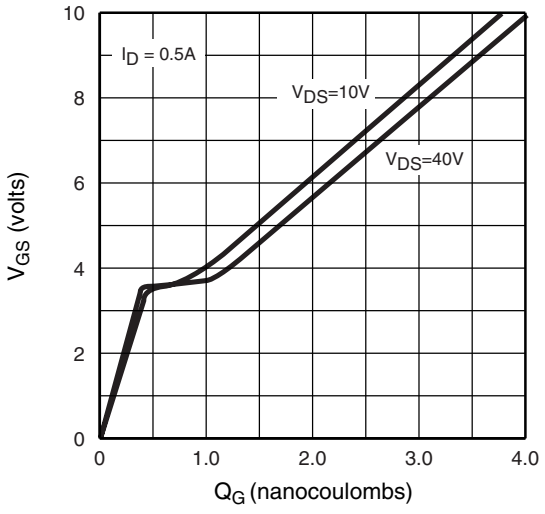
$V_{GS(TH)}$ and $R_{DS(ON)}$ w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



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