



# N-Channel Enhancement-Mode Vertical DMOS FETs

## **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	V <sub>GS(th)</sub>	Order Number / Package			
BV <sub>DGS</sub>	(max)	(max)	TO-92	14-Pin P-DIP	TO-243AA*	Die <sup>†</sup>
50V	0.3Ω	2.4V	VN3205N3	VN3205N6	VN3205N8	VN3205ND

<sup>\*</sup> Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

### Product marking for TO-243AA:

VN2L\*

Where \* = 2-week alpha date code

## **Features**

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

## **Applications**

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## **Absolute Maximum Ratings**

Drain-to-Source Voltage	$BV_{DSS}$
Drain-to-Gate Voltage	$BV_{DGS}$
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

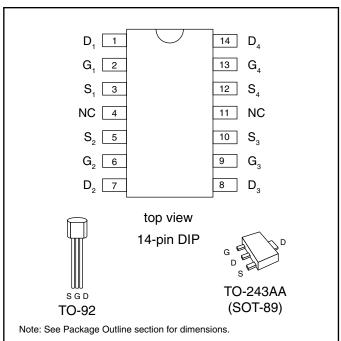
<sup>\*</sup> Distance of 1.6 mm from case for 10 seconds.

## **Advanced DMOS Technology**

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## **Package Options**



<sup>†</sup> MIL visual screening available

## **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>C</sub> = 25°C	$ heta_{ extsf{jc}}$ $^{\circ}$ C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-92	1.2A	8.0A	1.0W	125	170	1.2A	8.0A
SOT-89	1.5A	8.0A	$1.6W (T_A = 25^{\circ}C)$	15	78 <sup>†</sup>	1.5A	8.0A
Plastic DIP	1.5A	8.0A	3.0W <sup>‡</sup>	41.6‡	83.3‡	1.5A	8.0A

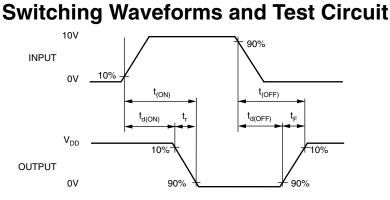
<sup>\*</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .  $T_A = 25$ °C.

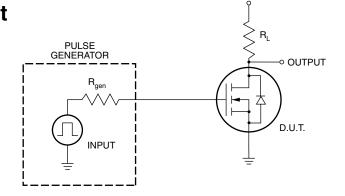
# Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Тур	Max	Unit	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage		50			V	$V_{GS} = 0V$ , $I_D = 10mA$	
V <sub>GS(th)</sub>	Gate Threshold Voltage		0.8		2.4	٧	$V_{GS} = V_{DS}$ , $I_D = 10$ mA	
$\Delta V_{GS(th)}$	Change in V <sub>GS(th)</sub> with Temperature			-4.3	-5.5	mV/°C	$V_{GS} = V_{DS}$ , $I_D = 10$ mA	
I <sub>GSS</sub>	Gate Body Leakage			1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I <sub>DSS</sub>	I <sub>DSS</sub> Zero Gate Voltage Drain Current				10	μА	$V_{GS} = 0V$ , $V_{DS} = Max$ Rating	
					1	mA	$V_{GS} = 0V$ , $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I <sub>D(ON)</sub>	ON-State Drain Current		3.0	14		Α	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 5V	
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance	TO-92 and P-DIP			0.45	Ω	$V_{GS} = 4.5V, I_D = 1.5A$	
		SOT-89			0.45	Ω	$V_{GS} = 4.5V, I_D = 0.75A$	
		TO-92 and P-DIP			0.3	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3A	
		SOT-89			0.3	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.5A	
$\Delta R_{DS(ON)}$	Change in R <sub>DS(ON)</sub> with Temperature			0.85	1.2	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3A	
G <sub>FS</sub>	Forward Transconductance		1.0	1.5		Ö	$V_{DS} = 25V, I_{D} = 2A$	
C <sub>ISS</sub>	Input Capacitance			220	300		V 0V V 05V	
C <sub>OSS</sub>	Common Source Output Capacitance			70	120	pF	$V_{GS} = 0V$ , $V_{DS} = 25V$ f = 1 MHz	
C <sub>RSS</sub>	Reverse Transfer Capac	citance		20	30			
t <sub>d(ON)</sub>	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$ $I_D = 2A$ $R_{GEN} = 10\Omega$	
t <sub>r</sub>	Rise Time				15			
t <sub>d(OFF)</sub>	Turn-OFF Delay Time				25			
t <sub>f</sub>	Fall Time				25			
V <sub>SD</sub>	Diode Forward Voltage Drop				1.6	V	$V_{GS} = 0V, I_{SD} = 1.5A$	
t <sub>rr</sub>	Reverse Recovery Time			300		ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 1A	

#### Notes:

All A.C. parameters sample tested.



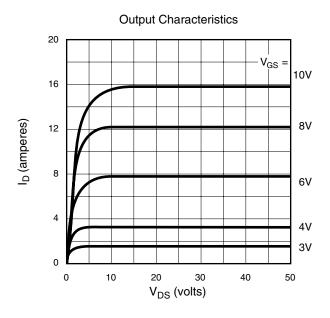


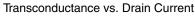
<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P<sub>D</sub> increase possible on ceramic substrate.

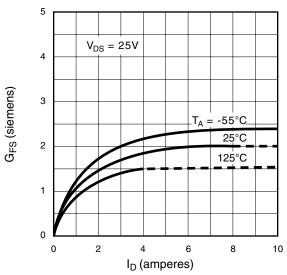
<sup>&</sup>lt;sup>‡</sup> Total for package.

<sup>1.</sup> All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test:  $300\mu s$  pulse, 2% duty cycle.)

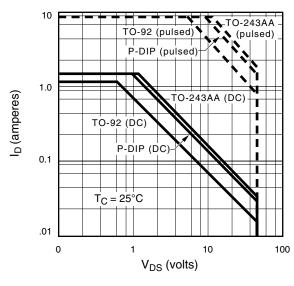
# **Typical Performance Curves**



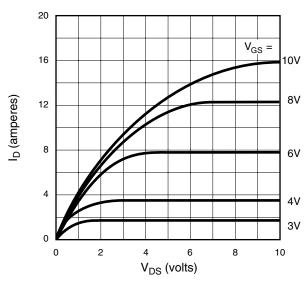




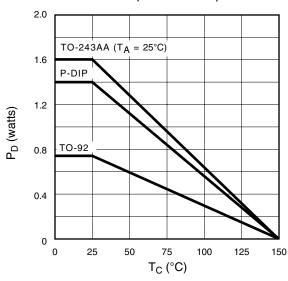
### Maximum Rated Safe Operating Area



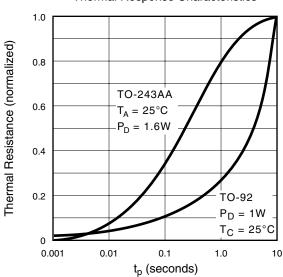
#### Saturation Characteristics



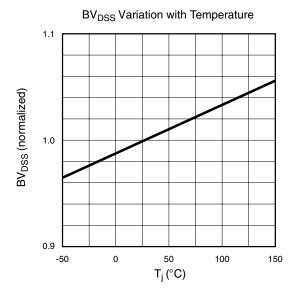
#### Power Dissipation vs. Temperature

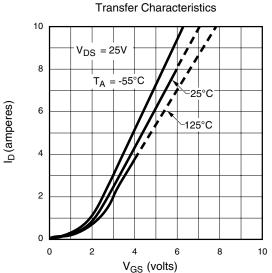


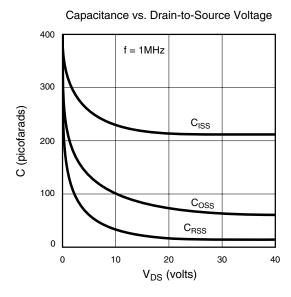
#### Thermal Response Characteristics

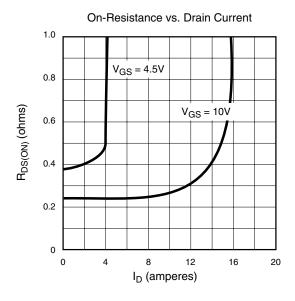


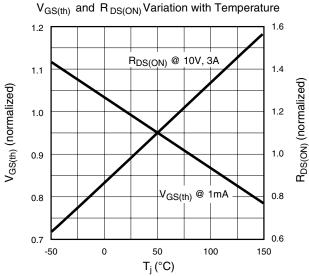
# **Typical Performance Curves**

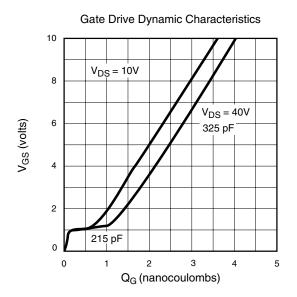












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