Super Device Microelectronics Co., Ltd.

SD101B Low Power Receiver IC

Description

The SD101B is a low power receiver IC and it is suitable for use in a variety of low power radio applications including remote keyless entry. The SD101B is based on a single-conversion, super-heterodyne receiver architecture and incorporates an entire phase-locked loop (PLL) for precise local oscillator generation. In addition, the SD101B provides an RSSI output.

Features

- Extremely low power operation
- Low external part count
- Receiver input frequency : 290 ~ 460 MHz
- On-chip VCO with integrated PLL using crystal oscillator reference
- PLL power down feature
- Integrated IF and data filters
- RSSI output
- SSOP-24 package (0.64 mm pitch)

Applications

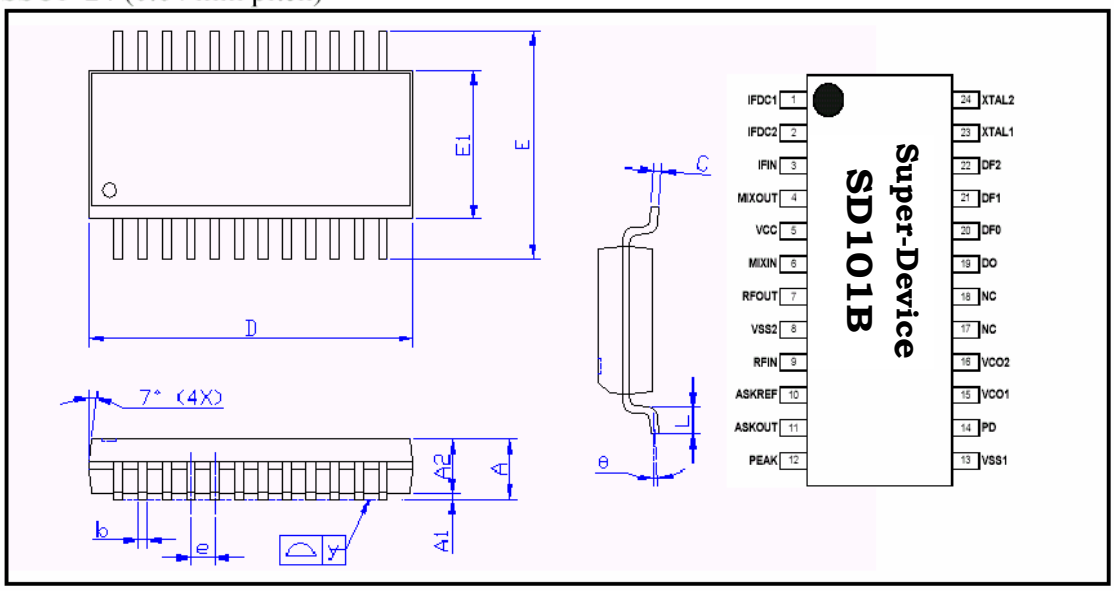
- Wireless mouse
- Video sender remote controller
- Car alarm and home security systems

Functional Description

The SD101B receiver IC incorporates an LNA; mixer; PLL-based local oscillator including VCO, fixed divider (÷ 64), reference crystal oscillator, phase-frequency detector (PFD), and charge pump; IF filter; logarithmic amplifier; data filter; peak detector; and 1bit comparator and is capable of demodulating ASK input signals.

Package and Pin Assignment

SSOP-24 (0.64 mm pitch)



Symbols	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.60	1.75	0.053	0.064	0.069
A1	0.10	—	0.25	0.004		0.010
A2	—	1.45	—	—	0.057	—
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.19	—	0.25	0.007	—	0.010
D	8.55	—	8.75	0.337	—	0.344
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e	—	0.64	—	—	0.025	—
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
0	0^0	—	g^0	0^0	—	8^0

Pin Descriptions

Number	Name	Description
1	IFDC1	If amplifier feedback decoupling connections
2	IFDC2	
3	IFIN	IF amplifier input
4	MIXOUT	Mixer output
5	VCC	Nominal 5V supply
6	MIXIN	RF mixer input
7	RFOUT	Open collector LNA output
8	VSS2	LNA ground
9	RFIN	LNA input
10	ASKREF	Comparator reference level
11	ASKOUT	Comparator output
12	PEAK	Peak detector output

Number	Name	Description
13	VSS1	Ground
14	PD	PLL power down: low
15	VCO1	Open collector differential VCO outputs
16	VCO2	
17	NC	No connection
18	RSS1	RSSI output
19	DO	Charge pump output
20	DF0	Data filter external connections
21	DF1	
22	DF2	
23	XTAL1	Crystal oscillator external connections
24	XTAL2	

Absolute Maximum Ratings

$V_{SS} = V_{SS1} = V_{SS2} = 0V$

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	V_{SS}-0.5 to V_{SS} +8.0	V
Operating temperature range	T_{OPR}	-40 to 85	^{O}C
Storage temperature range	T_{STG}	-55 to 150	^{O}C
Soldering temperature range	T_{SLD}	255	^{O}C
Soldering time range	T_{SLD}	10	s

Recommended Operating Conditions

$V_{SS} = V_{SS2} = 0V$

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	V_{CC}	4.75	5.0	7.0	V
RF input frequency	F_{RFIN}	290		460	MHZ
Operating temperature	T_A	-10	25	60	^{O}C

Electrical Characteristics

(V_{CC}= 4.75 to 7.0 V,V_{SS1} = OV , T_A = -40 to 85□ unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Current consumption	$I_{CC,total}$	V_{CC} = 5V		2.4	3.0	mA
Current consumption(PLL off)	$I_{CC,noPLL}$	V_{CC}=5V;V_{PD}=OV		1.8	2.4	mA
Sensitivity[a]	α_{SENS}	f_{RFIN}=434MHz;2KB/s		-103	-100	dBm
Signal handling[b]	α_{SH}		-30			dBm
Integrated IF filter-3-dB low pass cutoff frequency	$f_{IF,-3dB}$		450	550	750	KHz
Adjacent channel rejection[c]	α_{ACR}			65		dB
ASK output duty ratio	DR		40	50	60	%
Peak detector source current	I_{peak}			500		µA
Peak detector leakage current	I_{leak}				250	nA
Charge pump source/sink current	I_{CP}			±30		µA
PD logic HIGH input voltage	$V_{IL,PD}$		V_{CC} -0.5		V_{CC} +0.5	V
PD logic LOW input voltage	$V_{IL,PD}$		V_{SS2} -0.5		V_{SS2} -0.5	V
ASKOUT logic HIGH output voltage	$V_{OH,ASKOUT}$	I_{load} = 10µA	0.7* V_{CC}			V
ASKOUT logic LOW output voltage	$V_{OL,ASKOUT}$	I_{load} = 10µA			0.3* V_{CC}	V

Note of Electrical Characteristics

- Sensitivity is defined as the minimum average signal level measured at the input which is necessary to achieve a bit error rate of 0.01 when the input signal is a return-to-zero (RZ) pulse with an average duty cycle of 50%. The RF input is assumed to be matched to 50 ohms.
- Signal handling is defined as the maximum input signal capable of being successfully demodulated. It is assumed that the input signal is ASK modulated with a minimum extinction ratio of 40 dB. The RF input is assumed to be matched to 50 ohms.
- Adjacent channel rejection is defined for an interfering tone αACR [dB] above the receiving threshold and 10 MHz offset from the carrier giving a 3dB reduction in sensitivity.

Contact information

Super Device

For additional information please visit
http://www.super-device.com.tw
Tel: +886-2-8226-1788
Fax: +886-2-8226-2277
e-mail: sd@super-device.com.tw

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