

ADC150 Programmable Integrating A/D Converter



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FEATURES

- 24 BIT RESOLUTION
- SOFTWARE SELECTABLE FEATURES
- 0.5ppm/°C MAX. SCALE FACTOR ERROR
- 2 ppm MAX. LINEARITY ERROR
- AUTO ZERO
- BUS COMPATIBLE
- INTERNAL CLOCK and REFERENCE
- LOW POWER CONSUMPTION (0.450 WATTS)

APPLICATIONS

- TEST EQUIPMENT
- DATA ACQUISITION
- SCIENTIFIC INSTRUMENTS
- MEDICAL INSTRUMENTS
- SEISMOLOGICAL EQUIPMENT
- ROBOTIC SYSTEMS
- WEIGHING SYSTEMS

DESCRIPTION

ADC150 is a high performance programmable 24-bit integrating A/D converter based on a patented architecture. The integration time and resolution along with the power line cycle selection can be easily programmed through the Mode Control Byte.

ADC150 offers 2 ppm max. linearity error and 1 ppm/°C max. scale factor error over the military temperature range. It also has excellent offset stability at 2 ppm max. which the user can auto zero if desired.

ADC150's compatibility with popular microcomputer buses increases its ease of application in smart systems. An on-board microprocessor controls all internal functions of the ADC150. Thaler designers have minimized external connections to greatly reduce the problem often encountered when applying ADC's.

Operating from ± 15 VDC and a +5VDC power supply, ADC150 is packaged in a hermetically sealed 40-pin ceramic DIP package. Precision test equipment, scientific and medical instruments, and data acquisition systems are primary application areas for the unusually high resolution and accuracy of this ADC.

Type	Temperature Operating Range	Max. Scale Factor Deviation
ADC150C	-25°C to +85°C	60ppm
ADC150CA	-25°C to +85°C	30ppm
ADC150M	-55°C to +125°C	100ppm

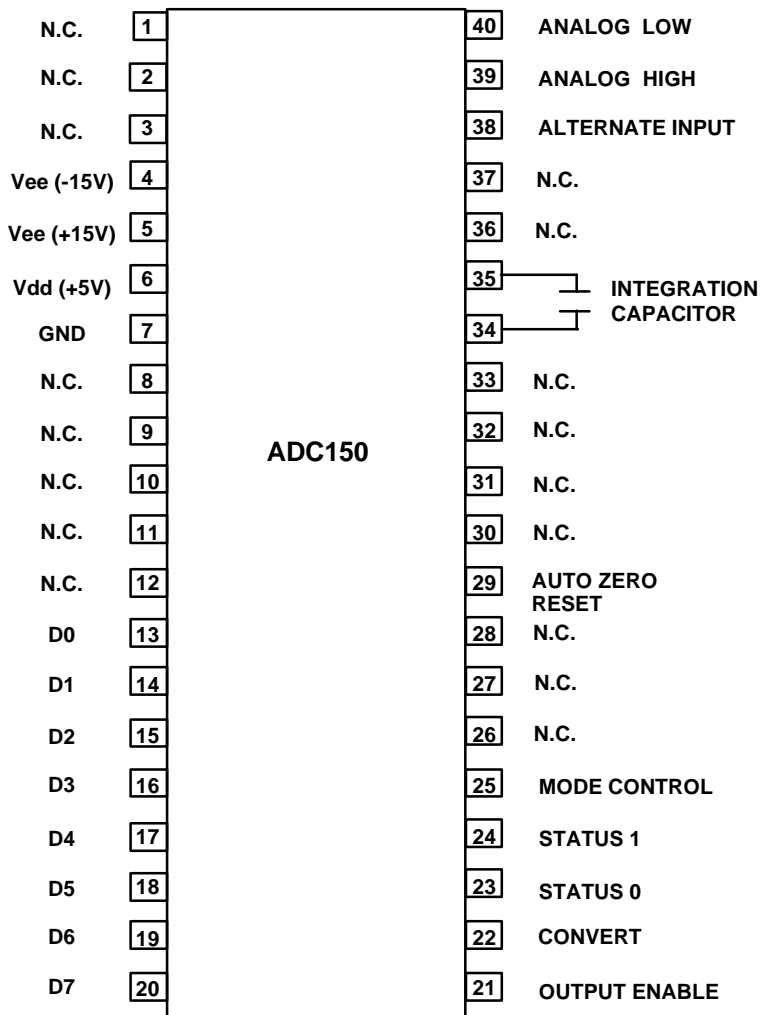
MAXIMUM RATING SPECIFICATIONS

ADC150

MODEL	ADC150		
PARAMETER	MIN	MAX	UNITS
TEMPERATURE			
Operating	-55	125	°C
Storage	0	160	°C
POWER SUPPLY			
V_{CC}	+14	+16	VDC
V_{EE}	-14	-16	VDC
V_{DD}	+4	+6	VDC
INPUTS			
Analog Inputs	V_{EE}	V_{CC}	
Digital Inputs	0	V_{DD}	

EXTERNAL CONNECTIONS

(TOP VIEW)



NOTES:

1. Power Supply Decoupling

The ADC150 has internal 0.1µF decoupling capacitors for all power supply inputs. The internal decoupling capacitors are adequate for applications with relatively short power supply leads (approx. 5") or if additional capacitors are located on a circuit board. For applications with long power supply leads an external capacitor of 10 µF on the +/- 15V inputs and 33 µF on the +5V input is recommended.

2. Ground

The ground connection (pin 7) should be made as solid as possible since ground noise can result in a loss of accuracy. Use of a ground plane is a good approach to maintain the full accuracy of the ADC150.

3. External Components

A .68 µF polystyrene integration capacitor must be connected to pins 34 and 35 with a lead length not exceeding 2".

4. Analog Inputs

In order to avoid differential noise pickup it is recommended to use parallel adjacent lines for the analog inputs (pins 39, 40) on PC boards and shielded lines outside of the PC connections.

ELECTRICAL SPECIFICATIONS

ADC150

(Vps = +/- 15V, +5V, T = 25 Deg. C.)

MODEL	ADC150C			ADC150CA			ADC150M			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY										
Resolution	18		24			*			*	Bits
Input Equivalent Noise		1			*			*		μV
Offset without Auto Zero			4						*	ppm
Offset with Auto Zero			1			0.5			*	ppm
Full Scale			100			50			*	ppm
Noise (.1-10Hz) @ 10V		6			*			*		μVpp
Nonlinearity		1	2		*	*		*	*	ppm
Normal Mode Rejection ¹	60			*			*			dB
TEMPERATURE STABILITY										
Offset			0.2			0.1			*	ppm/°C
Full Scale			1.0			0.5			*	ppm/°C
TIME STABILITY										
Offset		.1			*			*		ppm/month
Full Scale ²		2			*			*		ppm/24 hrs.
ERROR ALL SOURCES										
24 hrs, +/- 1 Deg. C Amb.			.0005, 2			.0003, 2			*	%, +/- Counts
90 days, +/- 5 Deg. C Amb.			.0010, 2			.0008, 2			*	%, +/- Counts
1 year, +/- 5 Deg. C Amb.			.0015, 2			.0013, 2			*	%, +/- Counts
CONVERSION TIME										
			1067			*			*	ms
WARM-UP TIME										
			5			*			*	minutes
POWER SUPPLY REJECTION										
+/- 15 VDC	80			*			*			dB
5 VDC	80			*			*			dB
ANALOG INPUT CHARACTERISTICS										
Input Range	-10.485760		10.485755	*		*	*		*	V
Bias Current		1.2	3		*			*		nA
Input Impedance		200			*			*		GΩ
POWER SUPPLY VOLTAGES										
+15 V	14.5	15	15.5	*	*	*	*	*	*	V
-15 V	14.5	15	15.5	*	*	*	*	*	*	V
5 v	4.5	5	5.5	*	*	*	*	*	*	V
POWER SUPPLY CURRENTS										
+15 V		23			*			*		mA
-15 V		24			*			*		mA
5 v		42			*			*		mA
DIGITAL INPUTS										
Low			0.8			*			*	V
High	4.0			*			*			V
DIGITAL OUTPUTS										
Low			0.8			*			*	V
High	4.0			*			*			V
AUTO ZERO INPUT										
Low			0.8			*			*	V
High	4.0			*			*			V
CONVERT INPUT										
Low			0.8			*			*	V
High	4.0			*			*			V
TEMPERATURE RANGE										
	-25		85	*		*	-55		125	°C

* Same as ADC150C

Note: 1) 60 Cycle

2) (Max-Min Value) - Noise(.1-10Hz)

THEORY OF OPERATION

In the ADC150 block diagram (see Figure 1), V_{hi} and V_{low} are the inputs. Both are buffered and fed into a differential, voltage controlled, single output current source. This current is added to the reference current at the input of the op amp integrator. The output of the integrator is fed into a Schmitt trigger, which in turn, is fed into the ADC's timing control circuitry. When the integrator output actuates the Schmitt trigger, the timing circuit changes the direction of the reference current source and the integrator begins integrating in the opposite direction. This continues until the Schmitt trigger is actuated again by the integrator and reverses the direction of the reference current.

The equation for integration times are:

$$T_p = \frac{V \times C}{I_{ref} + I_{inp}} \quad T_m = \frac{V \times C}{-I_{ref} + I_{inp}}$$

V = Voltage

C = Integration Capacitor Value

I_{ref} = Reference Current

I_{inp} = Input Current

Resolving these equations produces:

$$I_{inp} = I_{ref} \frac{T_p - T_m}{T_p + T_m}$$

T_p = Time Positive

T_m = Time Negative

The timing control circuitry governs the counters that measure the integration time in both directions.

The ADC150's on-board microprocessor is used to calculate the results of the integration equation and perform error corrections. Note that the μP automatically performs an auto zero function at start-up, but it is recommended to achieve maximum accuracy, that an auto zero be performed again after the ADC150 is fully warmed up.

When the μP detects a convert signal, it lowers the status lines to indicate that the ADC is involved in a conversion. When it detects a change in slope direction, the μP will collect the counts for the integration time. When sufficient counts have been collected, the μP performs the calculations described above.

When the calculations are complete, the μP places the most significant byte in the output buffer and raises the S_0 flag. When another pulse is placed on the convert line, the middle byte is placed on the output, the S_0 flag is lowered and the S_1 flag raised. When the last pulse is placed in the convert line, the least significant byte is placed in the output buffer and both status flags are high indicating that the ADC150 is ready for another conversion.

Status line summary:

S_1	S_0	
0	0	Conversion in progress.
0	1	Conversion complete. MSB in output.
1	0	Middle byte in output register.
1	1	LSB in output. Ready for next conversion.

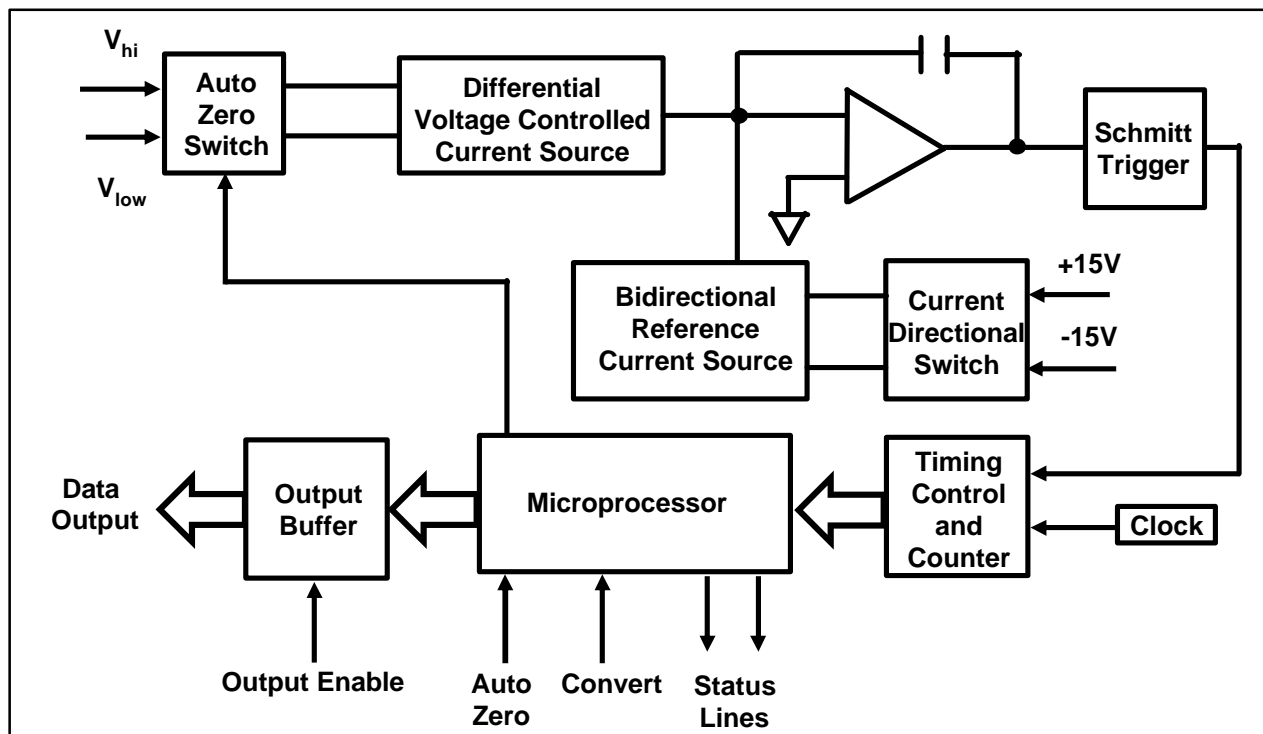


FIGURE 1. BLOCK DIAGRAM

CONNECTING THE ADC150

POWER SUPPLIES

The power supply lines are connected to pins 4-7. Pin 4 is -15V, pin 5 is +15V, pin 6 is +5V and pin 7 is GND.

OUTPUT DATA LINES

The output data is available in byte form on pins 13-20. Pin 20 is the Most Significant Bit and pin 13 the Least Significant Bit. The data lines go to a high impedance state when the Output Enable line is at a logic one level.

OUTPUT ENABLE (PIN 21)

Data is placed on the Output Data Lines by a logic zero on this line. See figure 2 for data output format.

CONVERT (Pin22)

This line is used to initiate a conversion cycle and to retrieve the output data. The status lines indicate which function will be executed. The first pulse (transition from logic one to logic zero) starts the conversion cycle. Two subsequent pulses are used to place the lower two bytes on the Output Data Lines. See figure 4 for timing diagram.

STATUS LINES (Pins 23, 24)

These lines indicate the present state of the ADC. When the Convert line receives the first pulse in a conversion cycle the Status Lines go to logic zero, indicating that a conversion cycle is in progress. When the conversion is complete the microprocessor places the MSB of the output data in the output buffer and then raises S_0 to a logic one, indicating that the MSB at the output data is available in the output buffer. When the Convert Line is pulsed again the middle byte of the output data is placed in that output buffer and S_1 changes to logic one and S_0 to logic zero. The third pulse places the LSB of the output data in the buffer and both status lines go to the logic one. The converter is now ready for the next conversion cycle. See figure 5 for timing diagrams.

The table below shows a summary of the status code.

S_1	S_0	
0	0	Conversion in process.
0	1	Conversion complete. MSB in output.
1	0	Middle byte in output register.
1	1	LSB in output. Ready for next conversion.

MODE CONTROL (Pin 25)

This line is used to program the ADC150. The mode control byte (8 bit) is placed on the data bus. Pin 25 is then set to logic high, pin 21 is pulsed low to accept the control byte. Pin 22 is then pulsed low and held low until the status lines return high (~2ms). Pin 21 is then pulsed high and pin 25 is then returned to logic low. The ADC150 has now been reset to the new parameters. See figure 6 for timing diagrams.

The mode control byte is defined as follows:

Bits 7 and 6	- unused
Bits 5 and 4	- 00 Pin 39 signal input, autozero*
	01 Pin 38 signal input
Bit 3	- 0 60 Hz.*
	1 50 Hz.
Bits 2,1,0	- 001 18 Bit
	010 20 Bit
	011 22 Bit*
	100 24 Bit

* Factory default settings

AUTO-ZERO / RESET (Pin 29)

A logic zero on this input will autozero the ADC150 by internally connecting the analog high to analog low. Since the μP is reset, the ADC150 reverts to the factory default settings in the EPROM (ie. 22bits, 60Hz, pin 39 analog high). To select a mode different than the default settings, the mode control must be set after auto zero. See figure 3 for timing diagrams.

INTEGRATION CAPACITOR (Pin 34, 35)

A 0.68 μF polystyrene or Mylar must be connected to these pins. Lead length should be as short as possible and not exceed 2".

ANALOG INPUTS (Pin 39, 40)

Both analog inputs are buffered by op-amps and have a common mode rejection of approximately 80dB minimum. To maintain the full accuracy at the ADC it is recommended to keep the input to analog low to less than 0.1VDC.

OUTPUT DATA REPRESENTATION

The output data is represented in BOB (Bipolar Offset Binary) format. The table below shows the output data codes for zero and plus-minus full scale input voltage for the programmable resolution of the converter.

24 Bits
1 LSB = 1.24 μ V

Input Voltage	Output Data		
	High Byte	Middle Byte	Low Byte
-10.485760 V	00	00	00
0.0 V	80	00	00
+10.485755 V	FF	FF	FF

22 Bits
1 LSB = 5 μ V

Input Voltage	Output Data		
	High Byte	Middle Byte	Low Byte
-10.485760 V	00	00	00
0.0 V	20	00	00
+10.485755 V	3F	FF	FF

20 Bits
1 LSB = 20 μ V

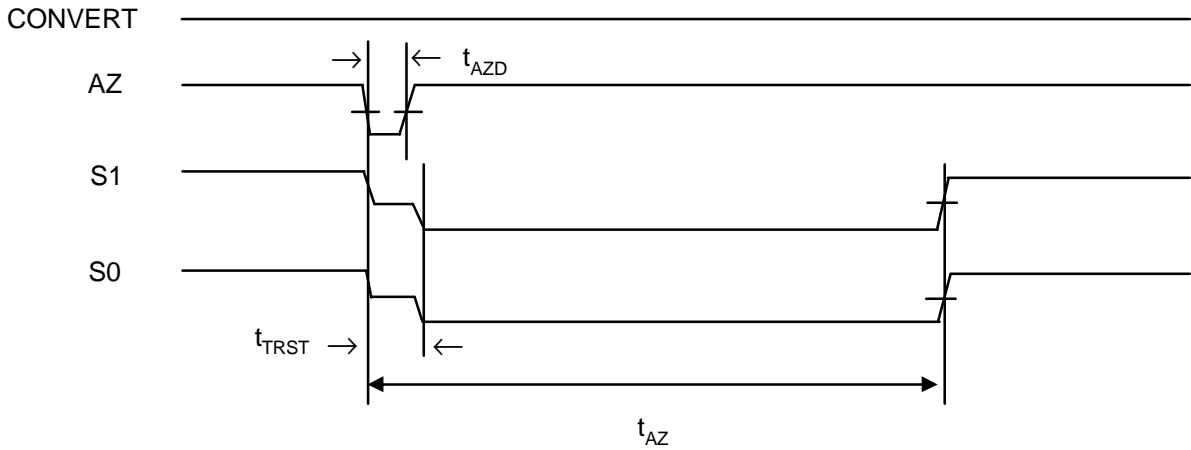
Input Voltage	Output Data		
	High Byte	Middle Byte	Low Byte
-10.485760 V	00	00	00
0.0 V	08	00	00
+10.485755 V	10	FF	FF

18 Bits
1 LSB = 80 μ V

Input Voltage	Output Data		
	High Byte	Middle Byte	Low Byte
-10.485760 V	00	00	00
0.0 V	02	00	00
+10.485755 V	04	FF	FF

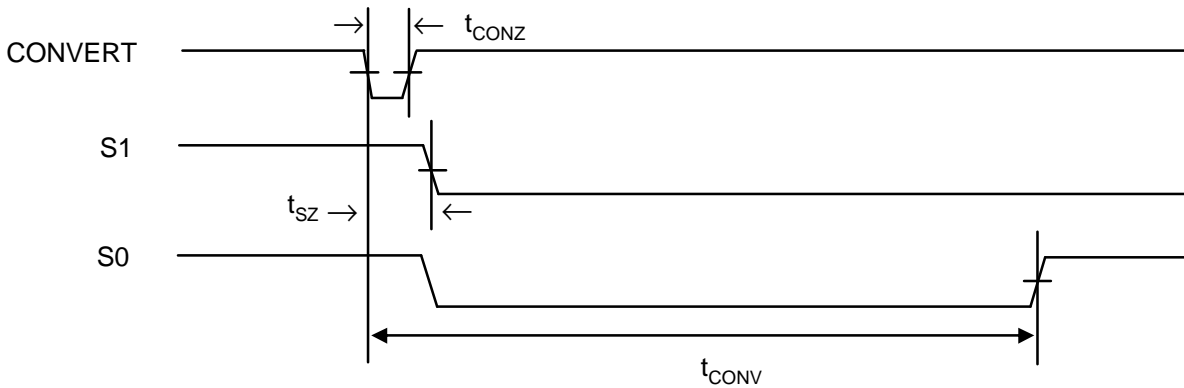
FIGURE 2

TIMING DIAGRAMS



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AZD}	AZ Pulse Width	0.2			μs
t_{TRST}	Tristate Time			30	ms
t_{AZ}	AZ Time			400	ms

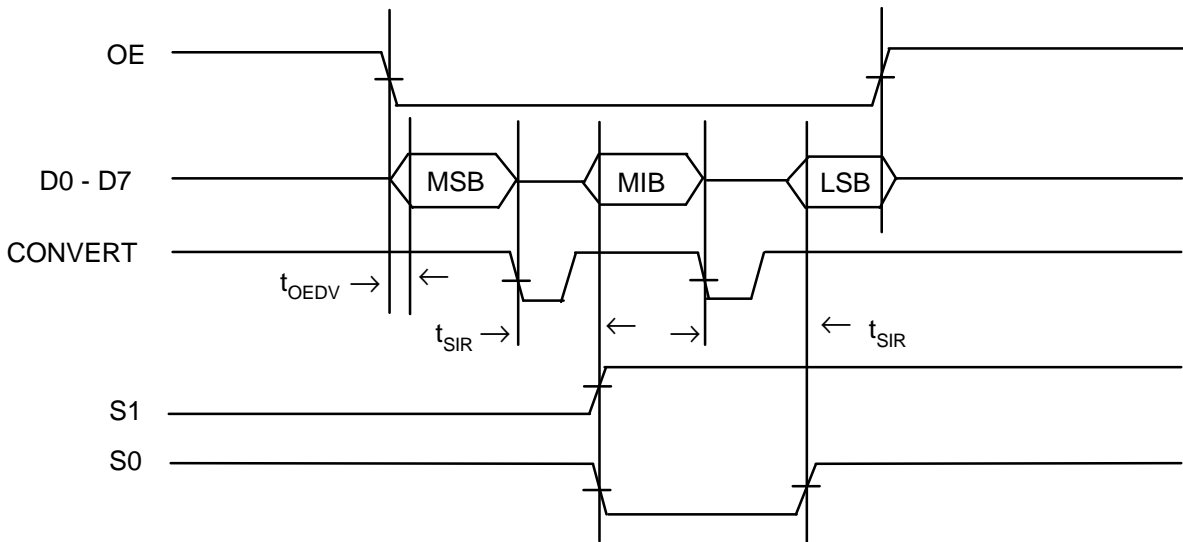
FIGURE 3. AUTO ZERO



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CONZ}	Convert Pulse	5.0			μs
t_{SZ}	Status Delay			8.0	μs
t_{CONV}	Convert Time			320	ms

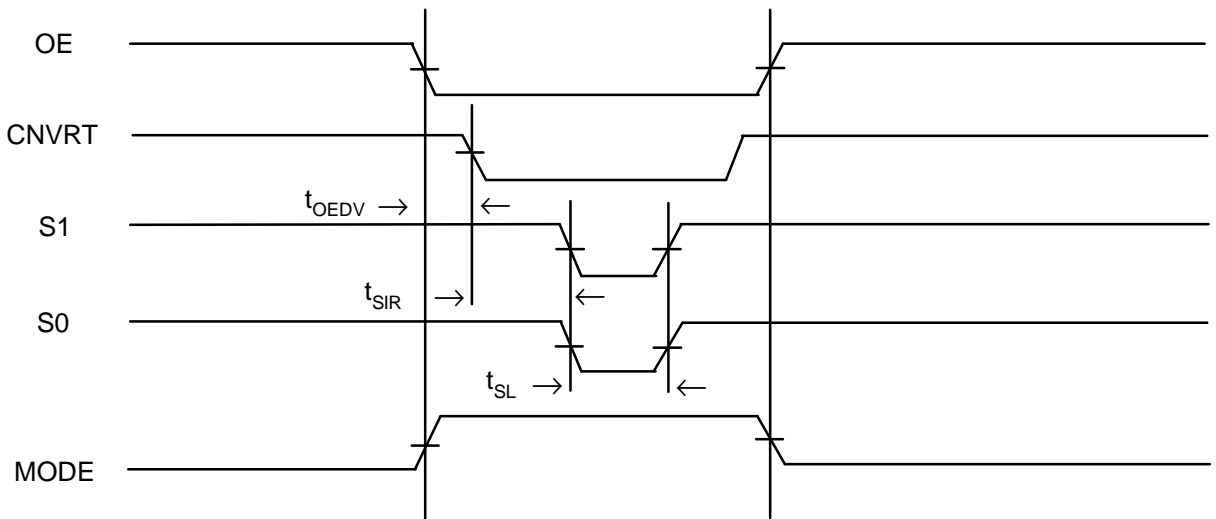
FIGURE 4. CONVERSION (22 Bits)

TIMING DIAGRAMS



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{OEDV}	OE Delay		45		ns
t_{SIR}	Status Delay		3.0		μ s

FIGURE 5. DATA OUTPUT



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SIR}	Status Delay		8.0		μ s
t_{SL}	Status Low			100	ms
t_{OEDV}	OE Delay		45		ns

FIGURE 6. MODE CHANGE

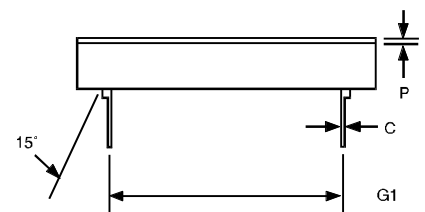
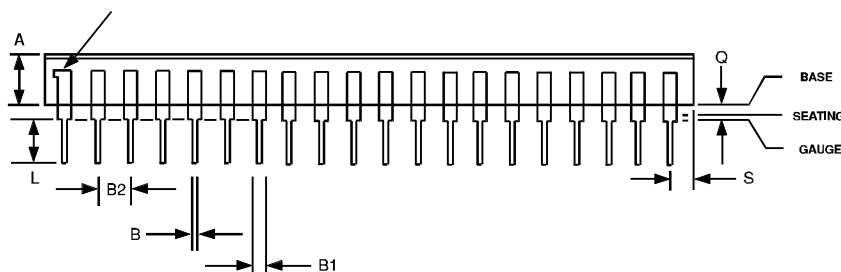
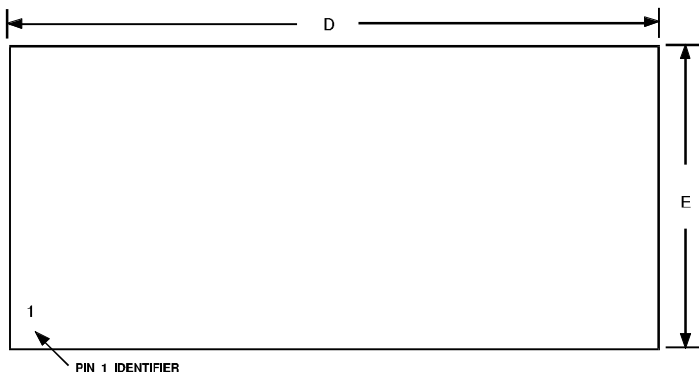
RESOLUTION	LINE CYCLES	CONV. / SEC (60/50 Hz)
18 BITS	1	60 / 50
20 BITS	4	15 / 12
22 BITS	16	3.7 / 3.1
24 BITS	64	1.2 / .93

Line Cycle at 60 Hz = 16.667 ms; 50 Hz = 20 ms

FIGURE 7. INTEGRATION TIMES

40-PIN HYBRID PACKAGE

DIM	INCHES	
	MIN	MAX
E	1.080	1.100
D	2.075	2.115
A	0.155	0.185
L	0.220	0.240
B2	.100 typ	
B	.018 typ	
Q	.015	.035
C	.009	.012
P	.012	.018
G1	.890	.910
B1	.040 typ	



NOTES:
 1. GOLD PLATING 60 MICRO INCHES MINIMUM THICKNESS OVER 100 MICRO INCHES NOMINAL THICKNESS OF NICKEL

FIGURE 8. MECHANICAL SPECIFICATIONS