ADC180
Programmable
Integrating A/D Converter

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FEATURES

- 26 BIT RESOLUTION
- UP TO 2.5kHz CONVERSION RATES
- AUTO ZERO FUNCTION
- ±10.48 V INPUT RANGE
- 0.5ppm/°C MAX. SCALE FACTOR ERROR AND 2 ppm MAX. LINEARITY ERROR (-55°C to +125°C).
- 8 BIT PARALLEL DATA BUS
- INTERNAL CRYSTAL CLOCK and PRECISION REFERENCE
- LOW POWER CONSUMPTION: 0.4 WATTS

APPLICATIONS

- INERTIAL GUIDANCE
- TEST EQUIPMENT
- DATA ACQUISITION
- SCIENTIFIC INSTRUMENTS
- MEDICAL INSTRUMENTS
- WEIGHT SCALES

DESCRIPTION

The ADC180 is a 26 bit, charge balanced A/D converter. Continuous sampling of 20 MHz and conversion rates of up to 2.5 kHz make the converter ideal for low frequency signal measurement. The integration time is user selectable through an external capacitor.

The ADC180 will continuously collect and average integrations until the user requests data. Converter resolution is dependent on the number of integration cycles completed before the data is requested. Converter resolution ranges from 13 - 26 bits.

In order to retain accuracy, internal calculations are made at a 32 bit level. The output of the result is also made at the 32 bit level. This makes it possible to use a relatively high conversion rate and average the data external to the converter without loss of accuracy due to computation roundoff errors. For inertial guidance systems, velocity information can be obtained at a high rate without loss of position accuracy.

The use of hybrid technology allows for separation of sensitive analog circuitry from digital circuit noise. This produces far superior accuracy over monolithic A/D convertors.

The converter uses a proprietary, patented charge balance modulator. It has an internal crystal clock, microcontroller, precision reference, and patented nonlinear temperature compensation network which provides excellent electrical performance over temperature.

The maximum scale factor drift is 0.5ppm/ºC, maximum offset drift of 0.1ppm/ºC, and a maximum nonlinearity over the mil. temp. range of 2 ppm.

The ADC180 is packaged in a 40 pin hermetic TDIP and requires ±15V and +5V supplies. The converter dissipates 450 mW and is available in commercial and military grades.

ELECTRICAL SPECIFICATIONS (Vcc = +15V, Vee = -15V, Vdd = + 5V, TA = +25ºC) ADC180

MODEL	ADC180C			ADC180CA			ADC180M			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
ACCURACY										
Resolution	13		26	*		*	*		*	bits
Input Equivalent Noise		.25			*			*		µV
Offset without Auto Zero			4			2			*	ppm FS
Offset with Auto Zero			1			0.5			*	ppm FS
Scale Factor Error			100			50			*	ppm FS
Noise (.1-10Hz) @ 10V		6			*			*		µVpp
Nonlinearity		1	2		*	*		*	*	ppm FS
Normal Mode Rejection (1)	60			*			*			dB
Common Mode Rejection	80			*			*			dB
TEMPERATURE STABILITY										
Offset			0.2			0.1			*	ppm/º C
Full Scale			1.0			0.5			*	ppm/º C
TIME STABILITY										
Offset		0.1			*			*		ppm/month
Full Scale (2)		2			*			*		ppm/24 hrs.
ERROR ALL SOURCES										
24 hrs, +/- 1 Deg. C Amb.			.0005, 2			.0003, 2			*	%, +/- counts
90 days, +/- 5 Deg. C Amb.			.0010, 2			.0008, 2			*	%, +/- counts
1 year, +/- 5 Deg. C Amb.			.0015, 2			.0013, 2			*	%, +/- counts
CONVERSION TIME	0.250		3200	*		*	*		*	ms
WARM-UP TIME			5			*			*	minutes
POWER SUPPLY REJECTION										
+Vcc, -Vee	80			*			*			dB
5 VDC	80			*			*			dB
ANALOG INPUT CHARACTERISTICS										
Input Range	-10.485760		+10.485755	*		*	*		*	V
Bias Current		1.2	3		*			*		nA
Input Impedance		200			*			*		GO
Max. Input Voltage	-Vee		+Vcc	*		*	*		*	V
POWER SUPPLY VOLTAGES										
+Vcc	+14.5	+15	+15.5	*	*	*	*	*	*	V
-Vee	-14.5	-15	-15.5	*	*	*	*	*	*	V
+Vdd	+4.5	+5	+5.5	*	*	*	*	*	*	V
POWER SUPPLY CURRENTS										
+Vcc		23			*			*		mA
-Vee		24			*			*		mA
+Vdd		42			*			*		mA
DIGITAL INPUTS										
Low			0.8			*			*	V
High	4.0			*			*			V
DIGITAL OUTPUTS										
Low			0.8			*			*	V
High	4.0			*			*			V
TEMPERATURE RANGE	-25		85	*		*	-55		125	ºC

* Same as ADC180C

Notes: 1) 60 Cycle 2) (Max-Min Value) - Noise(0.1-10Hz)

THEORY OF OPERATION

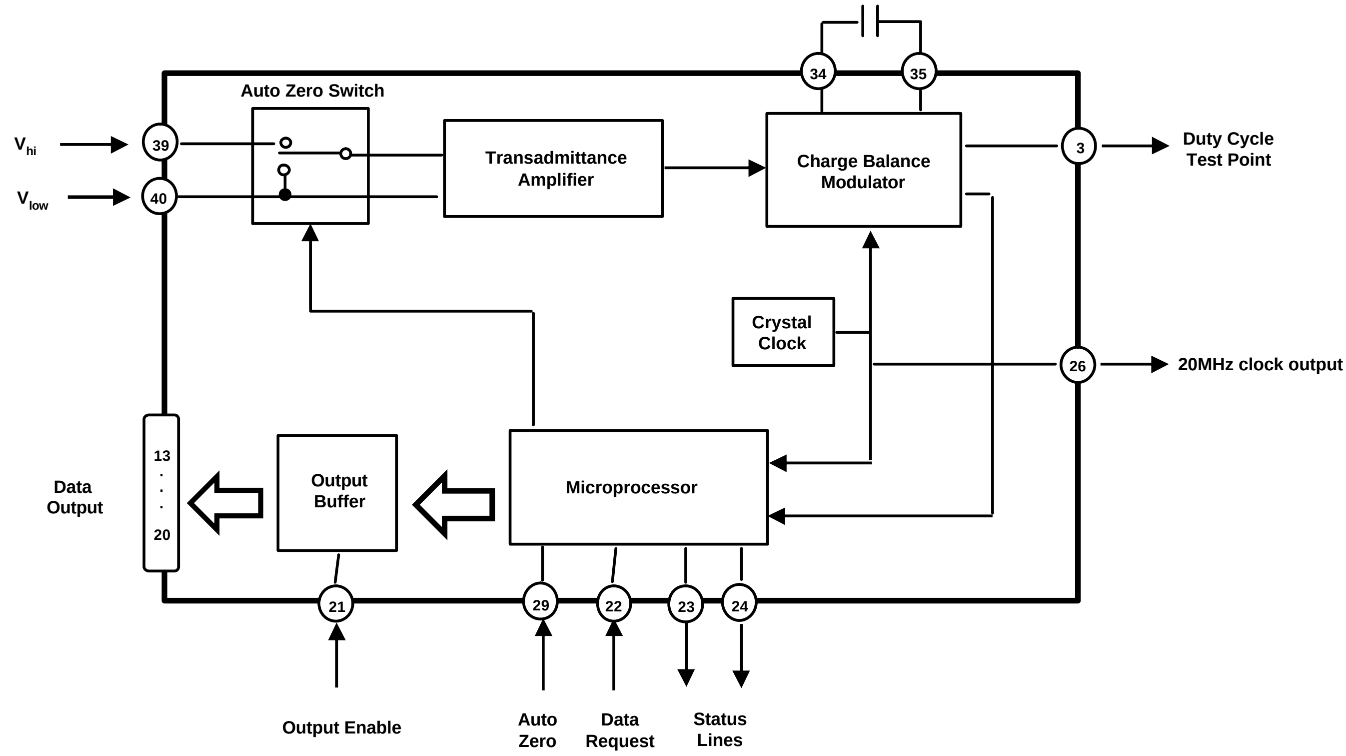

FIGURE 1. BLOCK DIAGRAM

The ADC180 uses a differential input to improve accuracy. To measure single source voltages, V_{low} should be connected to the ground point of the source voltage to be measured. In figure 1, the switch is shown in the normal operating mode connecting V_{hi} and V_{low} to the differential input of the transadmittance amplifier. For an autozero cycle, V_{hi} is disconnected and the input to the amplifier is shorted.

The charge balance modulator (figure 2) uses a proprietary patented architecture to achieve the high accuracy of the ADC180 without any error correction method other than autozero. This enables the converter to sample the output of the transadmittance amplifier continuously at a sampling rate of 20 MHz. This is important for applications like inertial guidance systems where

$$\int_{t1}^{t2} V_{inp} \cdot dt$$

must be measured without any loss of time increments. The output of the charge balance modulator is in the form of a pulse width modulation signal. The internal microprocessor provides all control functions and digital signal processing.

The converter also has an internal crystal clock to avoid phase jitter errors and a tristate output buffer for easy interface with bus based systems. For the data output timing see figures 5 and 6.

The conversion result between two consecutive data request inputs at times t_1 and t_2 is mathematically represented by the equation

$$V_{iav} = \frac{1}{t_2 - t_1} \int_{t1}^{t2} V_{inp} \cdot dt$$

The converter provides two 32 bit data words with the first word containing t_2-t_1 and the second word containing

$$\int_{t1}^{t2} V_{inp} \cdot dt$$

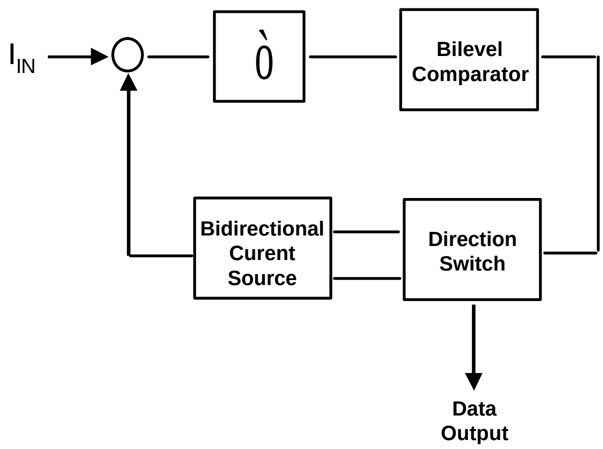

Figure 2. Patented Charge Balance Modulator

CONNECTING THE ADC180

DUTY CYCLE OUTPUT (pin 3)
This logic level output allows monitoring of the integration cycle and is usually used for timing purposes.

POWER SUPPLIES (pins 4-7)
The ADC180 has internal 0.1µF decoupling capacitors for all power supply inputs. This is sufficient for applications with relatively short power supply leads (approx. 5") or if additional capacitors are located on the circuit board. External capacitors of 10 µF on the ±15V inputs and 33 µF on the +5V input is recommended for applications with longer power supply leads.

GROUND (pin7)
Since ground noise can result in a loss of accuracy, the ground connection should be made as solid as possible. Use of a ground plane is a good approach to maintain the full accuracy of the ADC180.

OUTPUT DATA LINES (pins 13-20)
The parallel output data is available on pins 13-20. Pin 20 is the Most Significant Bit and pin 13 the Least Significant Bit. The data lines go to a high impedance state when the Output Enable line is at a logic 1 level.

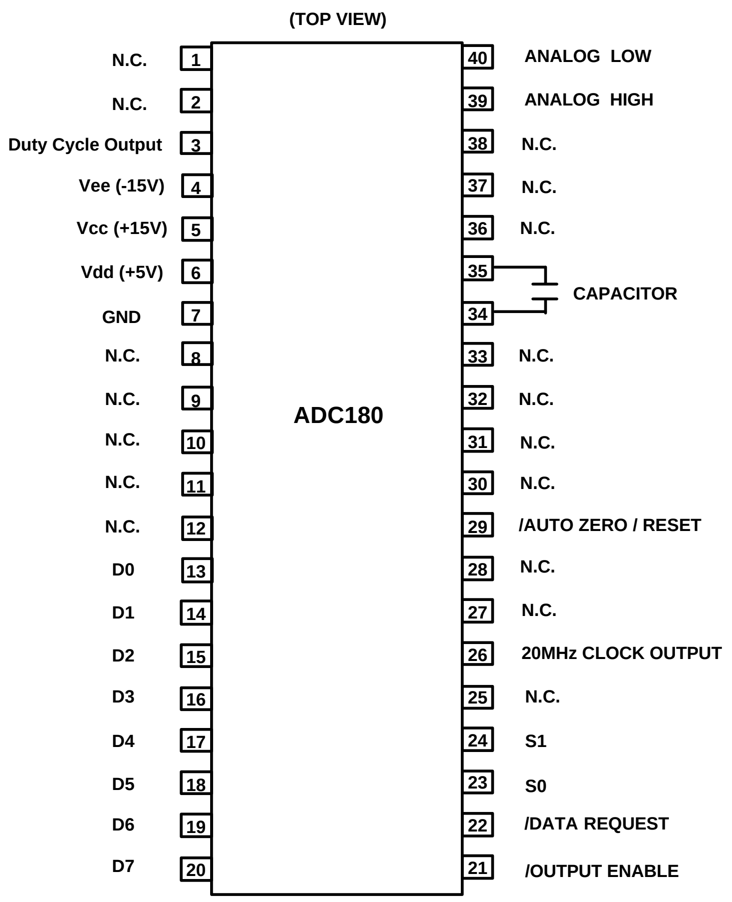

FIGURE 3. EXTERNAL CONNECTIONS

ANALOG INPUTS (pins 39,40)
The differential analog inputs are buffered by op amps and have a common mode rejection of approximately 80dB minimum. To maintain the full accuracy of the ADC180 it is recommended to maintain the input to analog low to less than 0.1VDC. To avoid differential noise pickup, parallel adjacent lines should be used for the analog inputs on PC boards and shielded lines outside of the PC connections.

CAPACITOR (pin 34, 35)
The only external component required to operate the ADC180 is a capacitor which sets the integration time. A 0.082 µF capacitor results in an integration time of approximately 250 µs. For 2,000 µs a 0.68µF capacitor is required. The relationship is linear for intermediate capacitor values.
The main parameter affected by shorter conversion times is bias stability over temperature. Polystyrene, mylar, or polycarbonate capacitors are recommended.

AUTO ZERO / RESET (pin 29)
A logic 0 on this input will autozero the ADC180 by internally connecting the analog high to analog low. Since the internal microprocessor is reset, the ADC180 is not functional during this time (approximately 1s). S_1 will go to logic 1 indicating that no data is available. After completing the autozero function, S_1 will return to logic 0 and the ADC will begin collecting data.

20MHz CLOCK OUTPUT (pin 26)
Output of the internal crystal oscillator.

STATUS LINES (pins 23, 24)
These lines indicate the present state of the ADC. After a data request has been received and the current integration cycle is complete, the ADC will output the data collected subsequent to the previous data request. S_1 will go to logic 1 to acknowledge the data request. The 8 bytes of data will be placed on the data bus sequentially. A logic 1 on S_0 indicates valid data on the data bus. After the data has been transmitted, S_1 will return to logic 0.

DATA REQUEST (pin 22)
A logic 0 on this line initiates a data transfer sequence.

OUTPUT ENABLE (pin 21)
A logic 0 on this line enables outputs D0 - D7.

NC= Factory test points, do not connect to these pins.

TIMING DIAGRAMS

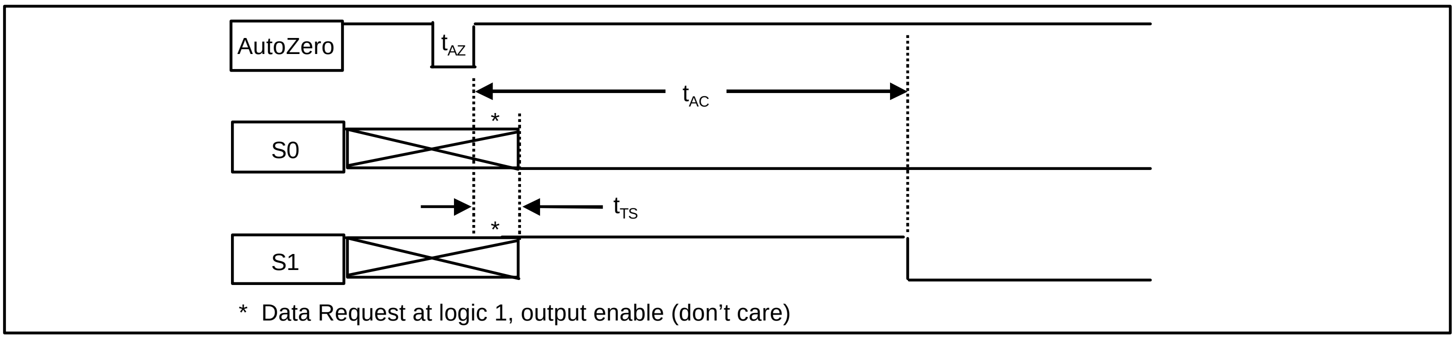

FIGURE 4. AUTO ZERO TIMING

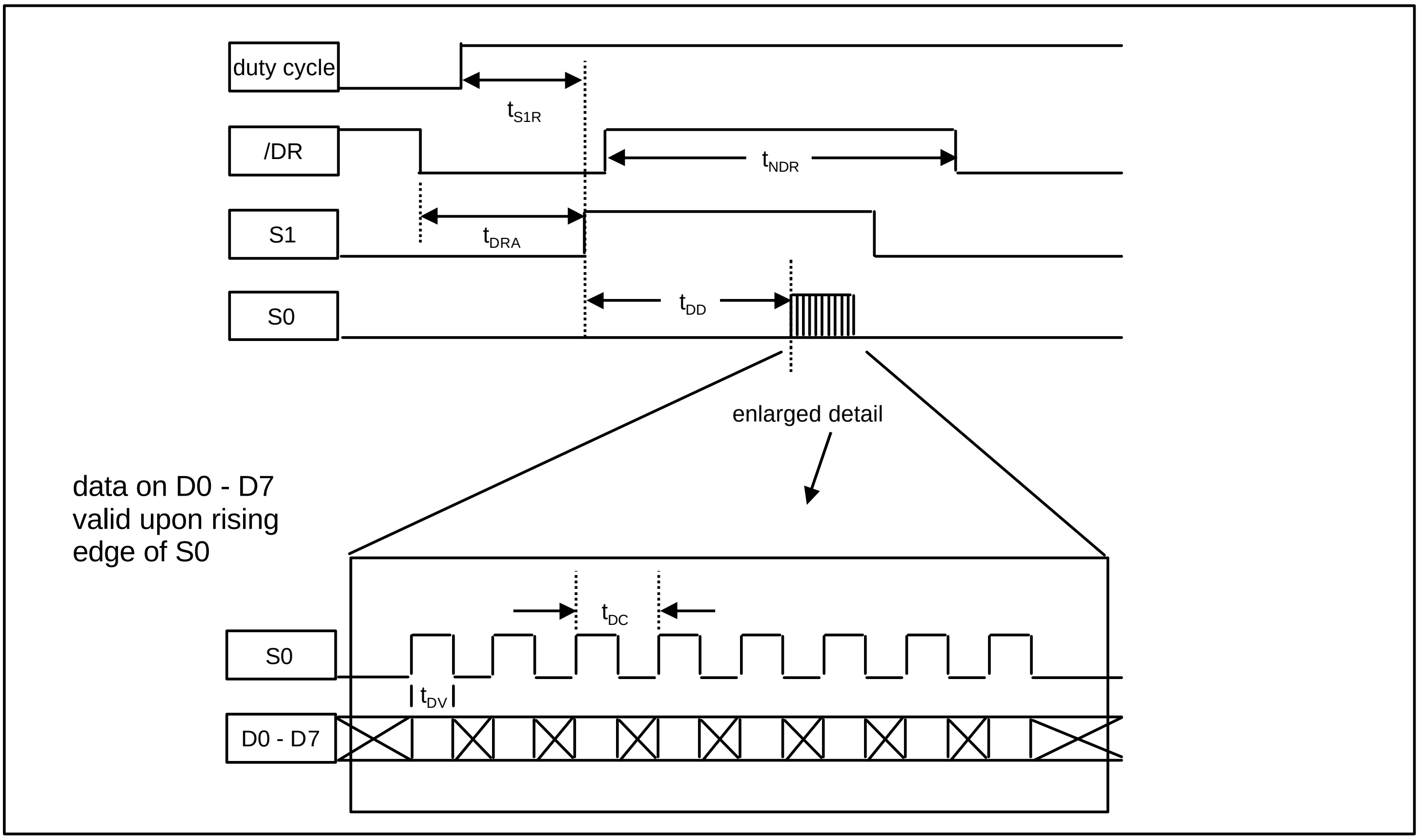

FIGURE 5. DATA REQUEST CYCLE TIMING

SIGNAL	SYMBOL	MIN	TYP	MAX	UNITS
AutoZero request	t_{AZ}	100			ns
Autozero Cycle	t_{AC}			1.3	s
port TriState time	t_{TS}		30		ms
Data Request Acknowledge	t_{DRA}	*		*	
S1 Response after duty cycle	t_{S1R}	27		34	µs
Data Delay	t_{DD}		50		µs
time before Next Data Request	t_{NDR}	0			µs
Data Valid	t_{DV}		1		µs
Data Cycle	t_{DC}		2		µs

* T_{DRA} must be either 1 integration cycle minimum or until S1 goes high.

FIGURE 6. TIMING TABLE

SPECIFICATIONS

MAXIMUM RATINGS

ADC180

MODEL	ADC180		
PARAMETER	MIN	MAX	UNITS
TEMPERATURE			
Operating	-55	125	° C
Storage	0	150	° C
POWER SUPPLY			
Vcc	+14	+16	VDC
Vee	-14	-16	VDC
Vdd	+4	+6	VDC
INPUTS			
analog inputs	Vee	Vcc	
digital inputs	0	Vdd	

RESOLUTION (bits)	LSB weighting (µV)	Sampling Time (ms) approx.	Conversions Per Second	cycles w/0.082µF capacitor	cycles w/ 0.68µF capacitor
26	0.31	3200	0.31	12800	1600
25	0.62	1600	0.62	6400	800
24	1.25	800	1.25	3200	400
23	2.5	400	2.5	1600	200
22	5	200	5	800	100
21	10	100	10	400	50
20	20	50	20	200	25
19	40	25	40	100	13
18	80	12.5	80	50	6
17	160	6.25	160	25	3
16	320	3.12	320	13	1
15	640	1.56	640	6	-
14	1280	0.78	1280	3	-
13	2560	0.39	2560	1	-

Note: 0.082µF external capacitor provides ~250µs integration cycle
0.68µF external capacitor provides ~2000µs integration cycle

FIGURE 7 APPROXIMATE SAMPLING TIME VS. RESOLUTION

input voltage	output	output (hex)
+10.485775 V	2^28	10 00 00 00
0 V	(2^28)/2	08 00 00 00
-10.485760 V	0	00 00 00 00

FIGURE 8 OUTPUT DATA REPRESENTATION

```
outputword1 = (byte1 * 2^24) + (byte2 * 2^16) + (byte3 * 2^8) + byte4

outputword2 = ((byte5 - 8) * 2^24) + (byte6 * 2^16) + (byte7 * 2^8) + byte8
                          scales to 0V

Vout = (outputword2 / outputword1) * 20
                                      scales to ±10V
```

FIGURE 9 OUTPUT CALCULATION PSEUDO-CODE

40-PIN HYBRID PACKAGE

	INCHES	
DIM	MIN	MAX
E	1.080	1.100
D	2.075	2.115
A	0.155	0.185
L	0.220	0.240
B2	.100 typ	
B	.018 typ	
Q	.015	.035
C	.009	.012
P	.012	.018
G1	.890	.910
B1	.040 typ	

NOTES:
1. GOLD PLATING 60 MICRO INCHES MINIMUM THICKNESS OVER 100 MICRO INCHES NOMINAL THICKNESS OF NICKEL

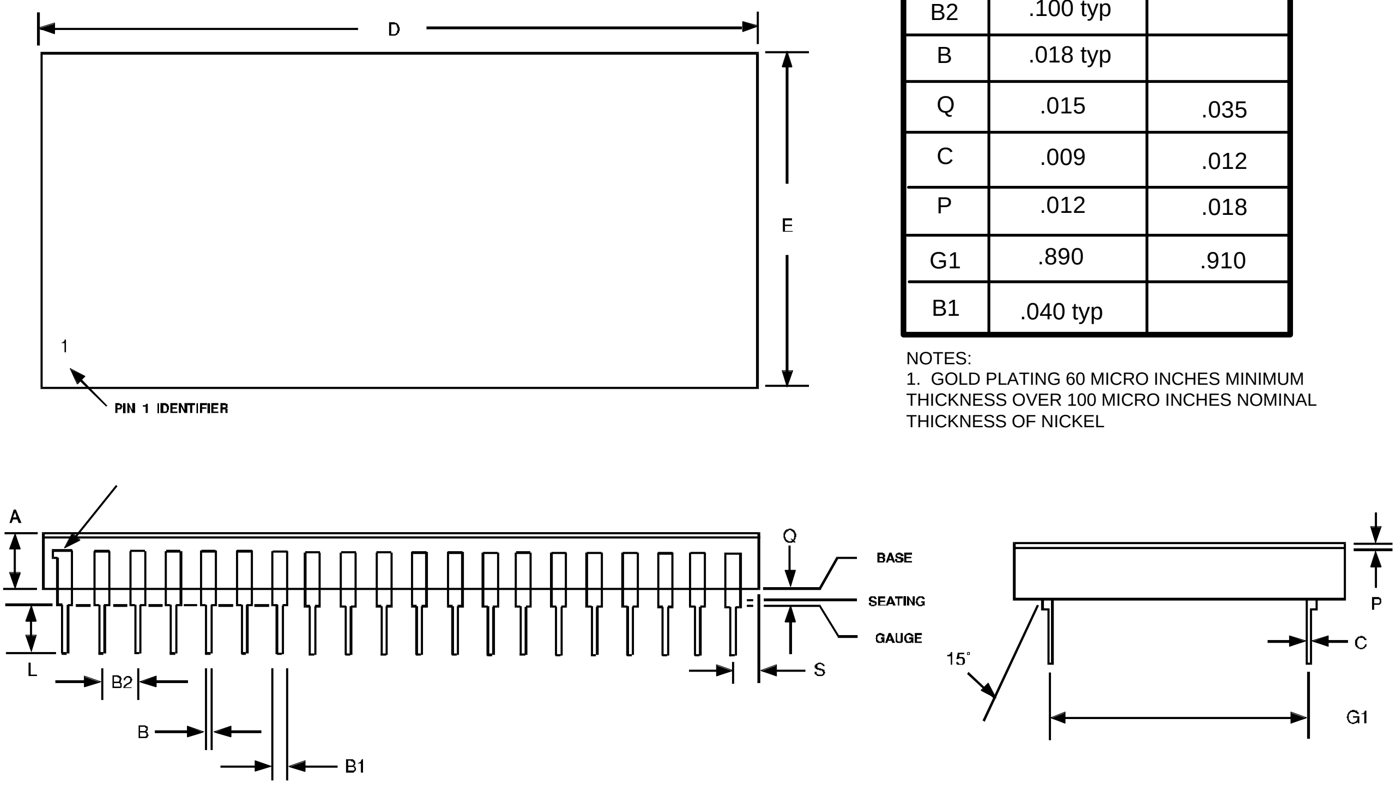

FIGURE 10 MECHANICAL SPECIFICATIONS