

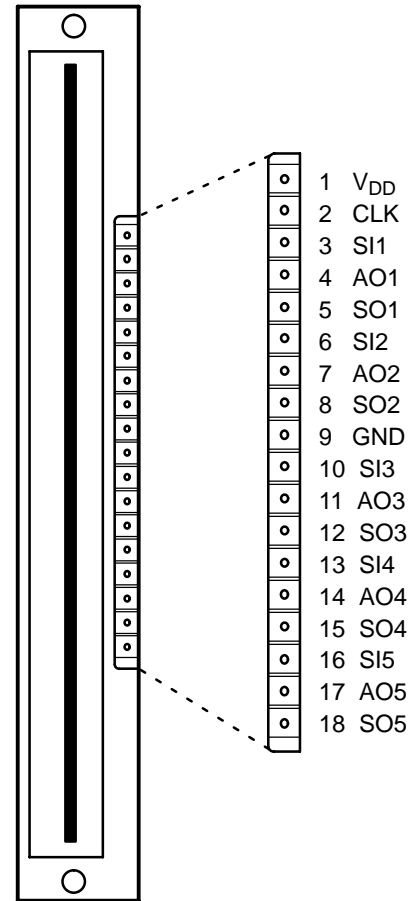
- **640 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 2000:1 (66 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 5 MHz**
- **Single 5-V Supply**

Description

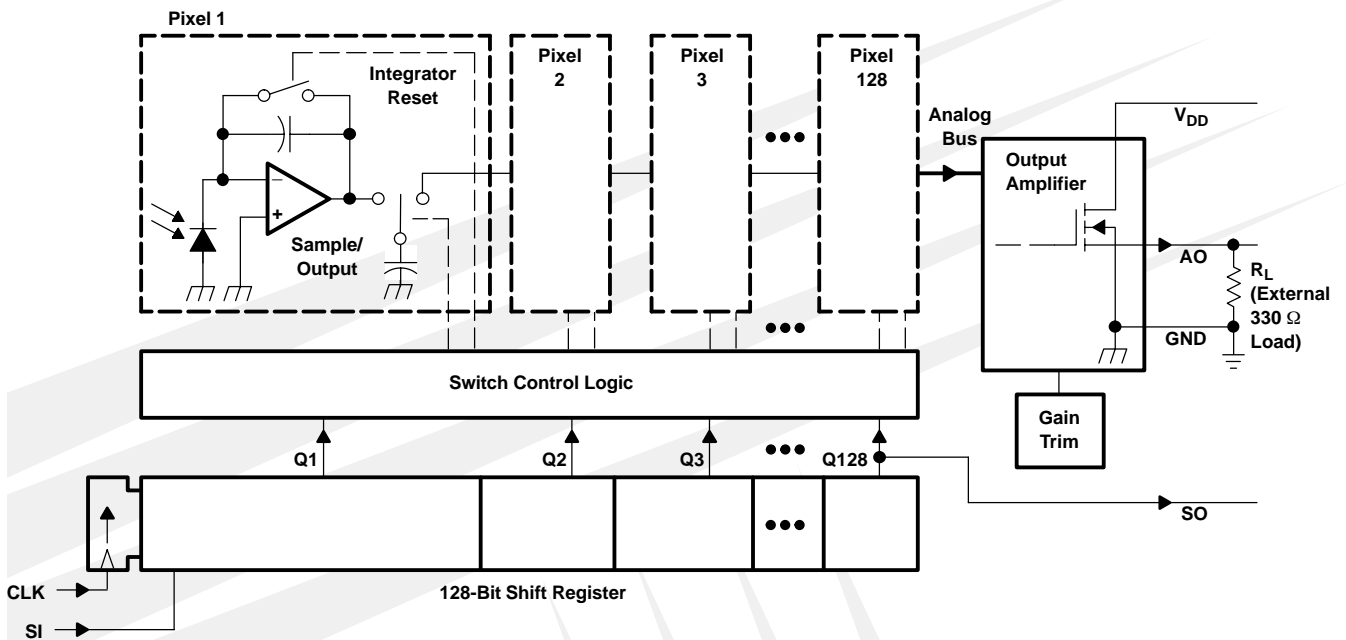
The TSL210 linear sensor array consists of five sections of 128 photodiodes, each with associated charge amplifier circuitry, running from a common clock. These sections can be connected to form a contiguous 640 × 1 pixel array. Device pixels measure 120 μm (H) by 70 μm (W) with 125-μm center-to-center pixel spacing. Operation is simplified by internal logic that requires only a serial input (SI1 through SI5) for each section and a common clock for the five sections.

The device is intended for use in a wide variety of applications including contact imaging, mark and code reading, bar-code reading, edge detection and positioning, OCR, level detection, and linear and rotational encoding.

**PACKAGE
(TOP VIEW)**



Functional Block Diagram (each section)



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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AO1	4	O	Analog output of section 1.
AO2	7	O	Analog output of section 2.
AO3	11	O	Analog output of section 3.
AO4	14	O	Analog output of section 4.
AO5	17	O	Analog output of section 5.
CLK	2	I	Clock input for all sections. The clock controls the charge transfer, pixel output, and reset.
GND	9		Ground (substrate). All voltages are referenced to the substrate.
SI1	3	I	SI1 defines the start of the data out sequence for section 1.
SI2	6	I	SI2 defines the start of the data out sequence for section 2.
SI3	10	I	SI3 defines the start of the data out sequence for section 3.
SI4	13	I	SI4 defines the start of the data out sequence for section 4.
SI5	16	I	SI5 defines the start of the data out sequence for section 5.
SO1	5	O	SO1 provides the signal to drive the SI2 input in serial mode or <i>end of data</i> for section 1 in parallel mode.
SO2	8	O	SO2 provides the signal to drive the SI3 input in serial mode or <i>end of data</i> for section 2 in parallel mode.
SO3	12	O	SO3 provides the signal to drive the SI4 input in serial mode or <i>end of data</i> for section 3 in parallel mode.
SO4	15	O	SO4 provides the signal to drive the SI5 input in serial mode or <i>end of data</i> for section 4 in parallel mode.
SO5	18	O	SO5 provides the signal to drive the SI input of another device for cascading or as an <i>end of data</i> indication.
VDD	1		Supply voltage for both analog and digital circuits.

Detailed Description

The device consists of five sections of 128 photodiodes (called pixels — 640 total in the device) arranged in a linear array. Each section has its own signal input and output lines, and all five sections are connected to a common clock line. Light energy impinging on a pixel generates photocurrent that is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time. The voltage output developed for each pixel is according to the following relationship:

$$V_{out} = V_{drk} + (R_e) (E_e) (t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in $V/(\mu J/cm^2)$
- E_e is the incident irradiance in $\mu W/cm^2$
- t_{int} is integration time in seconds

The output and reset of the integrators in each section are controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO (given above). After being read, the pixel integrator is then reset, and the next integration period begins for that pixel. On the 129th clock rising edge, the SO pulse is clocked out on SO signifying the end of the read cycle. The section is then ready for another read cycle. The SO of each section can be connected to SI on the next section in the array (Figure 4). SO can be used to signify the read is complete.

AO is driven by a source follower that requires an external pulldown resistor (330-Ω typical). The output is nominally 0 V for no light input, 2 V for normal white-level, and 3.4 V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

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Absolute Maximum Ratings†

Supply voltage range, V_{DD}	–0.3 V to 6 V
Input voltage range, V_I	–0.3 V to $V_{DD} + 0.3V$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	–20 mA to 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	–25 mA to 25 mA
Voltage range applied to any output in the high impedance or power-off state, V_O	–0.3 V to $V_{DD} + 0.3V$
Continuous output current, I_O ($V_O = 0$ to V_{DD})	–25 mA to 25 mA
Continuous current through V_{DD} or GND	–100 mA to 100 mA
Analog output current range, I_O	–25 mA to 25 mA
Operating free-air temperature range, T_A	–25°C to 85°C
Storage temperature range, T_{stg}	–25°C to 85°C
Lead temperature on connection pad for 10 seconds	260°C
ESD tolerance, human body model	2000 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		5000	kHz
Sensor integration time, serial, t_{int}	0.128		100	ms
Sensor integration time, parallel, t_{int}	0.026		100	ms
Load capacitance, C_L			330	pF
Load resistance, R_L	300		4700	Ω
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

Electrical Characteristics at $f_{\text{clock}} = 200 \text{ kHz}$, $V_{\text{DD}} = 5 \text{ V}$, $T_{\text{A}} = 25^{\circ}\text{C}$, $\lambda_{\text{p}} = 640 \text{ nm}$, $t_{\text{int}} = 5 \text{ ms}$, $R_{\text{L}} = 330 \Omega$, $E_{\text{e}} = 18 \mu\text{W}/\text{cm}^2$ (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Analog output voltage (white, average over 640 pixels)	See Note 2	1.6	2	2.4	V
V_{DRK}	Analog output voltage (dark, average over 640 pixels)	$E_{\text{e}} = 0$	0	0.05	0.15	V
PRNU	Pixel response nonuniformity	See Note 4			±20	%
	Nonlinearity of analog output voltage	See Note 5		±0.4%		FS
	Output noise voltage	See Note 6		1		mVrms
R_{e}	Responsivity		16	22	28	V/ ($\mu\text{J}/\text{cm}^2$)
SE	Saturation exposure	See Note 7		155		nJ/cm ²
V_{SAT}	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels, $E_{\text{e}} = 0$, See Note 8		0.04	0.12	V
IL	Image lag	See Note 9		0.5		%
I_{DD}	Supply current			125	160	mA
I_{IH}	High-level input current	$V_{\text{I}} = V_{\text{DD}}$			10	μA
I_{IL}	Low-level input current	$V_{\text{I}} = 0$			10	μA
V_{OH}	High-level output voltage, SO1 – SO5	$I_{\text{O}} = 50 \mu\text{A}$	4.5	4.95		V
		$I_{\text{O}} = 4 \text{ mA}$		4.6		
V_{OL}	Low-level output voltage, SO1 – SO5	$I_{\text{O}} = 50 \mu\text{A}$		0.01	0.1	V
		$I_{\text{O}} = 4 \text{ mA}$		0.4		
$C_{\text{i(SI)}}$	Input capacitance, SI			20		pF
$C_{\text{i(CLK)}}$	Input capacitance, CLK			50		pF

- NOTES: 2. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
3. Clock duty cycle is assumed to be 50%.
4. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
5. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
6. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
7. Minimum saturation exposure is calculated using the minimum V_{sat} , the maximum V_{drk} , and the maximum R_{e} .
8. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
9. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$\text{IL} = \frac{V_{\text{out(IL)}} - V_{\text{drk}}}{V_{\text{out(white)}} - V_{\text{drk}}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{\text{su(SI)}}$	Setup time, serial input (see Note 10)	20			ns
$t_{\text{h(SI)}}$	Hold time, serial input (see Note 10 and Note 11)	0			ns
t_{w}	Pulse duration, clock high or low	50			ns
$t_{\text{r}}, t_{\text{f}}$	Input transition (rise and fall) time	0		500	ns

- NOTES: 10. Input pulses have the following characteristics: $t_{\text{r}} = 6 \text{ ns}$, $t_{\text{f}} = 6 \text{ ns}$.
11. SI must go low before the rising edge of the next clock pulse.

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Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s Analog output settling time to $\pm 1\%$	$C_L = 10 \text{ pF}$		185		ns

TYPICAL CHARACTERISTICS

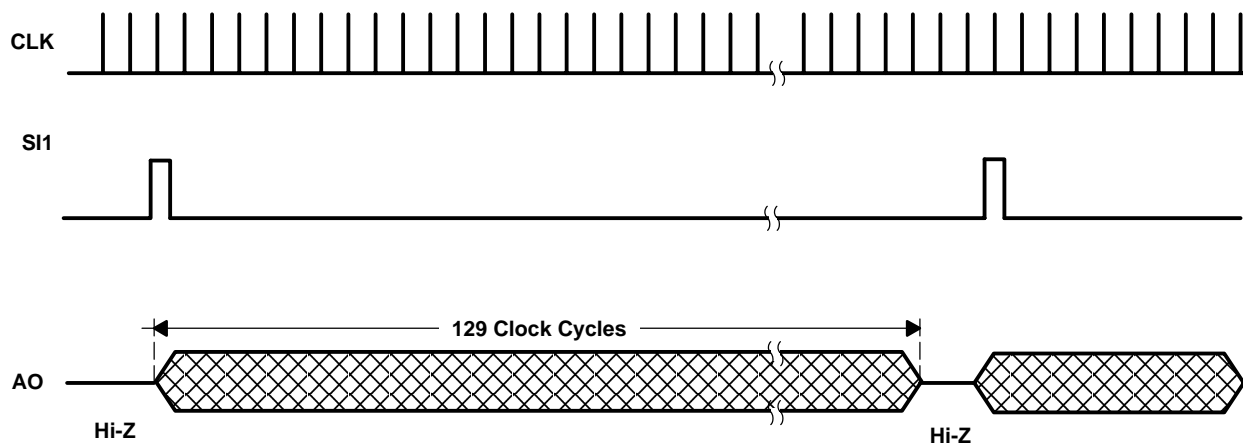


Figure 1. Timing Waveforms (each section)

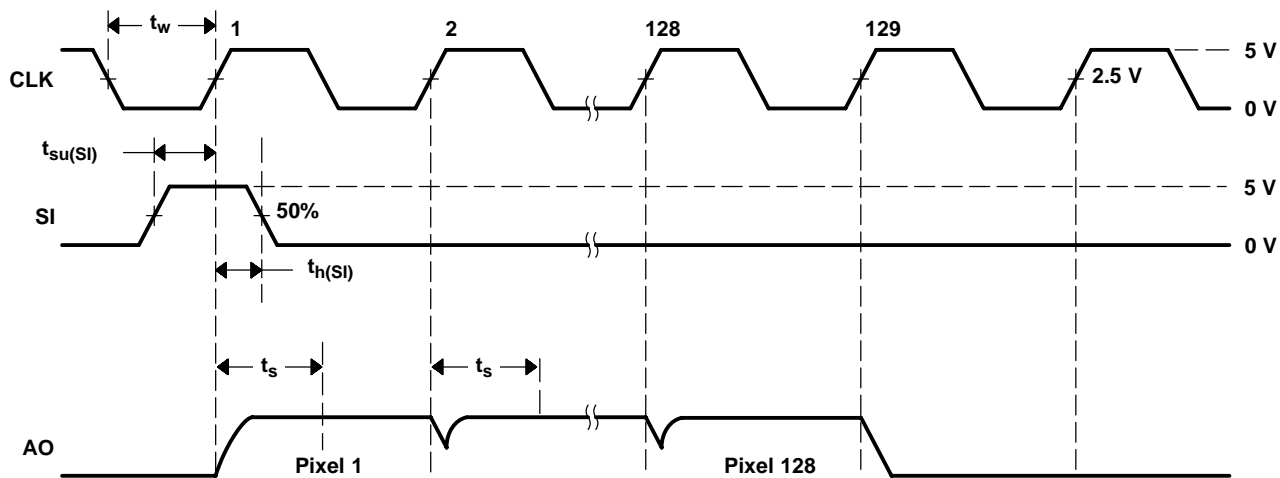


Figure 2. Operational Waveforms (each section)

TYPICAL CHARACTERISTICS

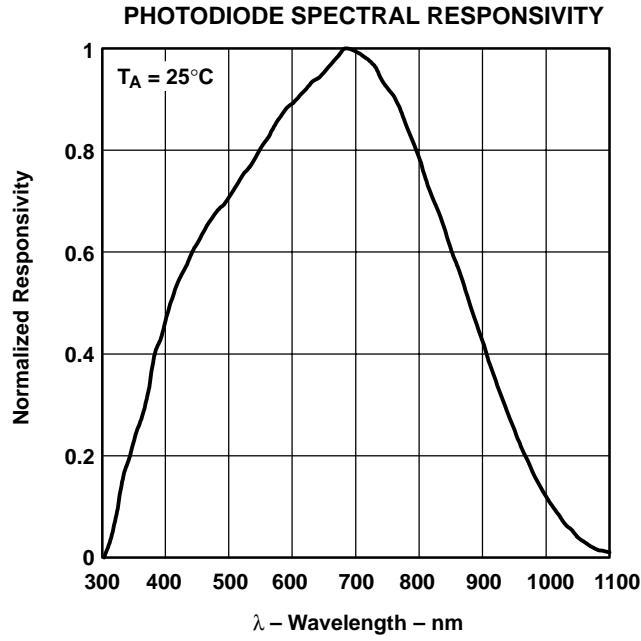


Figure 3

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APPLICATION INFORMATION

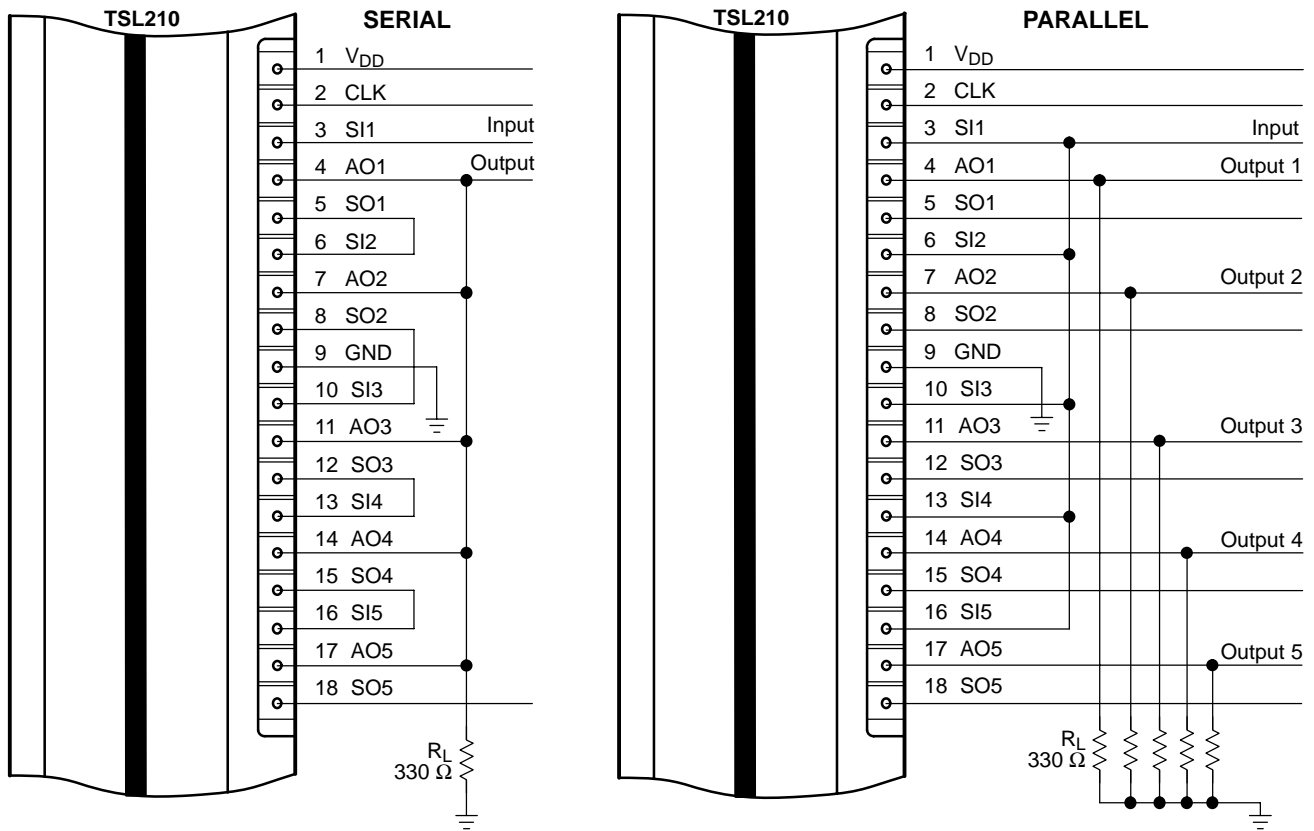
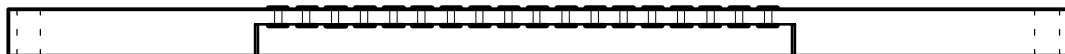


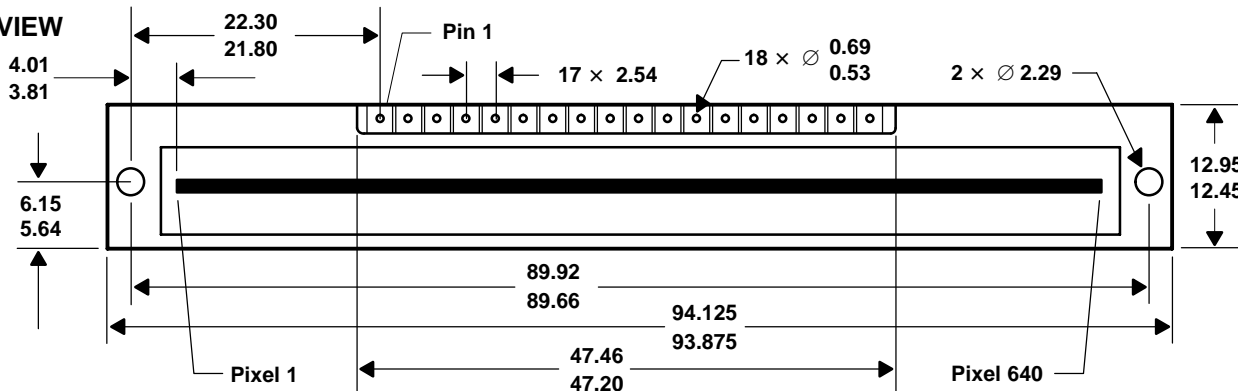
Figure 4. Connection Diagrams

MECHANICAL INFORMATION

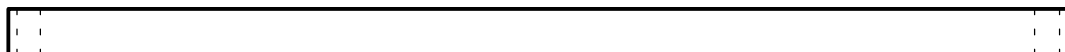
SIDE VIEW



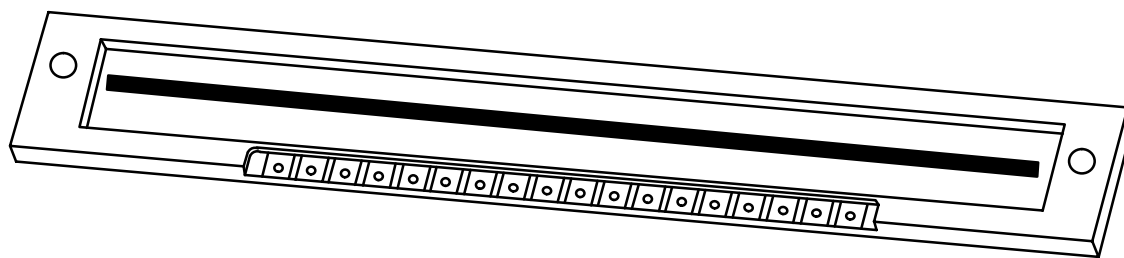
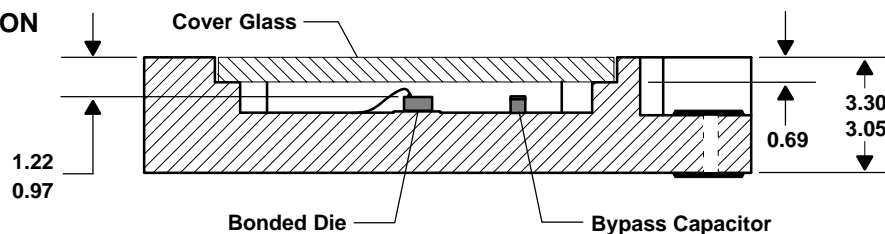
TOP VIEW



SIDE VIEW



CROSS SECTION



- NOTES: A. All linear dimensions are in millimeters.
 B. Pixel centers are located along the center line of the mounting holes.
 C. Cover glass index of refraction is 1.52.
 D. This drawing is subject to change without notice.

Figure 5. TSL210 Mechanical Specifications

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