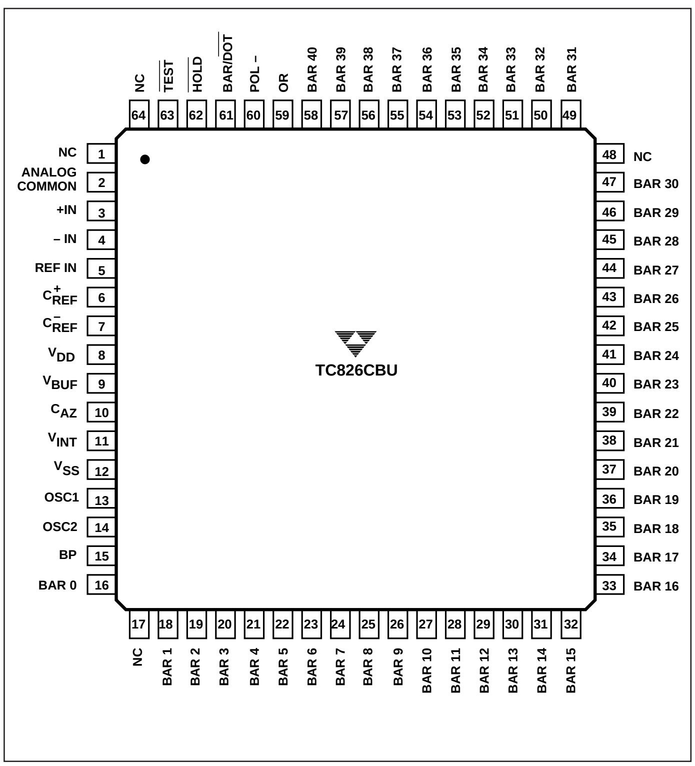
TelCom Semiconductor, Inc.

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

FEATURES

- **Bipolar A/D Conversion**
- **2.5% Resolution**
- **Direct LCD Display Drive**
- **'Thermometer' Bar or Dot Display**
- **40 Data Segments Plus Zero**
- **Overrange Plus Polarity Indication**
- **Precision On–Chip Reference .... 35ppm/°C**
- **Differential Analog Input**
- **Low Input Leakage 10pA**
- **Display Flashes on Overrange**
- **Display Hold Mode**
- **Auto–Zero Cycle Eliminates Zero Adjust Potentiometer**
- **9V Battery Operation**
- **Low Power Consumption 1.1mW**
- **20mV to 2.0 V Full–Scale Operation**
- **Non–Multiplexed LCD Drive for Maximum Viewing Angle**

PIN CONFIGURATION



GENERAL DESCRIPTION

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TC826 is a complete analog–to–digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full–scale differential input voltage range extends from 20mV to 2V. The TC826 sensitivity is 500µv. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design required only 125µA from a 9V battery. In +5V systems a TC7660 DC to DC converter can supply the –5V supply. The differential analog input leakage is a low 10pA.

Two display formats are possible. The BAR mode display is like a 'thermometer' scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto–zero phase maximizes noise immunity and eliminates zero–scale adjustment potentiometers. Zero–scale drift is a low 5 µV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TC826 prototyping work.

ORDERING INFORMATION

Part No.	Package	Temperature
TC826CBU	64–Pin PFP	0°C to +70°C

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)[1] .... V^+ to V^-
Power Dissipation ($T_A \leq 70°C$)
64-Pin Flat Package 1.14W
Operating Temperature
'C' Devices ....0°C to +70°C
Storage Temperature ....– 65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: unless otherwise stated V_S = 9V; R_{OSC} = 430 kΩ; T_A = 25°C; Full–Scale = 20 mV.

No.	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1	—	Zero Input	V_{IN} = 0.0V	– 0	±0	+0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0V 0°C ≤ T_A ≤ +70°C	—	0.2	1	μV/°C
3	NL	Linearity Error	Max Deviation From Best Straight Line	– 1	0.5	+1	Count
4	R/O	Rollover Error	$-V_{IN} = +V_{IN}$	– 1	0	+1	Count
5	EN	Noise	V_{IN} = 0V	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	V_{IN} = 0V	—	10	20	pA
7	CMRR	Common–Mode Rejection Ratio	VCM = ±1V V_{IN} = 0V	—	50	—	μV/V
8	—	Scale Factor Temperature Coefficient	0 ≤ T_A ≤ +70°C External Ref. Temperature Coefficient = 0 ppm/°C	—	1	—	ppm/°C
9	VCTC	Analog Common Temperature Coefficient	250kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C	—	35	100	ppm/°C
10	V_{COM}	Analog Common Voltage	250kΩ Between Common and V_{DD}	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	I_{DD}	Power Supply Current		—	125	175	μA

NOTES:
1. Input voltages may exceed the supply voltages when the input current is limited to 100μA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for 'off' segment and 180°C out of phase for 'on' segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, and 60 should be connected through 1MΩ series resistors to V_{SS} for logic 0.

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PIN DESCRIPTION

Pin No. (64-Plastic Quad Flat Package)	Symbol	Description
1	NC	
2	ANALOG COMMON	Establishes the internal analog ground point. Analog common is set to 2.9V below the positive supply by an internal zener reference circuit. The voltage difference beween V_{DD} and analog-common can be used to supply the TC826 voltage reference input at REF IN (Pin 5).
3	+IN	Positive analog signal input.
4	-IN	Negative analog signal input.
5	REF IN	Reference voltage positive input. Measured relative ato analog-common. REF IN ≈ Full-Scale/2.
6	$CREF^+$	Reference capacitor connection.
7	$CREF^-$	Reference capacitor connection.
8	V_{DD}	Positive supply terminal.
9	V_{BUF}	Buffer output. Integration resistor connection.
10	C_{AZ}	Negative comparator input. Auto-zero capacitor connection.
11	V_{INT}	Integrator output. Integration capacitor connection.
12	V_{SS}	Negative supply terminal.
13	OSC1	Oscillator resistor (ROSC) connection.
14	OSC2	Oscillator resistor (ROSC) connection.
15	BP	LCD Backplane driver.
16	BAR 0	LCD Segment driver: Bar 0
17	NC	
18	BAR 1	LCD Segment driver: Bar 1
19	BAR 2	LCD Segment driver: Bar 2
20	BAR 3	LCD Segment driver: Bar 3
21	BAR 4	LCD Segment driver: Bar 4
22	BAR 5	LCD Segment driver: Bar 5
23	BAR 6	LCD Segment driver: Bar 6
24	BAR 7	LCD Segment driver: Bar 7
25	BAR 8	LCD Segment driver: Bar 8
26	BAR 9	LCD Segment driver: Bar 9
27	BAR 10	LCD Segment driver: Bar 10
28	BAR 11	LCD Segment driver: Bar 11
29	BAR 12	LCD Segment driver: Bar 12
30	BAR 13	LCD Segment driver: Bar 13
31	BAR 14	LCD Segment driver: Bar 14
32	BAR 15	LCD Segment driver: Bar 15
33	BAR 16	LCD Segment driver: Bar 16
34	BAR 17	LCD Segment driver: Bar 17
35	BAR 18	LCD Segment driver: Bar 18
36	BAR 19	LCD Segment driver: Bar 19
37	BAR 20	LCD Segment driver: Bar 20
38	BAR 21	LCD Segment driver: Bar 21
39	BAR 22	LCD Segment driver: Bar 22
40	BAR 23	LCD Segment driver: Bar 23

PIN DESCRIPTION (Cont.)

Pin No. (64-Plastic Quad Flat Package)	Symbol	Description
41	BAR 24	LCD Segment driver: Bar 24
42	BAR 25	LCD Segment driver: Bar 25
43	BAR 26	LCD Segment driver: Bar 26
44	BAR 27	LCD Segment driver: Bar 27
45	BAR 28	LCD Segment driver: Bar 28
46	BAR 29	LCD Segment driver: Bar 29
47	BAR 30	LCD Segment driver: Bar 30
48	NC	
49	BAR 31	LCD Segment driver: Bar 31
50	BAR 32	LCD Segment driver: Bar 32
51	BAR 33	LCD Segment driver: Bar 33
52	BAR 34	LCD Segment driver: Bar 34
53	BAR 35	LCD Segment driver: Bar 35
54	BAR 36	LCD Segment driver: Bar 36
55	BAR 37	LCD Segment driver: Bar 37
56	BAR 38	LCD Segment driver: Bar 38
57	BAR 39	LCD Segment driver: Bar 39
58	BAR 40	LCD Segment driver: Bar 40
59	OR	LCD segment driver that indicated input out–of–range condition.
60	POL–	LCD segment driver that indicates input signal is negative.
61		Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to V_{SS} through 1MΩ resistor for Dot format.
62		Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_{SS} through 1MΩ series resistor for HOLD mode operation.
63		Input logic signal. Sets TC826 to BAR display mode. BAR 0 to 40, plus OR flash on and off. The POL– LCD driver is on. Pulled high internally to inactive state. Connect to V_{SS} with 1 MΩ series resistor to activate.
64	NC	

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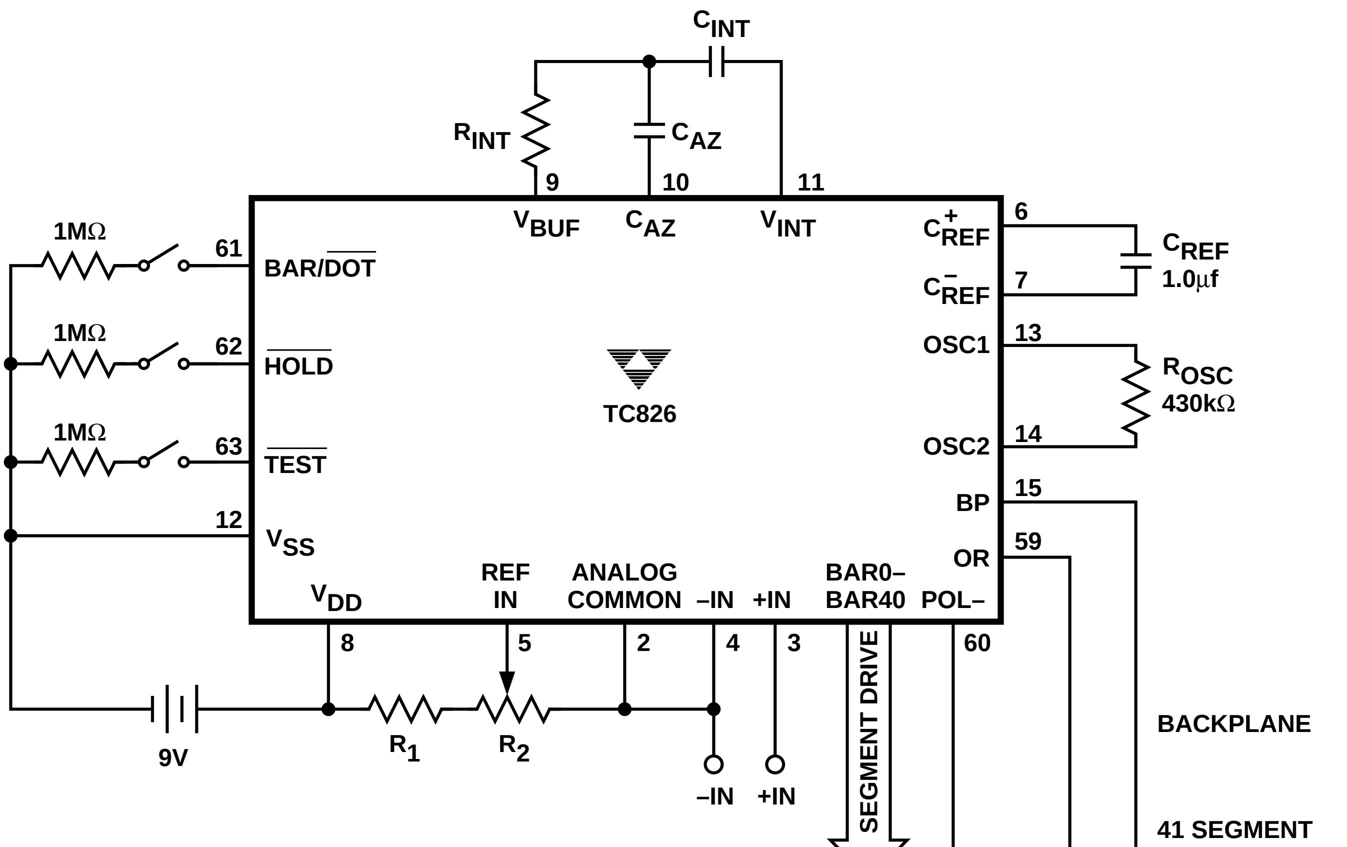

COMPONENT	2V FULL–SCALE	200 mV FULL–SCALE	20 mV FULL–SCALE
R_{INT}	2MΩ	20kΩ	20kΩ
C_{INT}	0.033µf	0.033 µf	0.033 µf
C_{REF}	1µf	1µf	1µf
C_{AZ}	0.068µf	0.068µf	0.014µf

$R_1 + R_2 = 250k\Omega$

Figure 1. Typical TC826 Circuit Connection

DUAL SLOPE CONVERSION PRINCIPLES

The TC826 is a dual slope, integrating analog–to–digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (TSI). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (TRI). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to 'ramp–up' and 'ramp–down'.

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R T_{RI}}{RC}$$

Where:
V_R = Reference Voltage
V_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3.)

The TC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

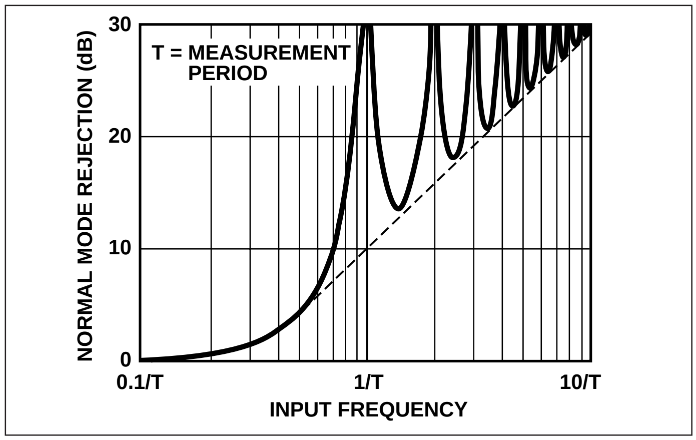

Figure 3. Normal-Mode Rejection of Dual Slope Converter

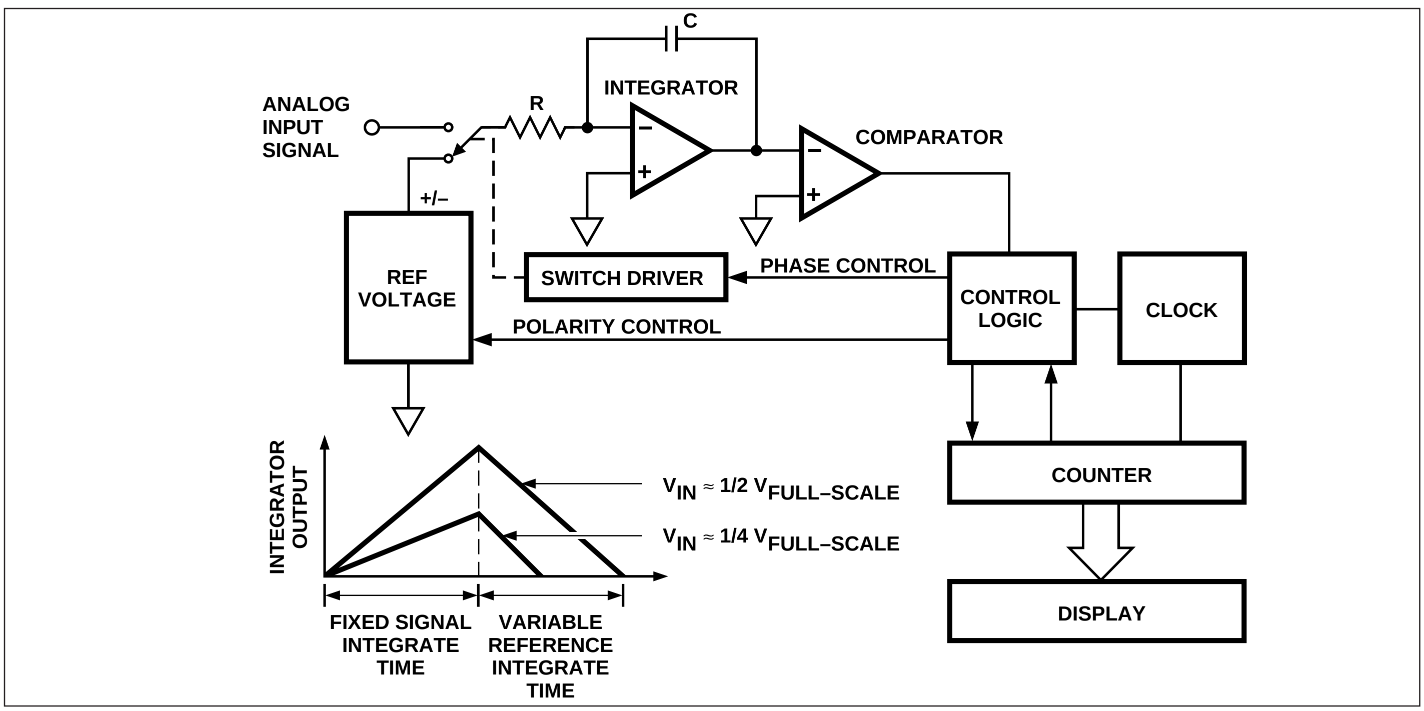

Figure 2. Basic Dual Slope Converter

THEORY OF OPERATION

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above, the TC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference cycle. (Figures 4 and 5.)

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and –IN. The differential input signal is integrated for a fixed time period. The TC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is divided by 32 before clocking the internal counters. The integration time period is:

Where: $T_{SI} = \frac{32}{F_{OSC}} \times 20$

F_{OSC} = External Clock Frequency

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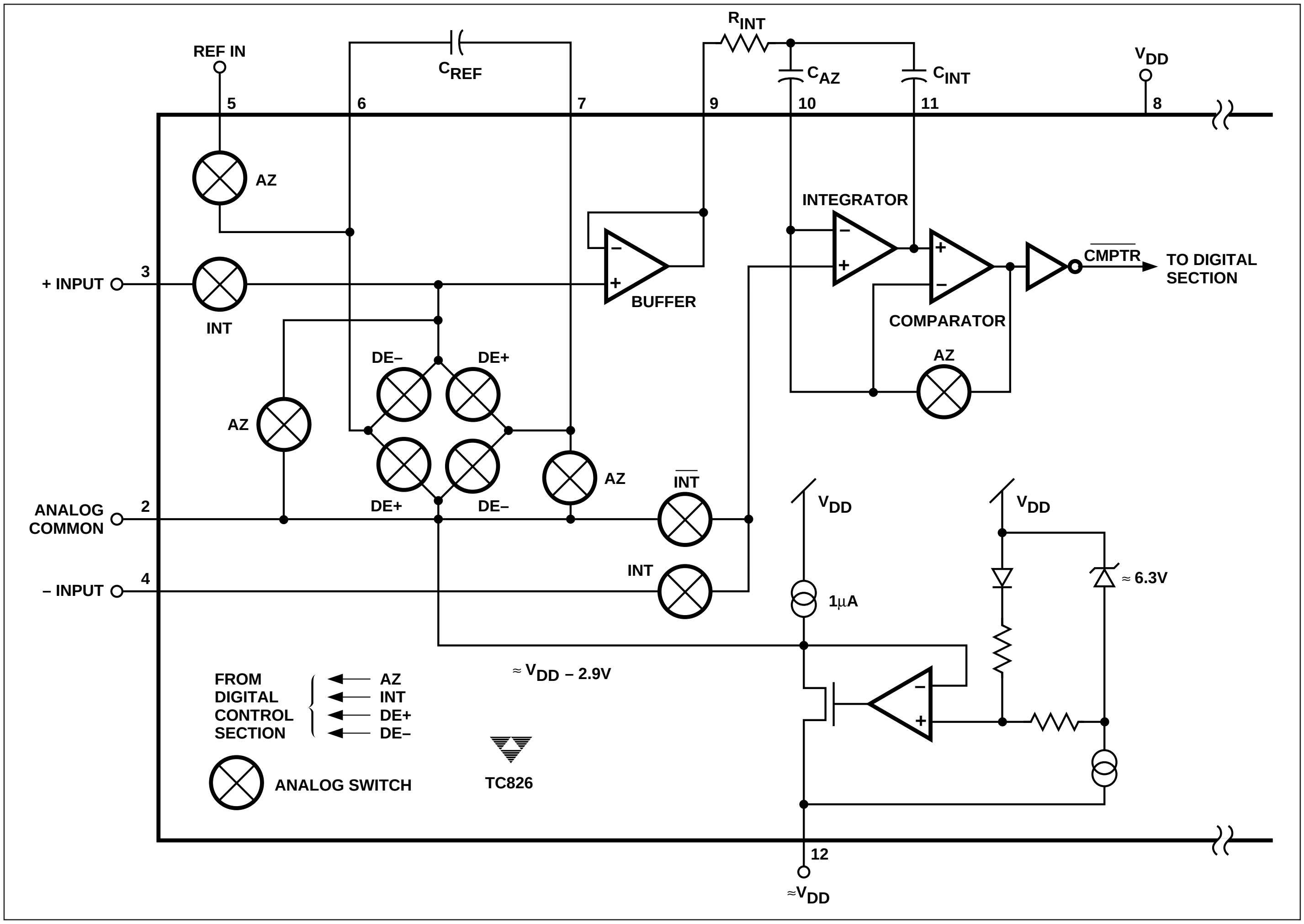

Figure 4. TC826 Analog Section

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, –IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. –IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20 = \frac{V_{IN}}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

  $$T_{SI} = 20\left[\frac{32}{F_{OSC}}\right]$$

  Where F_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 5) and ANALOG COMMON Pin 2).

Required Full-Scale Voltage	V_{REF}
20mV	10mV
2V	1V

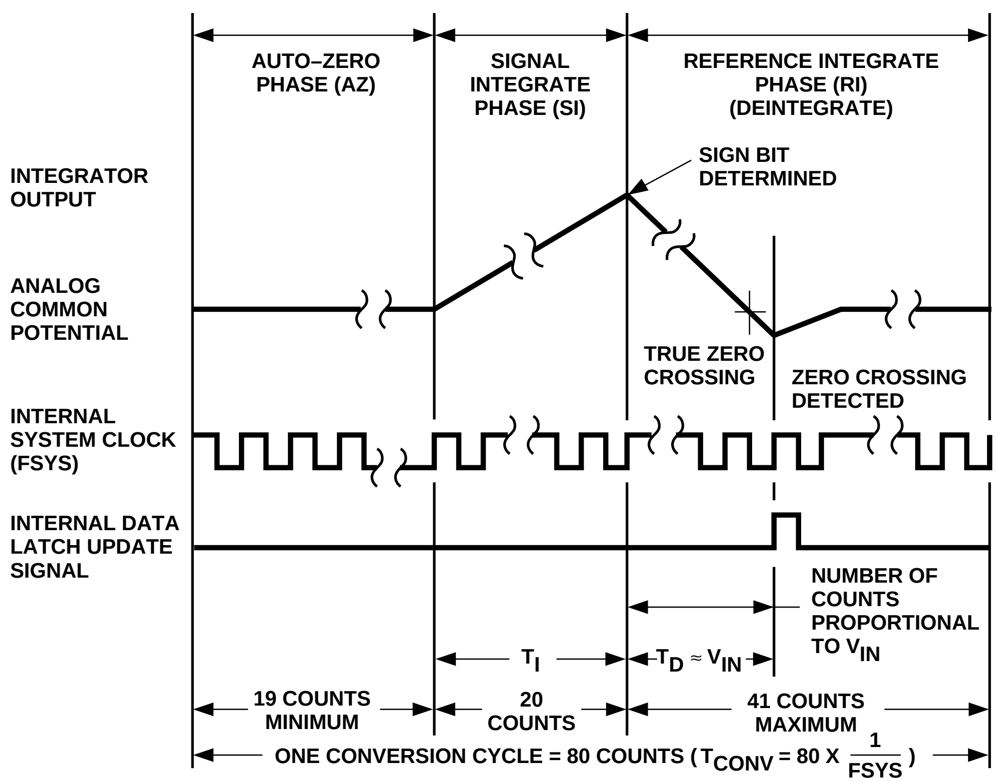

Figure 5. TC826 Conversion Has Three Phases

The internal voltage reference potential availabe at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

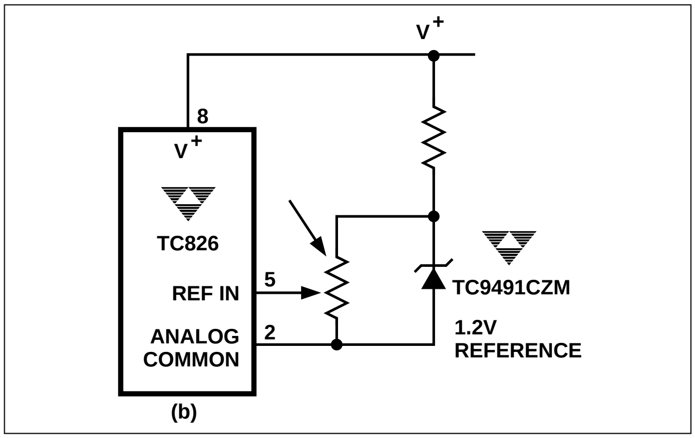

Figure 6. External Reference

Components Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1μA drive durrent with minimal linearity error. R_{INT} is easily calculated for a 1μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be slected to maximize intgrator output swing. The integrator output will swing to within 0.4V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$C_{INT} = \frac{VFS}{R_{INT}} \left(\frac{640}{F_{OSC} \times V_{INT}} \right)$$

Where : V_{INT} = Integrator Swing
F_{OSC} = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

C_{AZ} should be 2–3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14μF to 0.068 μF are satisfactory.

Reference Capacitor (CREF)

A 1 μF capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1 Suggested Component Values

Component	2V Full-Scale $V_{REF} \approx 1V$	200 mV Full-Scale $V_{REF} \approx 100$ mV	20 mV Full-Scale $V_{REF} \approx 10$ mV
R_{INT}	2 MΩ	200kΩ	20kΩ
C_{INT}	0.033μF	0.033μF	0.033μF
C_{REF}	1μF	1μF	1 F
C_{AZ}	0.068μF	0.068μF	0.14μF
R_{OSC}	430kΩ	430kΩ	430kΩ

NOTES: Approximately 5 conversions/second.

Differential Signal Inputs

The TC826 is designed with true differential inputs and accepts input signals within the input stage common–mode voltage range (VCM). The typical range is V^+ –1 to V^- +1V. Common–mode voltages are removed from the system when the TC826 operates from a battery or floating power source (Isolated from measured system) and –IN is connected to analog–common (V_{COM}).

In systems where common–mode rejection ratio minimizes error. Common–mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full–scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2V full–scale swing. The integrator output will swing within 0.3V of V_{DD} or V_{SS} without increased linearity error.

Digital Section

The TC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430kΩ $_{OSC}$ gets the backplane frequency to approximately 55Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is 'OFF'. An out–of–phase segment drive signal causes the segment to be 'ON' or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment drive, –POL, is 'ON' for negative analog inputs. If +IN and –IN are reversed this indicator would reverse. The TC826 transfer function is shown in Figure 7.

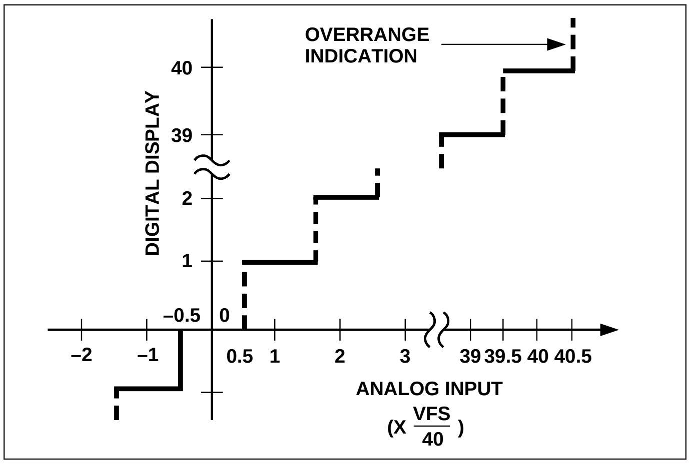

Figure 7. TC826 Transfer Function

BAR/$\overline{\text{DOT}}$ Input (Pin 61)

The BAR/$\overline{\text{DOT}}$ input allows the user to select the display format. The TC826 powers up in the BAR mode. Select the DOT display format by connecting BAR/$\overline{\text{DOT}}$ to the negative supply (Pin 12) through a 1MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 62)

The TC826 data ouput latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 12) through a 1 MΩ resistor. The LCD display continously displays the previous conversion results.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 63)

The TC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 12). The connection must be made through a 1MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annuniciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL–) segment will be on but not flashing

Overrange Display Operation (OR, Pin 59)

An out–of–range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 59) becoming active.

In the BAR display format the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is on fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL– Pin 60)

The TC826 converts and displays data for positive and negative input signals. The POL– LCD segment driver (Pin 60) is active for negative signals.

Oscillator Operation

The TC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 13 and 14. The oscillator frequency versus resistance curve is shown in Figure 8.

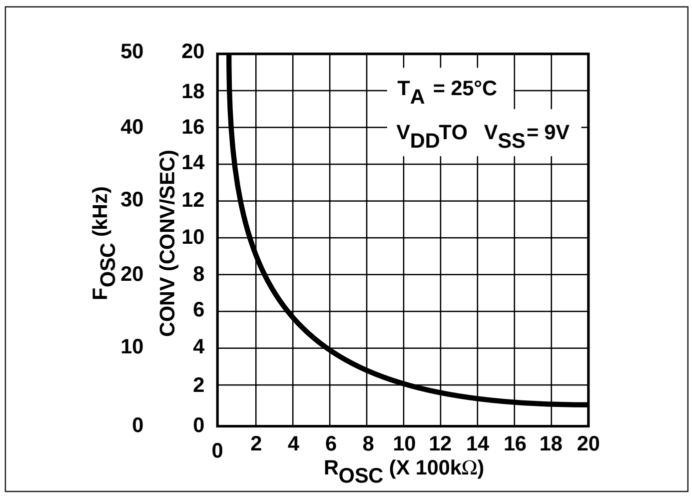

Figure 8. Oscillator Frequency vs. ROSC

FOSC is divided by 32 to provide an internal system clock, FYSY. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320.

The internal oscillator may be bypassed by driving OSCI (Pin 13) with an external signal generator. OSC2 (Pin 14) should be left unconnected.

The oscillator should swing from V_{DD} to V_{SS} in single supply operation (Figure 9). In dual supply operation the signal should swing from power supply ground to V_{DD}.

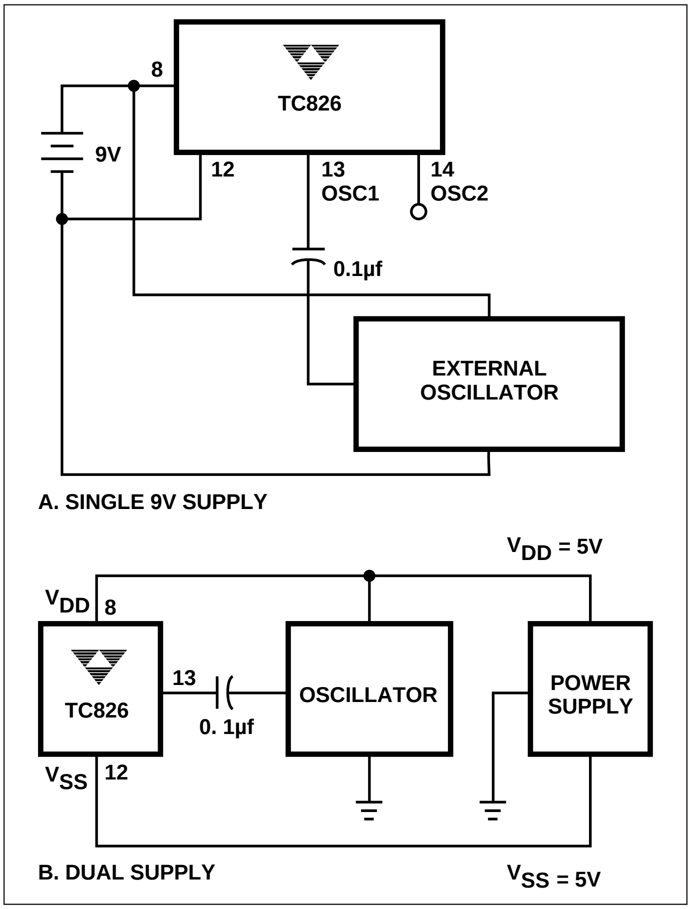

Figure 9. External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 10). The BAR/$\overline{\text{DOT}}$ input (Pin 61) selects the format. The TC826 measurement cycle operates indentically for either mode.

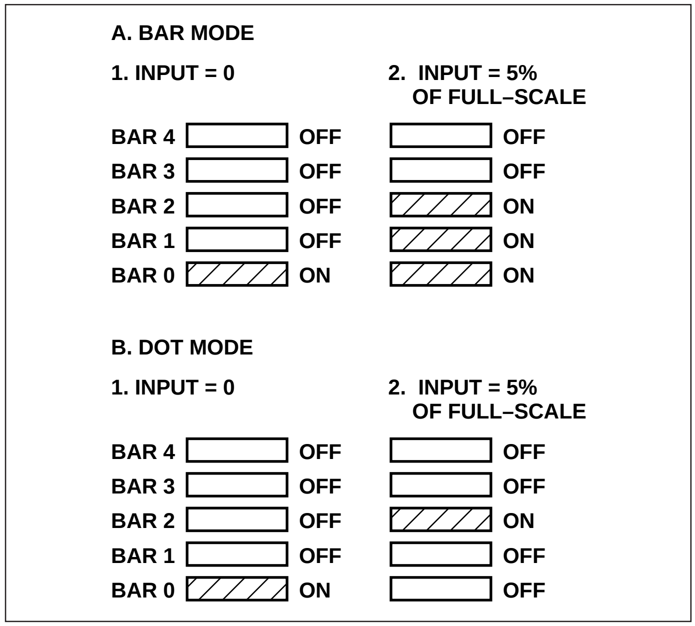

Figure 10. Display Option Formats

BAR Format

The TC826 power-ups in the BAR mode. BAR/$\overline{\text{DOT}}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equaling the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR/$\overline{\text{DOT}}$ to V_{SS} through a 1MΩ resistor the DOT mode is selected. Only the BAR LCD segment equaling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or 'needle' applications.

LCD DISPLAYS

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TC826 LCD display is available from Varitronix.

Varitronix Ltd. LCDs
4/F Liven House
61-63 King Yip Street
Kwun Tong, Kowloon
Hong Kong
Tel: (852)2389-4317
Fax: (852)2343-9555

USA Office:
VL Electronics / Varitronix
3250 Wilshire Blvd., Suite 901
Los Angeles, CA 90010
Tel: (213) 738-8700
Fax: (213) 738-5340

- Part No.: VBG-413-DP

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
Tel: 203/838-7509

- Part No. 5040: 50 segment circular display with 3 digit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD BACKPLANE DRIVER (PIN 15)

Additional drive electronics is not required to interface the TC826 to an LCD display. The TC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$F_{BP} = F_{OSC}/256$$

Figure 11 gives typical backplane driver rise/fall time versus backplane capacitance.

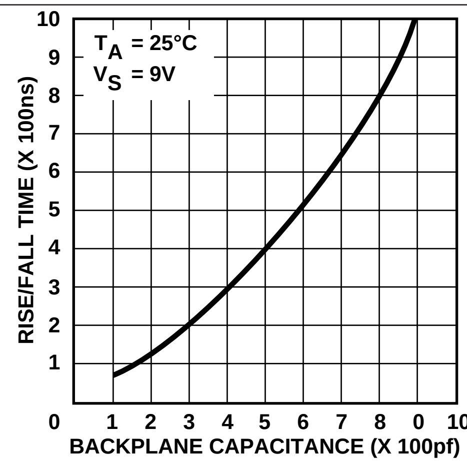

Figure 11. Backplane Driver Rise/Fall Time vs. Capacitance

FLAT PACKAGE SOCKET

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
Tel: 415/856-9332
Telex: 910/373-2060

'BQ' Socket Part No.: IC51-064-042 BQ