CMOS CURRENT MODE PWM CONTROLLER

FEATURES

- **Low Supply Current With CMOS Technology ..... 3.8mA Max**
- **Internal Reference 5.1V**
- **Fast Rise/Fall Times (C_L = 1000pF) 50nsec**
- **Dual Push-Pull Outputs**
- **Direct-Power MOSFET Drive**
- **High Totem-Pole Output Drive 300mA**
- **Differential Current-Sense Amplifier**
- **Programmable Current Limit**
- **Soft-Start Operation**
- **Double-Pulse Suppression**
- **Undervoltage Lockout**
- **Wide Supply Voltage Operation 8V to16V**
- **High Frequency Operation 200kHz**
- **Available with Low OFF State Outputs**
- **Low Power, Pin-Compatible Replacement for UC3846**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC170COE	16-Pin SOIC (Wide)	0°C to +70°C
TC170CPE	16-Pin Plastic DIP (Narrow)	0°C to +70°C

GENERAL DESCRIPTION

The TC170 brings low-power CMOS technology to the current-mode-switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current-mode control integrated circuits require five times more operating current.

The dual totem-pole CMOS outputs drive power MOSFETs or bipolar transistors. The 50nsec typical output rise and fall times (1000pF capacitive loads) minimize MOSFET power dissipation. Output peak current is 300mA.

The TC170 contains a full array of system-protection circuits (see features).

Current-mode control lets users parallel power supply modules. Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator or an external system oscillator.

The TC170 operates from an 8V to 16V power supply. An internal 2%, 5.1V reference minimizes external component count. The TC170 is pin compatible with the Unitrode UC1846/2846/3846 bipolar controller.

Other advantages inherent in current-mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

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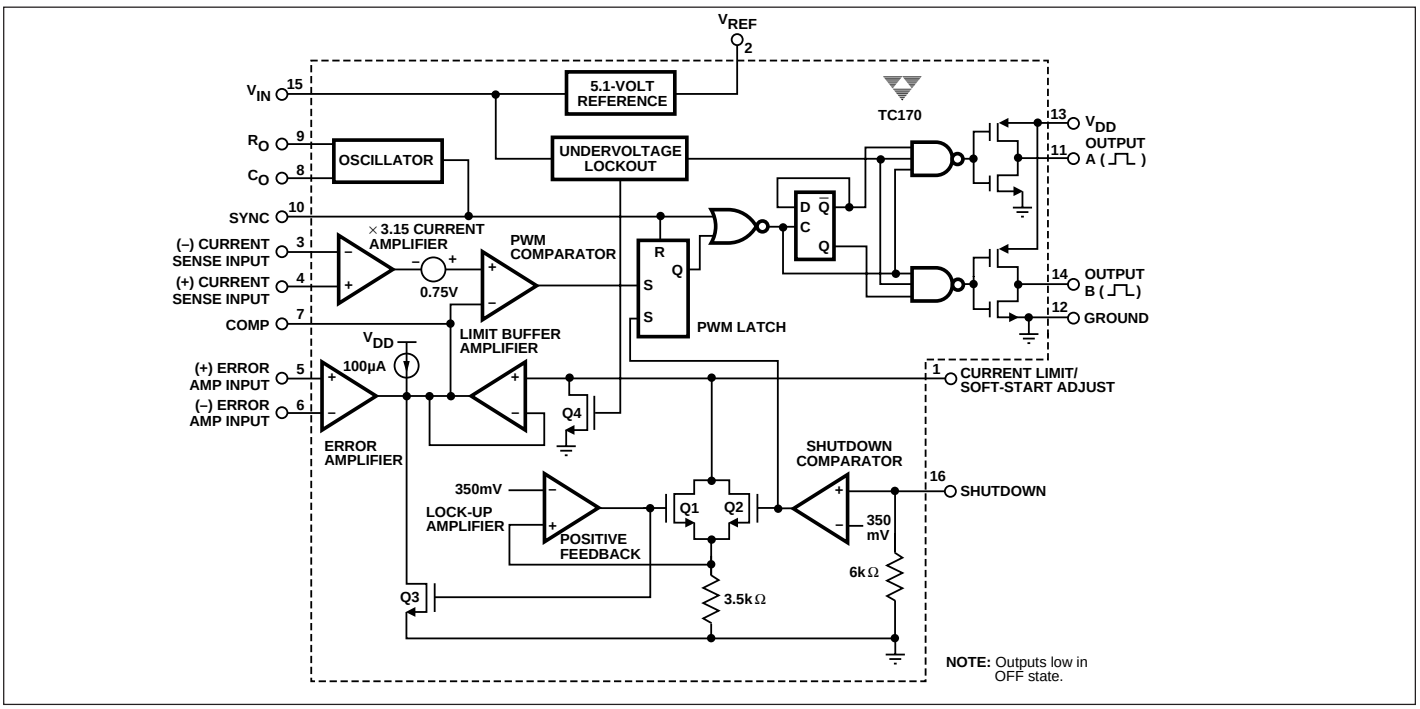
FUNCTIONAL BLOCK DIAGRAM



TC170

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 18V
Output Voltage ..... V_{DD} or 18V
Analog Inputs ..... – 0.3V to V_S + 0.3V
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Maximum Chip Temperature ..... 150°C
Plastic Package Thermal Resistance:
θ_{JA} (Junction to Ambient) ..... 140°C/W
θ_{JC} (Junction to Case) ..... 70°C/W

Operating Temperature Range
Commercial ..... 0°C to +70°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{IN} = 16V, R_O = 24kΩ, C_O = 1 nF, T_A = 25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Reference Voltage						
V_{REF}	Output Voltage	I_{OUT} = 1mA	5	5.1	5.3	V
	Line Regulation	V_{IN} = 8V to 16V		5	15	mV
	Load Regulation	I_{OUT} = 1mA to 10mA		13	20	mV
V_{RTC}	Temperature Coefficient	Over Operating Temperature Range		0.4	0.5	mV/°C
Oscillator						
	Oscillator Frequency		35	42	46	kHz
	Voltage Stability	V_{IN} = 8V to 16V		1.1	1.5	%/V
	Temperature Stability	Over Operating Temperature Range		5	10	%
Error Amplifier						
V_{OS}	Input Offset Voltage				±30	mV
I_B	Input Bias Current				±1	nA
V_{CMRR}	Common-Mode Input Voltage	V_{IN} = 8V to 16V	0		V_{DD} – 2V	V
A_{VOL}	Open-Loop Voltage Gain	V_{OUT} = 1V to 6V	70			dB
BW	Unity Gain Bandwidth			1.2		MHz
CMRR	Common-Mode Rejection Ratio	V_{CMV} 0V to 14V	60			dB
PSRR	Power Supply Rejection Ratio	V_{IN} = 8V to 16V	60			dB
Current Sense Amplifier						
	Amplifier Gain	Pin 3 = 0V to 1.1V	3	3.15	3.3	V/V
	Maximum Differential Input Signal	$V_{PIN4} – V_{PIN3}$			≤1.1	V
	Common-Mode Input Voltage		0		V_{DD} – 3V	V
Current Limit Adjust						
	Current Limit Offset Voltage		0.5		1	V
I_B	Input Bias Current				1	nA
Shutdown Terminal						
V_{TB}	Threshold Voltage		0.3	0.35	0.4	V
V_{IN}	Input Voltage Range		0		V_{DD}	V
	Minimum Latching Current at Pin 1		125			µA
	Maximum Nonlatching Current at Pin 1				50	µA
Output Stage						
V_{DD}	Output Voltage	Pin 13	V_{IN} – 0. 5	V_{IN}	V_{IN} + 0.5	V
V_{OL}	Output Low Level	I_{SINK} = 20mA			0.4	V
V_{OL}	Output Low Level	I_{SINK} = 100mA			2	V

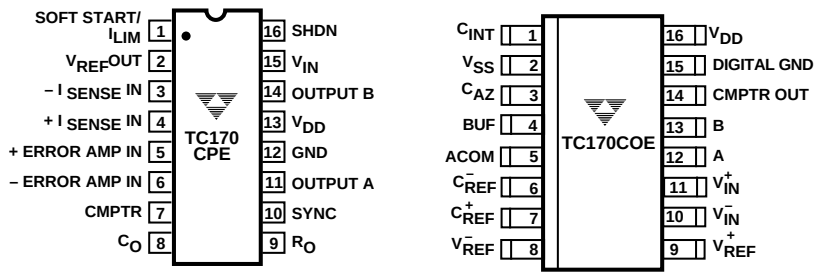
ELECTRICAL CHARACTERISTICS (Cont.): V_{IN} = 16V, R_O = 24kΩ, C_O = 1nF, T_A = 25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Output Stage (Cont.)						
V_{OH}	Output High Level	I_{SOURCE} = 20mA	V_{DD} – 1V			V
V_{OL}	Output High Level	I_{SOURCE} = 100mA	V_{DD} – 4V			V
t_R	Output Rise Time	C_L = 1000pF		50	150	nsec
t_F	Output Fall Time	C_L = 1000pF		50	150	nsec
Undervoltage Lockout						
	Start-Up	Threshold	7.15	7.7	8.25	V
	Threshold Hysteresis		0.5	0.75	1	V
Supply						
I_S	Standby Supply Current			2.7	3.8	mA

PIN DESCRIPTION

Pin No. (16-Pin PDIP)	Symbol	Description
1	SOFT START/I_{LIM}	Soft Start Adjust / Current Limit. For setting the peak current threshold of sense inputs (pins 3 and 4). Second function of this pin is Soft-Start Adjust.
2	V_{REF} OUT	Reference supply output of 5.1 volts. It can supply a minimum of 10mA.
3	– I_{SENSE} IN	– Current Sense Input. Inverting input for sensing peak current of the pass transistor through series sense current monitor resistor.
4	+ I_{SENSE} IN	+ Current Sense Input. Non-inverting input used in conjunction with pin 3. This senses the positive end of current monitor resistor.
5	+ ERROR AMP IN	+ Error Amp In. Non-inverting input for output voltage regulation.
6	– ERROR AMP IN	– Error Amp In. Inverting input of the amplifier for the reference voltage.
7	CMPTR	For compensation of the feedback loop response.
8	C_O	Timing capacitor (C_O) input to set oscillator frequency in conjunction with pin 9, R_O, resistor input. Second function is for setting crossover dead time of pin 11and 14 outputs.
9	R_O	Timing resistor (R_O) input to set oscillator frequency by setting constant current charge rate to charge capacitor C_O.
10	SYNC	For PWM controller oscillator synchronization of two or more controllers. or as a clock input to sync oscillator from external signal.
11	OUTPUT A	A output drive of phase A from push pull transistors.
12	GND	Ground return for all input and output pins.
13	V_{DD}	Supplies power to operate the output drivers only.
14	OUTPUT B	Output of phase B from push pull transistors.
15	V_{IN}	Voltage bias supply for all TC170 circuits except the output transistors.
16	SHUTDOWN	Input pin to disable both output drives to 0V OFF.

PIN CONFIGURATIONS (DIP and SOIC)



NOTE: Outputs LOW in "OFF" state.

Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (pin 1) set the TC170 peak current limit (Figure 1). The potential at pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for $(V_{REF} - 0.35)/R1 < 50\mu A$ and is latched for currents greater than 125µA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.15.

I_{PCL}, the peak current limit, is the current that causes the PWM comparator noninverting input to exceed V1, the potential at the inverting input. Once the comparator trip point is exceeded, both outputs are disabled.

I_{PCL} is easily calculated:

$$I_{PCL} = \frac{V1 - 0.75V}{3.15\ (RS)}$$

where:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

V_{REF} = Internal voltage reference = 5.1V

3.15 = Gain of current-sense amplifier

0.75V = Current limit offset

Both driver outputs (pins 11 and 14) are OFF (LOW) when the peak current limit is exceeded. When the sensed current goes below I_{PCL}, the circuit operates normally.

Output Shutdown

The TC170 outputs can be turned OFF quickly through the shutdown input (pin 16). A signal greater than 350 mV at pin 16 forces the shutdown comparator output HIGH. The PWM latch is held set, disabling the outputs.

Q2 is also turned ON. If $V_{REF}/R1$ is greater than 125µA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.75V. Q3 remains ON even after the shutdown input signal is removed, because of the positive feedback. The state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at pin 1 is below 0.75V.

The shutdown terminal gives a fast, direct way to disable the TC170 output transistors. System protection and remote shutdown applications are possible.

The input pulse to pin 16 should be at least 500 nsec wide and have an amplitude of at least 1V in order to get the minimum propagation delay from input to output. If these parameters are met, the delay should be less than 600nsec at 25°C; however, the delay time will increase as the device temperature rises.

Soft Restart From Shutdown

A soft restart can be programmed if nonlatched shutdown operation is used.

A capacitor at pin 1 will cause a gradual increase in potential toward V1. When the voltage at pin 1 reaches 0.75V, the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it is necessary to insert a capacitor between pin 1 and ground if the current I_L is greater than 125µA. This capacitor will prevent "noise triggering" of the latch, yet minimize the soft-start effect.

Soft-Start Power-Up

During power-up, a capacitor at R1, R2 initiates a soft-start cycle. As the input voltage (pin 15) exceeds the undervoltage lockout potential (7.7V), Q4 is turned OFF, ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.5V, both outputs are disabled.

When the undervoltage lockout level is passed, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current-Sense Amplifier

The current-sense amplifier operates at a fixed gain of 3.15. Maximum differential input voltage ($V_{PIN4} - V_{PIN3}$) is 1.1V. Common-mode input voltage range is 0V to $V_{IN} - 3V$.

Resistive-sensing methods are shown in Figure 2. In Figure 2(A), a simple RC filter limits transient voltage spikes at pin 4, caused by external output transistor-collector capacitance. Transformer coupling (Figure 3) offers isolation and better power efficiency, but cost and complexity increase.

In order to minimize the propagation delay from the input to the current amplifier to the output terminals, the current ramp should be in the order of 1 µs in width (min). Typical time delay values are in the 300 to 400nsec region at 25°C. The delay time increases with device temperature so that at 50°C, the delay times may be increased by as much as 100nsec.

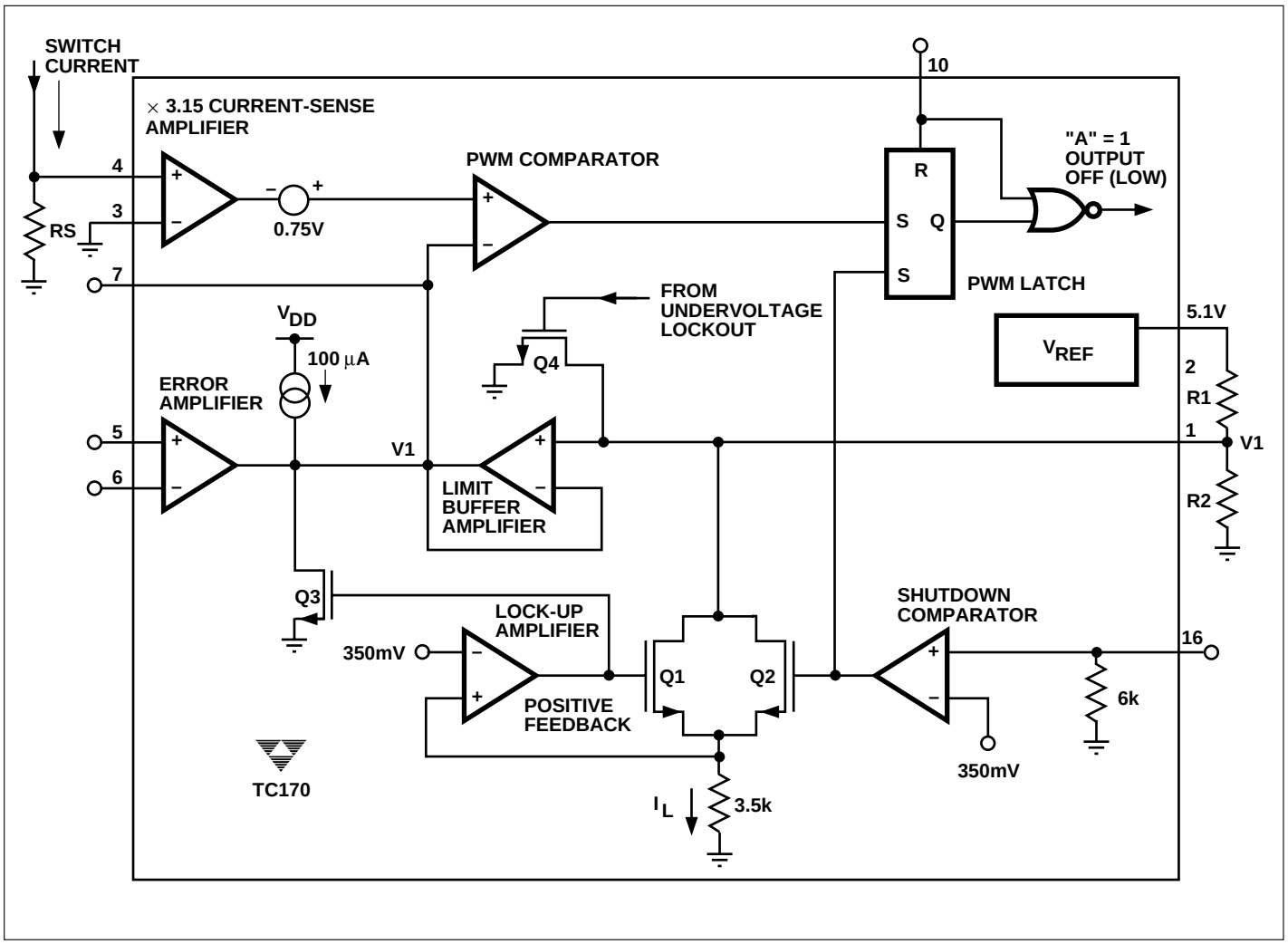


Figure 1. R1 and R2 Set Maximum Peak Output Current

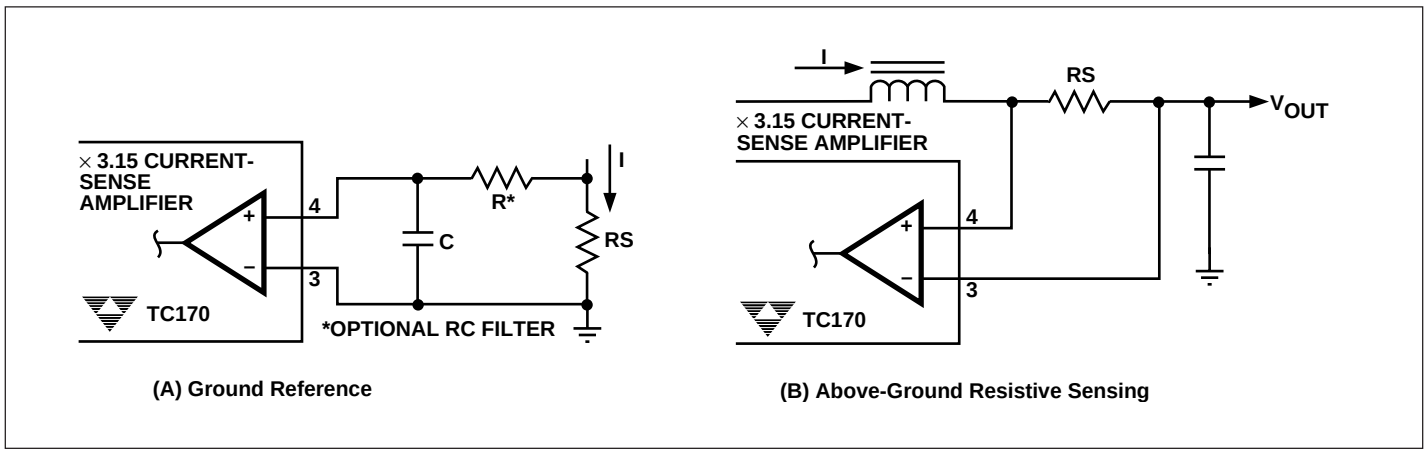


Figure 2. Resistive Sensing

TC170

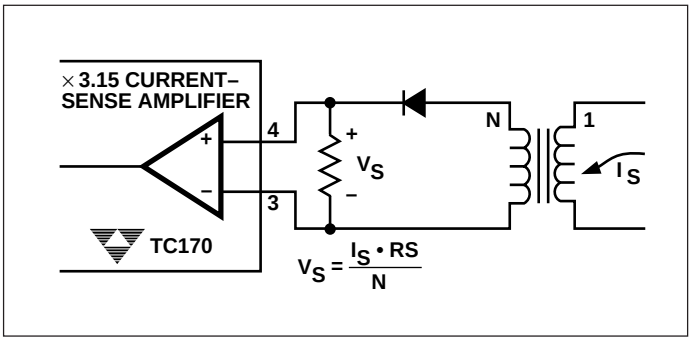


Figure 3 Transformer Isolated Current Sense

Undervoltage Lockout

The undervoltage lockout circuit forces the TC170 outputs OFF (low) if the supply voltage is below 7.7V. Threshold hysteresis is 0.75V and guarantees clean, jitter-free turn-on and turn-off points. The hysteresis also reduces capacitive filtering requirements at the PWM controller supply input (pin 15).

Circuit Synchronization

Current-mode-controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage-mode controllers unequally share the load current, decreasing system reliability.

Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding pin 8. Slave controllers derive an oscillator from the bidirectional synchronization output signal at pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver, a buffer is required (Figure 4). In order to use pin 10 as a sync input, it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_{IN}. Since V_{IN} must be above 8.25V for the undervoltage lockout to be disabled, a CMOS or open-collector TTL driver should be used.

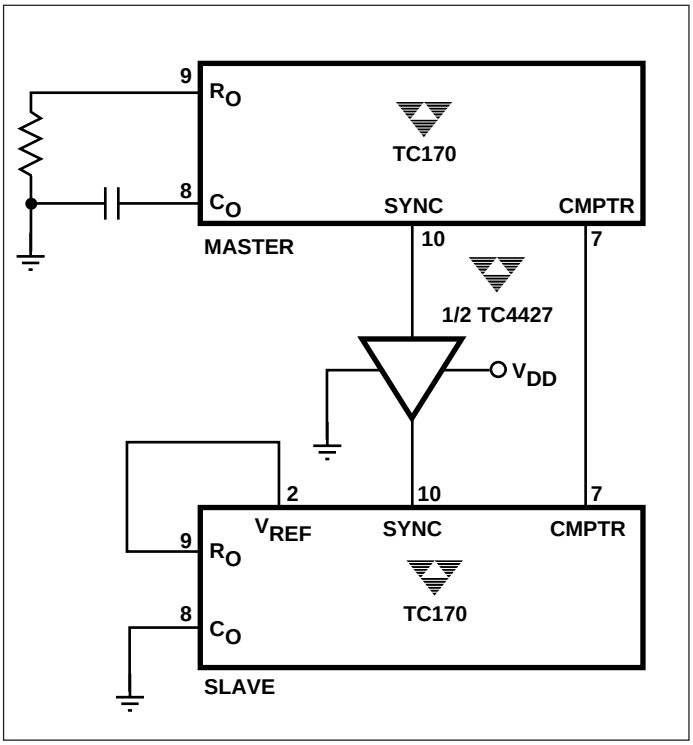


Figure 4. Master/Slave Parallel Operation

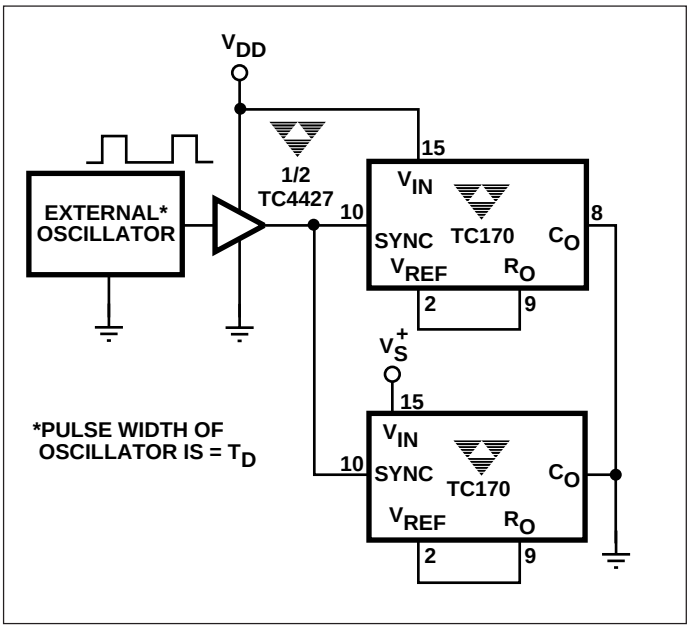


Figure 5. External Clock Synchronization

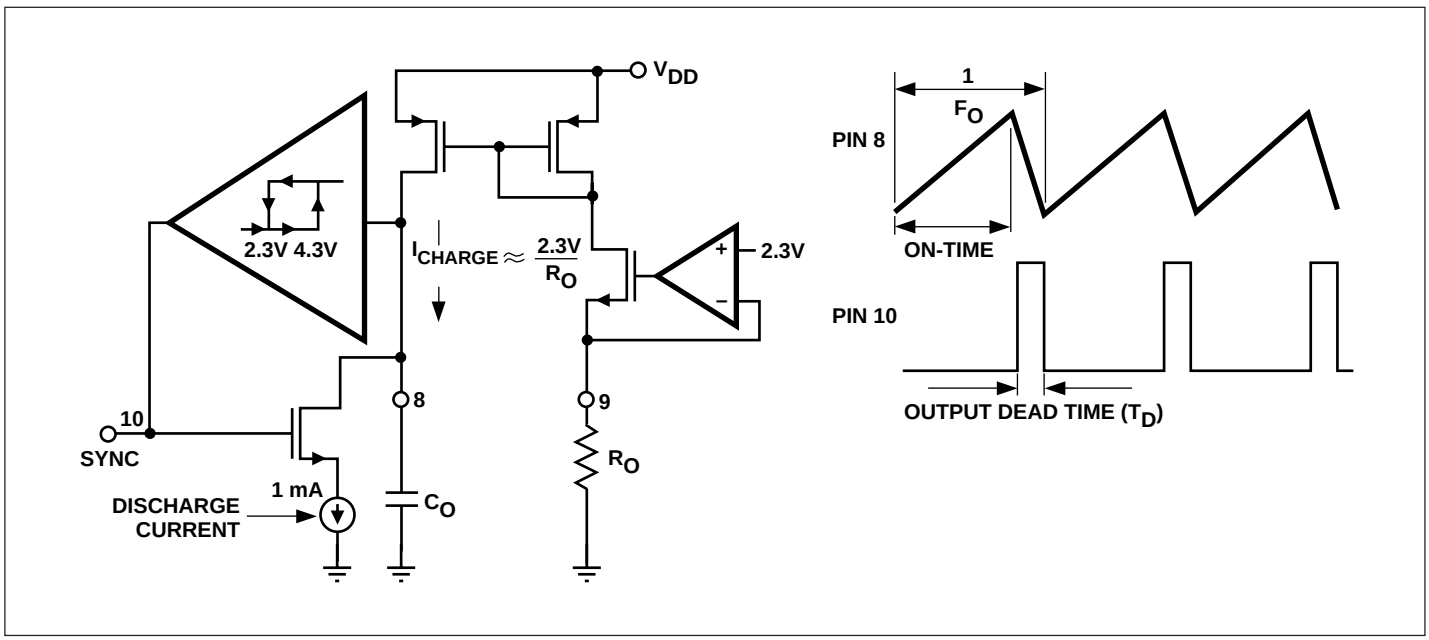


Figure 6 . Oscillator Circuit

Oscillator Frequency and Output Dead Time

The oscillator frequency for R_O = 24kΩ and C_O = 1000pF is:

$$F_O = \left[\frac{1.27}{R_O C_O} - \frac{2800}{R_O^2 C_O} \right] \frac{C_O}{C_O + 150 \times 10^{-12}}$$

where: R_O = Oscillator Resistor (Ω)
C_O = Oscillator Capacitor (F)
F_O = Oscillator Frequency (Hz)

The oscillator resistor can range from 5 kΩ to 50 kΩ.

Oscillator capacitor can range from 250 pF to 1000 pF. Figure 7 shows typical operation for various resistance and capacitance values.

During transitions between the two outputs, simultaneous conduction is prevented. Oscillator fall time controls the output off, or dead time (Figure 6).

Dead time is approximately:

$$T_D = \frac{2000\,[C_O]}{1 - \left(\frac{2.3}{R_O}\right)}$$

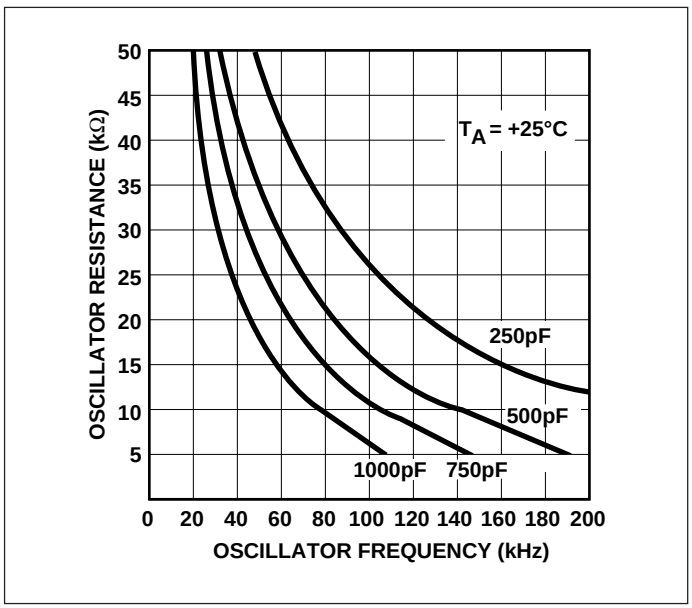


Figure 7. Oscillator Frequency vs Oscillator Resistance

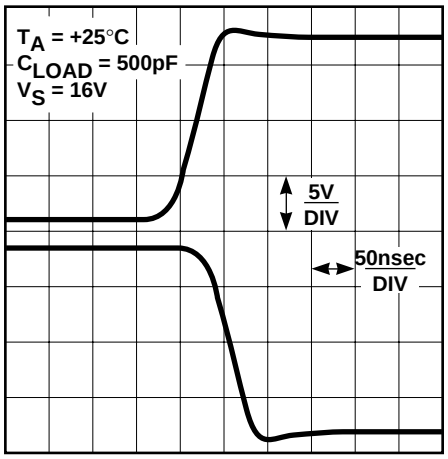
where: R_O = Oscillator Resistor (kΩ)
C_O = Oscillator Capacitor (pF)
T_D = Output Dead Time (sec)

Maximum possible duty cycle is set by the dead time.

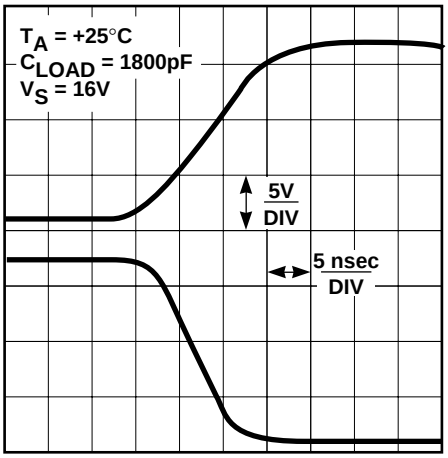
TC170

TYPICAL CHARACTERISTICS

Output Rise and Fall Times



Output Rise and Fall Times



Output Rise and Fall Times