

+5V TO $\pm 10V$ VOLTAGE CONVERTER

FEATURES

- 99% Voltage Conversion Efficiency
- 85% Power Conversion Efficiency
- Wide Voltage Range +2.0V to +5.5V
- Only 4 External Capacitors Required
- Space Saving 8-Pin SOIC Design

APPLICATIONS

- $\pm 10V$ From +5V Logic Supply
- $\pm 6V$ From a 3V Lithium Cell
- Handheld Instruments
- Portable Cellular Phones
- LCD Display Bias Generator
- Panel Meters
- Operational Amplifier Power Supplies

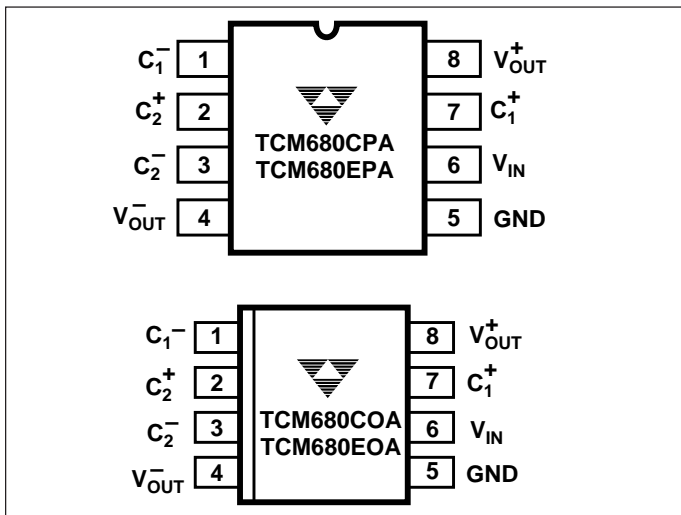
GENERAL DESCRIPTION

The TCM680 is a dual charge pump voltage converter that develops output voltages of $+2V_{IN}$ and $-2V_{IN}$ from a single input voltage of +2.0V to +5.5V. Common applications include $\pm 10V$ from a single +5V logic supply, and $\pm 6V$ from a +3V lithium battery.

The TCM680 is packaged in a space-saving 8-pin SOIC package and requires only four inexpensive external capacitors. The charge pumps are clocked by an on-board 8kHz oscillator. Low output source impedances (typically 150Ω) provides maximum output currents of 10mA for each output. Typical power conversion efficiency is 85%.

High efficiency, small installed size and low cost make the TCM680 suitable for a wide variety of applications that need both positive and negative power supplies derived from a single input voltage.

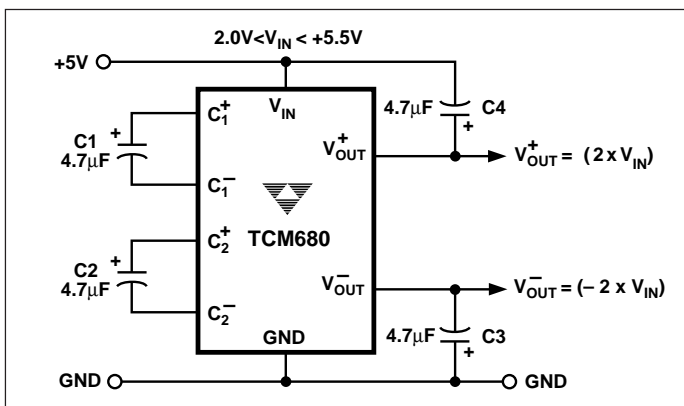
PIN CONFIGURATIONS (DIP AND SOIC)



ORDERING INFORMATION

Part No.	Package	Temperature
TCM680COA	8-Pin SOIC	0°C to +70°C
TCM680CPA	8-Pin Plastic DIP	0°C to +70°C
TCM680EOA	8-Pin SOIC	-40°C to +85°C
TCM680EPA	8-Pin Plastic DIP	-40°C to +85°C
TC7660EV	Charge Pump Family	
	Evaluation Kit	

TYPICAL OPERATING CIRCUIT



+5V TO $\pm 10V$ VOLTAGE CONVERTER

TCM680

ABSOLUTE MAXIMUM RATINGS*

V_{IN}	+6.0V
V_{OUT}^+	+12.0V
V_{OUT}^-	- 12.0V
V_{OUT}^- Short-Circuit Duration	Continuous
V_{OUT}^+ Current	75mA
V_{IN} dV/dT	1V/ μ sec

Power Dissipation ($T_A \leq 70^\circ\text{C}$)

Plastic DIP	730mW
Small Outline	470mW
Storage Temperature	- 65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

*Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or other conditions above those indicated in the operation section of the specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{IN} = +5V$, $T_A = +25^\circ\text{C}$, test circuit Figure 1, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Supply Voltage Range	MIN. $\leq T_A \leq$ MAX., $R_L = 2k\Omega$	2.0	1.5 to 5.5	5.5	V
	Supply Current	$V_{IN} = 3V$, $R_L = \infty$ $V_{IN} = 5V$, $R_L = \infty$ $V_{IN} = 5V$, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, $R_L = \infty$ $V_{IN} = 5V$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, $R_L = \infty$	—	0.5 1 — —	1 2 2.5 3	mA
	Negative Charge Pump Output Source Resistance	$I_L^- = 10\text{mA}$, $I_L^+ = 0\text{mA}$, $V_{IN} = 5V$ $I_L^- = 5\text{mA}$, $I_L^+ = 0\text{mA}$, $V_{IN} = 2.8V$ $I_L^- = 10\text{mA}$, $I_L^+ = 0\text{mA}$, $V_{IN} = 5V$: $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	140 180 — —	180 250 220 250	Ω
	Positive Charge Pump Output Source Resistance	$I_L^+ = 10\text{mA}$, $I_L^- = 0\text{mA}$, $V_{IN} = 5V$ $I_L^+ = 5\text{mA}$, $I_L^- = 0\text{mA}$, $V_{IN} = 2.8V$ $I_L^+ = 10\text{mA}$, $I_L^- = 0\text{mA}$, $V_{IN} = 5V$: $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	140 180 — —	180 250 220 250	Ω
F_{OSC}	Oscillator Frequency		—	21	—	kHz
P_{EFF}	Power Efficiency	$R_L = 2k\Omega$	—	85	—	%
$V_{OUT} E_{FF}$	Voltage Conversion Efficiency	V_{OUT}^+ , $R_L = \infty$ V_{OUT}^- , $R_L = \infty$	97 97	99 99	— —	%

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PIN DESCRIPTION

8-Pin		
DIP/SOIC	Symbol	Description
1	C_1^-	Input. Capacitor C1 negative terminal.
2	C_2^+	Input. Capacitor C2 positive terminal.
3	C_2^-	Input. Capacitor C2 negative terminal.
4	V_{OUT}^-	Output. Negative output voltage ($-2V_{IN}$).
5	GND	Input. Device ground.
6	V_{IN}	Input. Power supply voltage.
7	C_1^+	Input. Capacitor C1 positive terminal.
8	V_{OUT}^+	Output. Positive output voltage ($+2V_{IN}$).

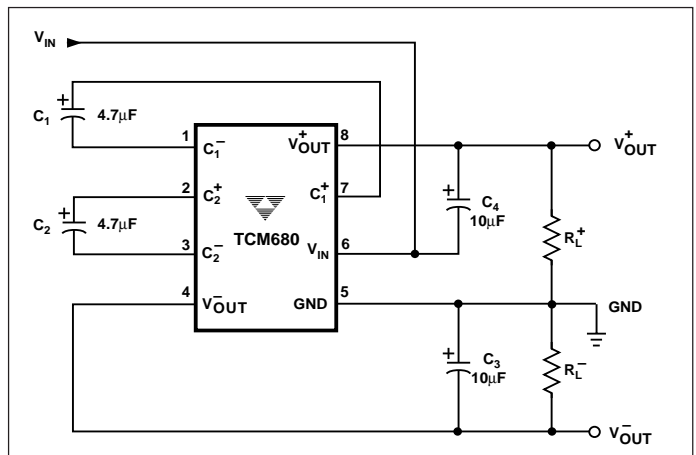


Figure 1. Test Circuit

DETAILED DESCRIPTION

Phase 1

V_{SS} charge storage – The positive side of capacitors C₁ and C₂ are connected to +5V at the start of this phase. C₁⁺ is then switched to ground and the charge in C₁ is transferred to C₂⁻. Since C₂⁺ is connected to +5V, the voltage potential across capacitor C₂ is now 10V.

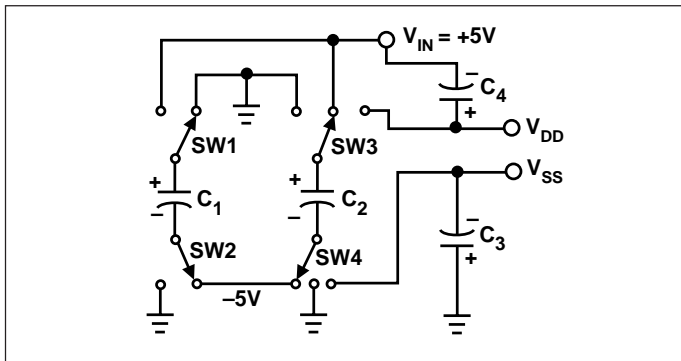


Figure 2. Charge Pump – Phase 1

Phase 2

V_{SS} transfer – Phase two of the clock connects the negative terminal of C₂ to the V_{SS} storage capacitor C₃ and the positive terminal of C₂ to ground, transferring the generated –10V to C₃. Simultaneously, the positive side of capacitor C₁ is switched to +5V and the negative side is connected to ground.

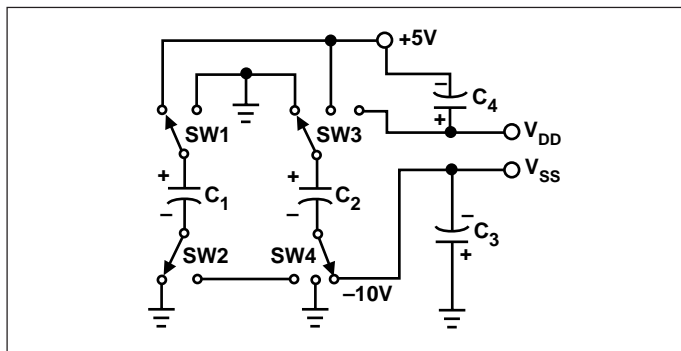


Figure 3. Charge Pump – Phase 2

Phase 3

V_{DD} charge storage – The third phase of the clock is identical to the first phase – the charge transferred in C₁ produces –5V in the negative terminal of C₁, which is applied to the negative side of capacitor C₂. Since C₂⁺ is at +5V, the voltage potential across C₂ is 10V.

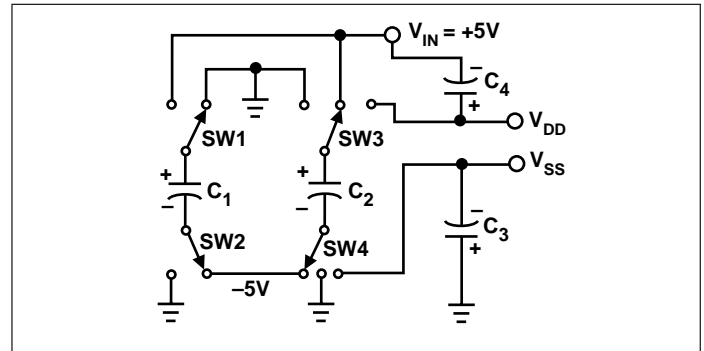


Figure 4. Charge Pump – Phase 3

Phase 4

V_{DD} transfer – The fourth phase of the clock connects the negative terminal of C₂ to ground, and transfers the generated 10V across C₂ to C₄, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C₁ is switched to +5V and the negative side is connected to ground, and the cycle begins again.

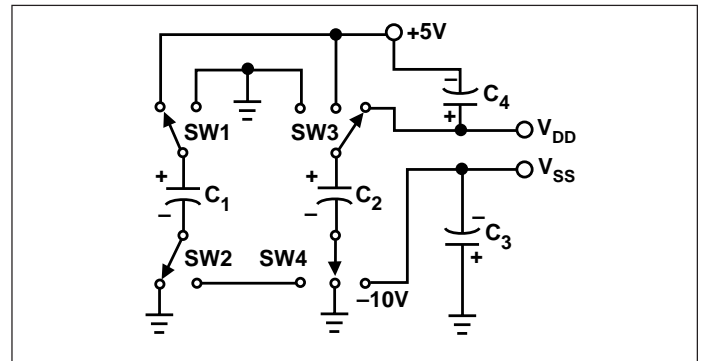


Figure 5. Charge Pump – Phase 4

MAXIMUM OPERATING LIMITS

The TCM680 has on-chip zener diodes that clamp V_{IN} to 5.8V, V_{OUT}⁺ to 11.6V, and V_{OUT}⁻ to –11.6V. Never exceed the maximum supply voltage or excessive current will be shunted by these diodes, potentially damaging the chip. The TCM680 will operate over the entire operating temperature range with an input voltage of 2V to 5.5V.

TCM680

EFFICIENCY CONSIDERATIONS

Theoretically a charge pump can approach 100% efficiency under the following conditions:

- The charge Pump switches have virtually no offset and extremely low on resistance
- Minimal power is consumed by the drive circuitry
- The impedances of the reservoir and pump capacitors are negligible

For the TCM680, efficiency is as shown below:

$$\begin{aligned} \text{Efficiency } V^+ &= V_{DD} / (2V_{IN}) \\ V_{DD} &= 2V_{IN} - V_{DROD}^+ \\ V_{DROD}^+ &= (I_{OUT}^+)(R_{OUT}^+) \end{aligned}$$

$$\begin{aligned} \text{Efficiency } V^- &= V_{SS} / (-2V_{IN}) \\ V_{SS} &= 2V_{IN} - V_{DROD}^- \\ V_{DROD}^- &= (I_{OUT}^-)(R_{OUT}^-) \end{aligned}$$

$$\text{Power Loss} = (V_{DROD}^+)(I_{OUT}^+) + (V_{DROD}^-)(I_{OUT}^-)$$

There will be a substantial voltage difference between $(V_{OUT}^+ - V_{IN})$ and V_{IN} for the positive pump and between V_{OUT}^+ and V_{OUT}^- if the impedances of the pump capacitors C_1 and C_2 are high with respect to the output loads.

Larger values of reservoir capacitors C_3 and C_4 will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency. See "Capacitor Selection" in Applications Section.

APPLICATIONS

Positive and negative Converter

The most common application of the TCM680 is as a dual charge pump voltage converter which provides positive and negative outputs of two times a positive input voltage. The simple circuit of Figure 6 performs this same function using the TCM680 and external capacitors, C_1 , C_2 , C_3 and C_4 .

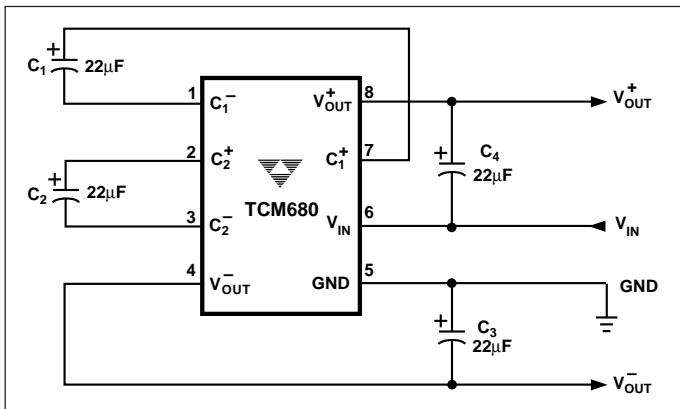


Figure 6. Positive and Negative Converter

Capacitor Selection

The TCM680 requires only 4 external capacitors for operation. These can be inexpensive polarized aluminum electrolytic types. For the circuit in Figure 6 the output characteristics are largely determined by the external capacitors. An expression for R_{OUT} can be derived as shown below:

$$\begin{aligned} R_{OUT}^+ &= 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) \\ &\quad + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) \\ &\quad + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C4} \end{aligned}$$

$$\begin{aligned} R_{OUT}^- &= 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) \\ &\quad + 4(R_{SW1} + R_{SW2} + ESR_{C1} + R_{SW3} + R_{SW4} + ESR_{C2}) \\ &\quad + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) + ESR_{C3} \end{aligned}$$

Assuming all switch resistances are approximately equal...

$$\begin{aligned} R_{OUT}^+ &= 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C4} \\ &\quad + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) \end{aligned}$$

$$\begin{aligned} R_{OUT}^- &= 32R_{SW} + 8ESR_{C1} + 8ESR_{C2} + ESR_{C3} \\ &\quad + 1/(f_{PUMP} \times C1) + 1/(f_{PUMP} \times C2) \end{aligned}$$

R_{OUT} is typically 140Ω at $+25^\circ\text{C}$ with $V_{IN} = +5\text{V}$ and $C1$ and $C2$ as $4.7\mu\text{F}$ low ESR capacitors. The fixed term ($32R_{SW}$) is about 130Ω . It can be seen easily that increasing or decreasing values of $C1$ and $C2$ will affect efficiency by changing R_{OUT} . However, be careful about ESR. This term can quickly become dominant with large electrolytic capacitors. Table 1 shows R_{OUT} for various values of $C1$ and $C2$ (assume 0.5Ω ESR). $C1$ and $C4$ must be rated at 6VDC or greater while $C2$ and $C3$ must be rated at 12VDC or greater.

Output voltage ripple is affected by $C3$ and $C4$. Typically the larger the value of $C3$ and $C4$ the less the ripple for a given load current. The formula for $V_{RIPPLE(p-p)}$ is given below:

$$\begin{aligned} V_{RIPPLE(p-p)} &= \{1/[2(f_{PUMP}/3) \times C4] + 2(ESR_{C4})\}(I_{OUT}^+) \\ V_{RIPPLE(p-p)} &= \{1/[2(f_{PUMP}/3) \times C3] + 2(ESR_{C3})\}(I_{OUT}^-) \end{aligned}$$

For a $10\mu\text{F}$ (0.5Ω ESR) capacitor for $C3$, $C4$, $f_{PUMP} = 21\text{kHz}$ and $I_{OUT} = 10\text{mA}$ the peak-to-peak ripple voltage at the output will be less than 100mV . In most applications ($I_{OUT} \leq 10\text{mA}$) $10\text{-}20\mu\text{F}$ output capacitors and $1\text{-}5\mu\text{F}$ pump capacitors will suffice. Table 2 shows V_{RIPPLE} for different values of $C3$ and $C4$ (assume 1Ω ESR).

Table 1. R_{OUT} vs. C₁, C₂

C ₁ , C ₂ (μF)	R _{OUT} (Ω)
0.1	1089
0.47	339
1	232
3.3	165
4.7	157
10	146
22	141
100	137

Table 2. V_{RIPPLE} (p-p) vs. C₃, C₄ (I_{OUT} = 10mA)

C ₃ , C ₄ (μF)	V _{RIPPLE} (mV)
0.47	1540
1	734
3.3	236
4.7	172
10	91
22	52
100	27

Paralleling Devices

Paralleling multiple TCM680s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure 7, each requires separate pump capacitors C₁ and C₂, but all can share a single set of reservoir capacitors.

±5V Regulated Supplies From A Single 3V Battery

Figure 8 shows a complete ±5V power supply using one 3V battery. The TCM680 provides +6V at V_{OUT}⁺, which is regulated to +5V by the TC55, and -5V by the negative LDO. The input to the TCM680 can vary from 3V to 6V without affecting regulation appreciably. With higher input voltage, more current can be drawn from the outputs of the TCM680. With 5V at V_{IN}, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150Ω source resistance for both converters, with (I_L⁺ + I_L⁻) = 20mA, the positive charge pump will droop 3V, providing +7V for the negative charge pump.

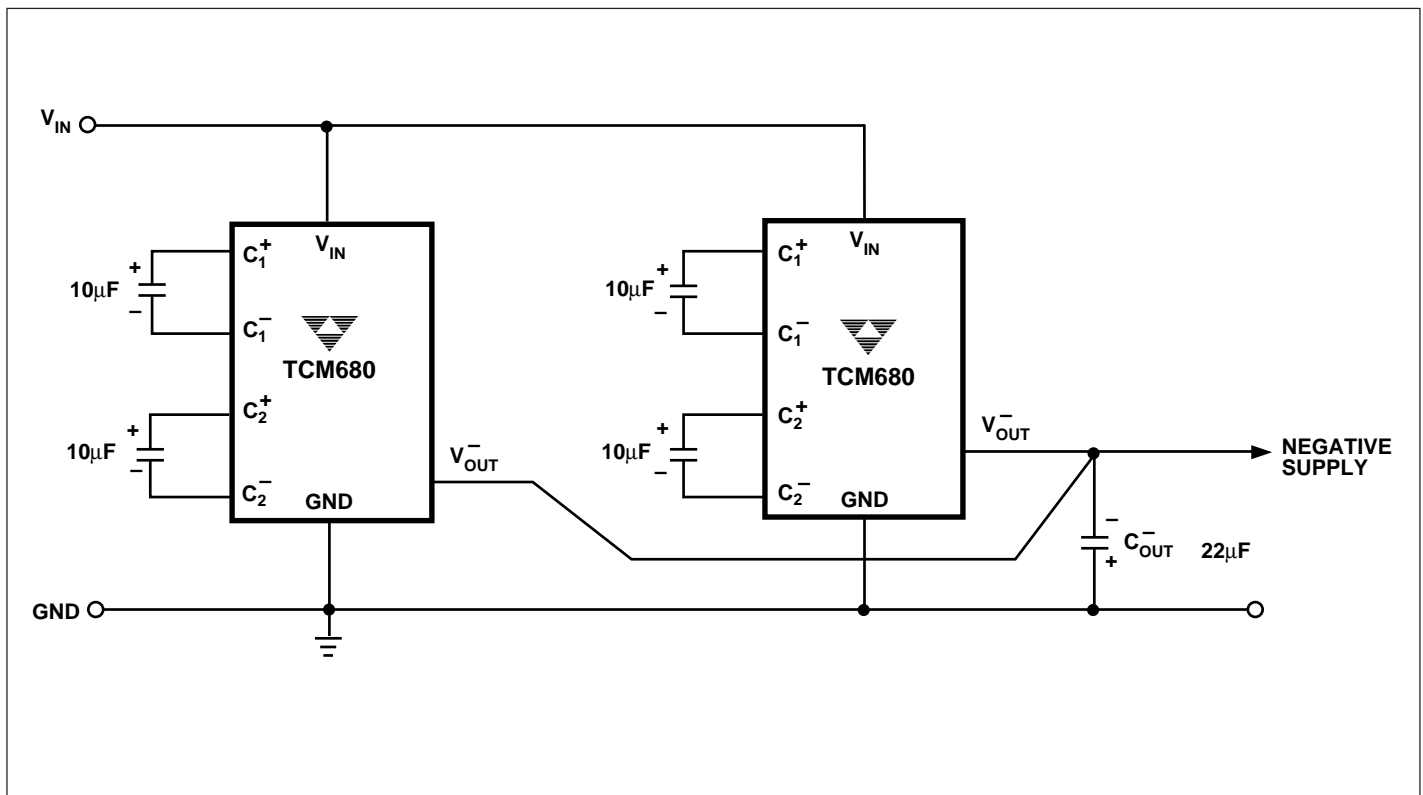


Figure 7. Paralleling TCM680 for Lower Output Source Resistance

TCM680

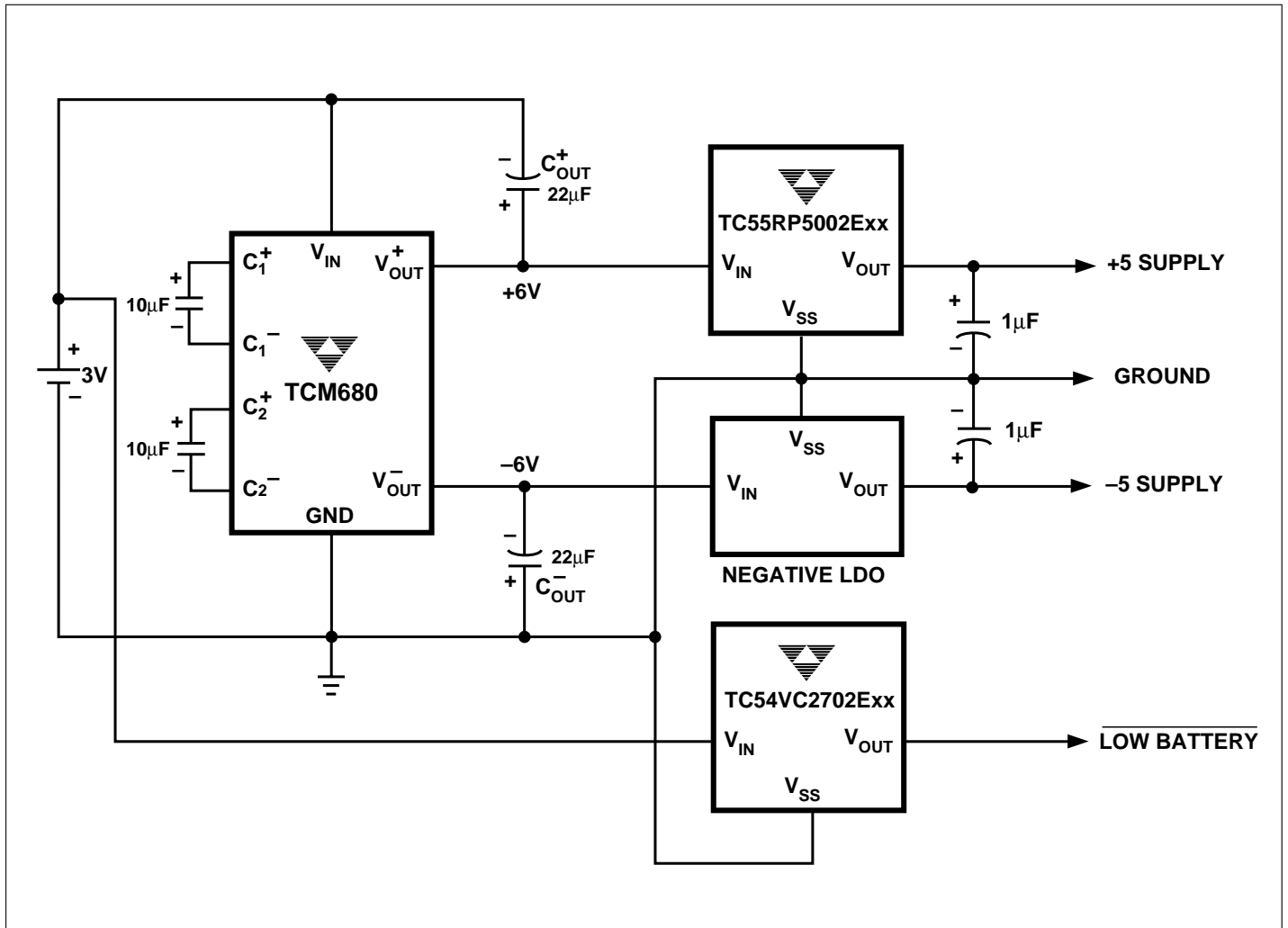
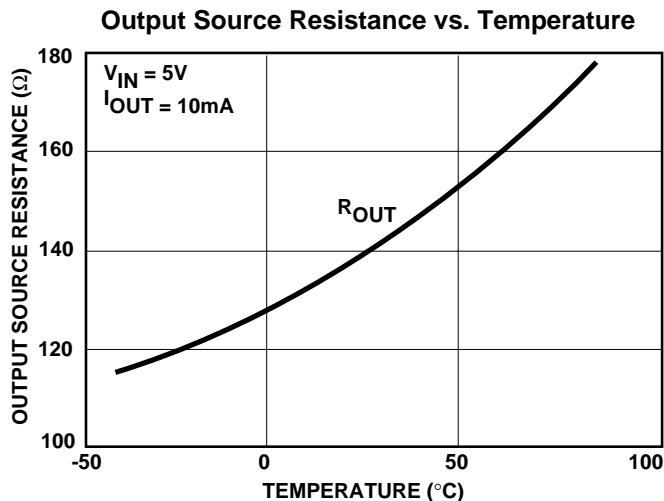
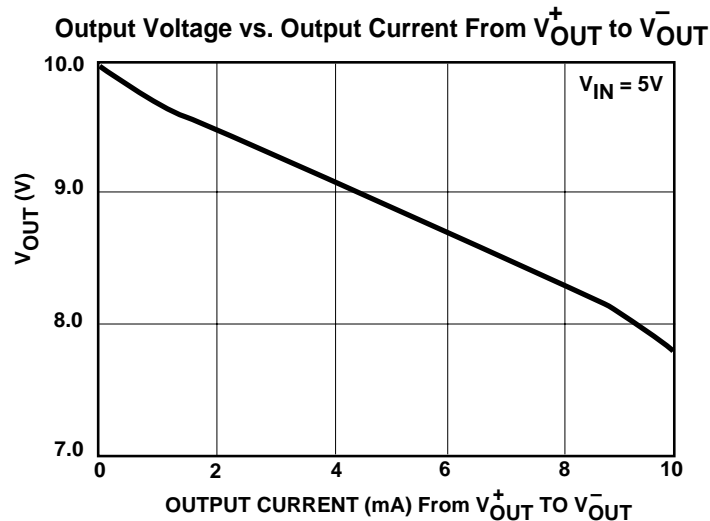
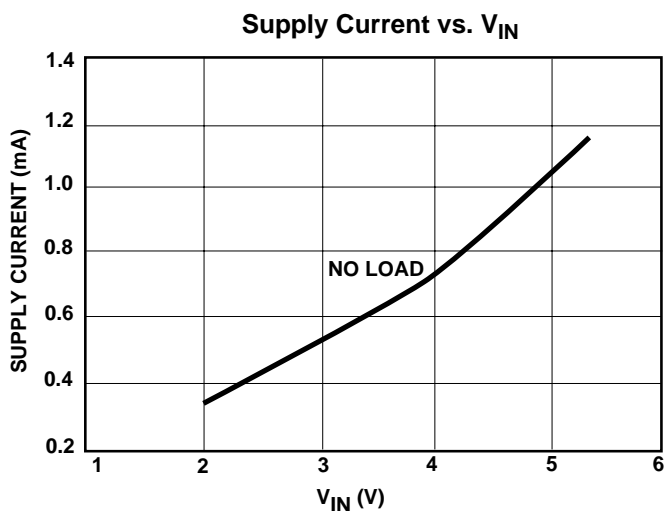
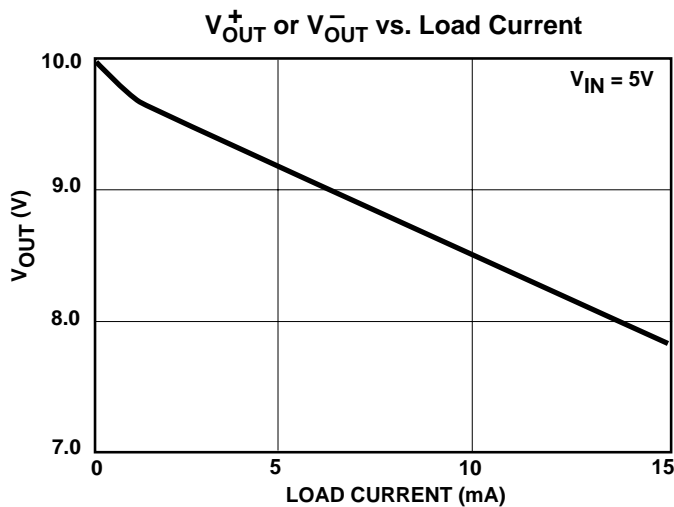
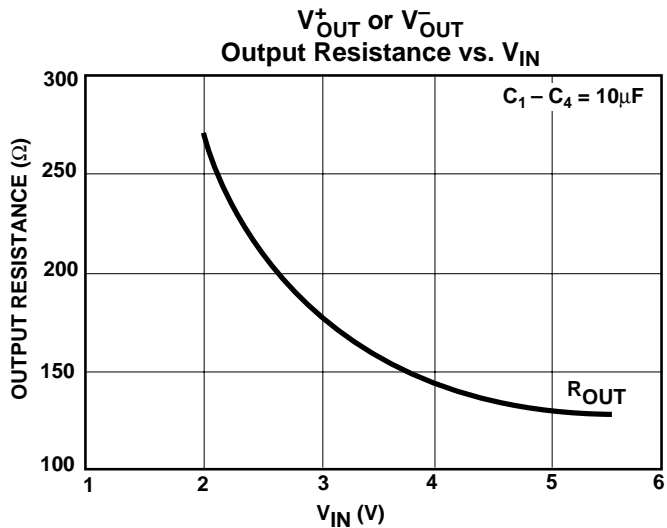


Figure 8. Split Supply Derived from 3V Battery

TYPICAL CHARACTERISTICS



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