MICROMASTER™ – SYSTEM SUPERVISOR WITH POWER SUPPLY MONITOR, WATCHDOG AND BATTERY BACKUP

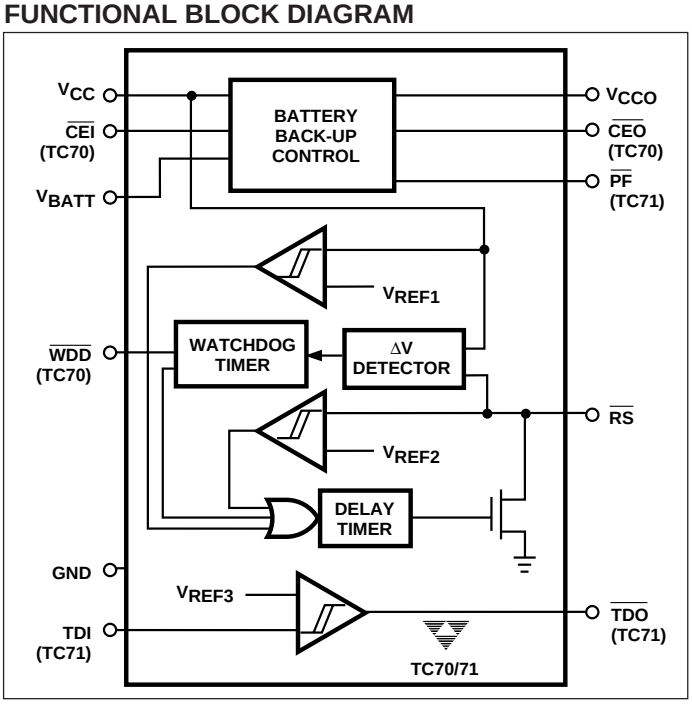
FEATURES

- **Maximum Functional Integration: Precision Power Supply Monitor, Watchdog Timer, External RESET Override, Threshold Detector and Battery Backup Controller in an 8-Pin Package**
- **Generates Power-on RESET and Guards Against Unstable Processor Operation Resulting from Power "Brown-out"**
- **Automatically Halts and Restarts an Out-of-Control Microprocessor**
- **Output Can be Wire-ORed, or Hooked to Manual RESET Pushbutton Switch**
- **Watchdog Disable Pin for Easier Prototyping (TC70)**
- **Voltage Monitor for Power Fail or Low Battery Warning (TC71)**
- **Available in 8-Pin Plastic DIP or 8-Pin SOIC Packages**
- **Cost Effective**

TYPICAL APPLICATIONS

- **All Microprocessor-based Systems**
- **Test Equipment**
- **Instrumentation**
- **Set-Top Boxes**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The TC70/71 is a fully-integrated power supply monitor, watchdog and battery backup circuit in a space-saving 8-pin package.

When power is initially applied, the TC70/71 holds the processor in its reset state for a minimum of 500msec after V_{CC} is in tolerance to ensure stable system start-up. After start-up, processor sanity is monitored by the on-board watchdog circuit. The processor must provide periodic high-to-low level transitions to the TC70/71 to verify proper execution. Should the processor fail to supply this signal within the specified timeout period, an out-of-control processor is indicated and the TC70/71 issues a momentary processor reset as a result. The TC70 also features a watchdog disable pin to facilitate system test and debug.

The output of the TC70/71 can be wire-ORed to a push-button switch (or electronic signal) to reset the processor. When connected to a push-button switch, the TC70/71 provides contact debounce.

The integrated battery backup circuit on-board the TC70/71 converts CMOS RAM into nonvolatile memory by first write-protecting, then switching the V_{CC} line of the RAM over to an external battery.

The TC71 incorporates an additional 1.3V threshold detector for power fail warning, low battery detection or to monitor power supply voltages other than +5V.

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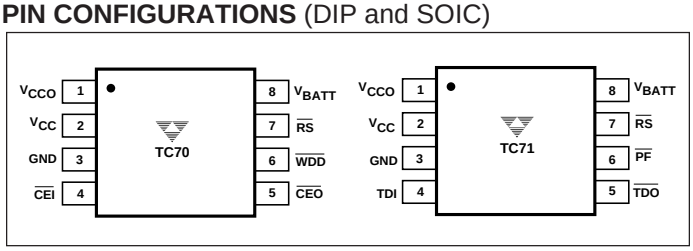
ORDERING INFORMATION

Part No.	Package	Temp. Range
TC70COA	8-Pin SOIC	0°C to +70°C
TC70CPA	8-Pin Plastic DIP	0°C to +70°C
TC70EOA	8-Pin SOIC	– 40°C to +85°C
TC70EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC71COA	8-Pin SOIC	0°C to +70°C
TC71CPA	8-Pin Plastic DIP	0°C to +70°C
TC71EOA	8-Pin SOIC	– 40°C to +85°C
TC71EPA	8-Pin Plastic DIP	– 40°C to +85°C

PIN CONFIGURATIONS (DIP and SOIC)



TC70/71-1 11/18/96

ABSOLUTE MAXIMUM RATINGS*

Voltage (Any Pin) with Respect to Ground ..... GND – 0.3 to V_{CC} + 0.3V
Operating Temperature Range ..... – 40°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

Recommended DC Operations: $T_A = T_{MIN}$ to T_{MAX}, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Note 1	4.5	5.0	5.5	V
V_{IH}	Input HIGH Level	$\overline{CEI}$, $\overline{WDD}$ (Note 1)	2.5	—	—	V
V_{IH}	Input HIGH Level	$\overline{RS}$ (Note 1)	2.2	—	—	V
V_{IL}	Input LOW Level	$\overline{CEI}$, $\overline{WDD}$, $\overline{RS}$ (Note 1)	—	—	0.8	V

ELECTRICAL CHARACTERISTICS:

DC: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{CC1}	Operating Current	Notes 2, 3	—	5	6.5	mA
I_{CC2}	Operating Current in Battery Backup Mode	V_{CC} = 0; V_{BATT} = 2.8V; (Note 3)	—	0.01	0.20	µA
I_{IH}	Input Leakage	$\overline{CEI}$	—	4	7	µA
I_{IL}	Input Leakage	$\overline{CEI}$	—	1	—	µA
I_{IH}	Input Leakage	$\overline{RS}$	—	1	—	µA
I_{STBY}	Battery Standby Current	5.5V > V_{CC} > V_{BATT} + 0.2V	– 1.0	—	0.02	µA
I_{STBY}	Battery Standby Current	5.5V > V_{CC} > V_{BATT} + 0.2V T_A = 25°C	– 0.1	—	0.02	µA

ELECTRICAL CHARACTERISTICS:

DC: Power Supply Monitor, EXT. RESET and Watchdog: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Output Current 0.4V ($\overline{RS}$, $\overline{TDO}$, $\overline{CEO}$, $\overline{PF}$ Pins)	V_{OL} = 0.4V	2	5	—	mA
I_{OH}	Output Current 2.4V ($\overline{TDO}$, $\overline{CEO}$, $\overline{PF}$ Pins)	V_{OH} = 2.4V	2	3	—	mA
WDD_I	$\overline{WDD}$ Input Current	WDD = GND WDD = V_{CC}	– 120 —	— —	— 25	µA
V_{STH}	$\overline{RS}$ Strobe (HIGH) Level	Figure 3 (Note 1)	V_{DD} – 0.5	—	—	V
V_{STL}	$\overline{RS}$ Strobe (LOW) Level	Figure 3 (Note 1)	2.2	—	V_{DD} – 1.8	V
V_{CCTRIP}	V_{CC} Trip Point	(Note 1) 0°C ≤ T_A ≤ 70°C – 40°C ≤ T_A ≤ 85°C	4.25 4.20	—	4.49 4.49	

ELECTRICAL CHARACTERISTICS:

DC: Battery Backup and Threshold Detector: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OUT1}	V_{CCO} Output Voltage	I_{OUT} = 1mA I_{OUT} = 50mA	V_{CC} – 0.3 V_{CC} – 0.5	V_{CC} – 0.1 V_{CC} – 0.20	— —	V
V_{OUT2}	V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT} – 0.2, V_{BATT} = 2.8V	V_{BATT} – 0.1	V_{BATT} – 0.02	—	V

ELECTRICAL CHARACTERISTICS: (Cont.)

DC: Battery Backup and Threshold Detector: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OUT1}	V_{CCO} Output Current	V_{CC} = 4.5V, V_{CCO} = 3.5V	50	100	—	mA
I_{OUT2}	V_{CCO} Output Current in Battery Backup Mode	$V_{CCO} = V_{BATT} – 0.3V$ V_{BATT} = 2.8V	500	—	—	µA
V_{SW}	Battery Switchover Threshold (V_{CC} Falling)		—	$V_{BATT} – 0.01$	—	V
V_{HYST}	Battery Switchover Hysteresis		—	20	—	mV
$VOH_{\overline{CEO}}$	$\overline{CEO}$ Output Voltage in Battery Backup Mode	$V_{CC} < V_{BATT} – 0.2$, V_{BATT} = 2.8V I_{OH} = 10µA	$V_{BATT} – 0.2$	—	—	V
V_{TDI}	Threshold Detector Trip Voltage		1.2	—	1.4	V
I_{TDI}	Threshold Detector Input Current	T_A = 25°C	–25	—	+25	nA
$V_{TDI\ (HYST)}$	Threshold Detector Hysteresis		—	10	—	mV

ELECTRICAL CHARACTERISTICS:

AC: Power Supply Monitor, EXT. RESET and Watchdog: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PBH}	PB Hold Time	Figure 4 (Note 4)	20	—	—	msec
t_{RST}	Reset Active Time	Figure 6	500	—	900	msec
t_{ST}	$\overline{RS}$ STROBE Pulsewidth	Figure 3	500	—	—	nsec
t_{TD}	Watchdog Timeout Period	Figure 3	500	700	900	msec
t_{RPD}	V_{CC} Detect to $\overline{RS}$ LOW	Figure 6	—	—	100	nsec

ELECTRICAL CHARACTERISTICS:

AC: Battery Backup and Threshold Detector: $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 4.5V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PD}	CE Propagational Delay	Figure 7	—	—	50	nsec

ELECTRICAL CHARACTERISTICS:

AC: $T_A = T_{MIN}$ to T_{MAX}.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_F	V_{CC} Fall Time From 4.25V to 3.0V	Figure 5 (Note 1)	10	—	—	µsec
t_R	V_{CC} Rise Time From 3.0V to 4.25V	Figure 5 (Note 1)	0	—	—	µsec

NOTES: 1. All voltages referenced to ground.
2. No output load.
3 Measured with V_{CCO} and $\overline{CEO}$ open.
4. The $\overline{RS}$ output must be held low for a minimum of 20msec to guarantee a reset.

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PIN DESCRIPTION

Pin No (TC70)	Pin No (TC71)	Symbol	Description
1	1	V_{CCO}	V_{CC} Output. The higher of V_{CC} or V_{BATT} is internally switched to this output. Connect to V_{CC} if V_{BATT} and V_{CCO} are not used.
2	2	V_{CC}	V_{CC} Input. +5V power supply.
3	3	GND	GND Input. Ground.
4	–	$\overline{CEI}$	Chip enable input. Chip enable to static RAM or other device to be battery backed-up. Connect to ground if V_{CCO} is not used.
–	4	TDI	Threshold detector input. When the voltage on threshold detector input (TDI) is less than 1.3V, threshold detector output ($\overline{TDO}$) goes low.
5	–	$\overline{CEO}$	Chip enable output. This line goes low only when $\overline{CEI}$ is low and V_{CC} is above the RESET threshold.
–	5	$\overline{TDO}$	Threshold detector output. $\overline{TDO}$ goes low when TDI is less than 1.3V and V_{CC} is greater than V_{BATT}. (The threshold detector is turned off when V_{CC} is less than V_{BATT}.
6	–	$\overline{WDD}$	Watchdog disable input. Grounding this line disables the watchdog timer (no RESET pulses are generated after the watchdog timer times out). This input is provided to facilitate system debug. This input is internally pulled-up and can be left open, or tied to V_{CC} for normal watchdog operation.
–	6	$\overline{PF}$	Power fail output. This line goes low when V_{CC} is below 4.5V nominal. It is used to write-protect the external device to be battery backed.
7	7	$\overline{RS}$	$\overline{RESET/STORE}$ (Bidirectional). An open drain with pull-up (in output mode) that goes active if: 1. V_{CC} falls below 4.5V nominal 2. If pulled low by an external electronic signal or switch closure 3. If the watchdog is not strobed within the minimum watchdog timeout period 4. During power-up and power down In the input mode, $\overline{RS}$ is a negative edge triggered input that resets the watchdog timer when pulled to ground through a 10kΩ, 5% tolerance resistor.
8	8	V_{BATT}	Backup battery input. Connect to ground if battery backup is not used.

DETAILED DESCRIPTION

Precision Power Supply Monitor

The $\overline{RS}$ pin is immediately driven low any time V_{CC} is below 4.5V nominal. The processor is held in its reset state during power-up and power-down. $\overline{RS}$ remains low for a minimum of 500msec after V_{CC} is within tolerance to allow the power supply and processor to stabilize.

Watchdog Timer

The processor drives the $\overline{RS}$ pin with an input/output (I/O) line in series with a voltage divider to V_{DD}. Pulling the bottom of this divider low results in an internal voltage change (strobe) sufficient to reset the watchdog timer, but above the V_{IL} input threshold of the processor $\overline{RESET}$ input. The processor must continuously apply strobes in this manner within a set period to verify proper software execution. A momentary reset (500msec minimum) is generated if a hardware or software failure keeps $\overline{RS}$ from being strobed within the watchdog timeout period. This action typically initiates the processor's power-up routine. If the interruption persists, new reset pulses are generated each timeout period until $\overline{RS}$ is strobed. The timeout period is typically 700msec.

It is often difficult to debug a system while the watchdog is continuously generating reset pulses. For example, the watchdog must be disabled when the system is operated with an in-circuit emulator (ICE). The watchdog disable input (TC70) is provided for system debugging, (or if the watchdog timer on-board the processor is to be used). Grounding $\overline{WDD}$ disables the watchdog (all other functions remain intact). For normal watchdog operation, $\overline{WDD}$ can be tied to V_{DD}.

The software routine that drives the $\overline{RS}$ strobe must be in a section of the program that executes frequently enough so the time between toggles is less than one watchdog timeout period. The strobe signal can be derived from microprocessor address, data and/or control signals. Typical circuit examples are shown in Figure 1.

Resistor Value Selection

The values of R1 and R2 must be chosen to ensure a valid low strobe level (V_{STL}) on $\overline{RS}$ when the processor I/O line is low. The use of 10kΩ, ±5% tolerance resistors are recommended. These values result in a nominal strobe level of 2.83V on $\overline{RS}$ (min/max of 2.43V/3.24V, assuming V_{DD} = 5.0V ±10%). Other resistor values can be used, so long as the additive tolerances of the power supply and resistor values result in a strobe that falls within V_{STH} and V_{STL} under all additive tolerance conditions.

External Override Reset Control

A built-in debounce circuit allows a pushbutton switch (or other electronic reset signal) to be wire-ORed to $\overline{RS}$ as an external reset override (Figure 4). The external reset signal is required to be an active low signal of at least 20msec in duration. Internally, this input is timed to provide a minimum reset pulse width output of 500msec.

Threshold Detector

The TC71 issues a low-true output on the $\overline{TDO}$ pin any time the TDI pin is less than 1.3V and V_{CC} is greater than V_{BATT}. The voltage to be monitored is connected to the TDI input through a simple resistor divider. The threshold detector can be used to generate an early power fail warning if the unregulated DC input to the +5V regulator is available for monitoring.

Integrated Battery Backup (TC70)

The $\overline{CEO}$ line (TC70) drives the $\overline{CE}$ input of a CMOS RAM or other device to be battery-backed. $\overline{CEO}$ follows $\overline{CEI}$ as long as V_{CC} is greater than 4.5V nominal. If V_{CC} falls below 4.5V nominal, $\overline{CEO}$ is driven to the potential of VCCO thus write protecting the RAM and preventing accidental data corruption during power up and power down. The battery switchover circuit compares V_{CC} to the V_{BATT} input and connects VCCO to whichever is higher. Switchover (V_{SW}) occurs when V_{CC} is 10mV below V_{BATT} as V_{CC} falls, and when V_{CC} is 10mV more than V_{BATT} as V_{CC} rises. The battery switchover comparator has 20mV of hysteresis to prevent switch chattering if V_{CC} falls very slowly.

Integrated Battery Backup (TC71)

The TC71 differs from the TC70 in that it has a Power Fail (PF) output instead of a gated chip enable ($\overline{CEI}$, $\overline{CEO}$). PF must be externally gated with the decode for the CMOS RAM or other device to be battery-backed. (Many CMOS RAMs have both $\overline{CE}$ and CE enables. In this case, the $\overline{PF}$ output can be connected directly to the CE input of the RAM). PF is high as long as V_{CC} is greater than 4.5V nominal. When V_{CC} falls below 4.5V nominal, $\overline{PF}$ is driven low. Battery switchover for the TC71 is otherwise identical to that of the TC70.

Supply Monitor Noise Sensitivity

The TC70/71 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays), may require a 0.1µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC70/71 as possible to keep the capacitor lead length short.

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TYPICAL APPLICATIONS

Figure 1 shows a full feature implementation of the TC70; Figure 2 shows the TC71. Resistors R1 and R2 of Figure 2 set the trip point voltage for the early power fail warning circuit using the TC71 threshold detector.

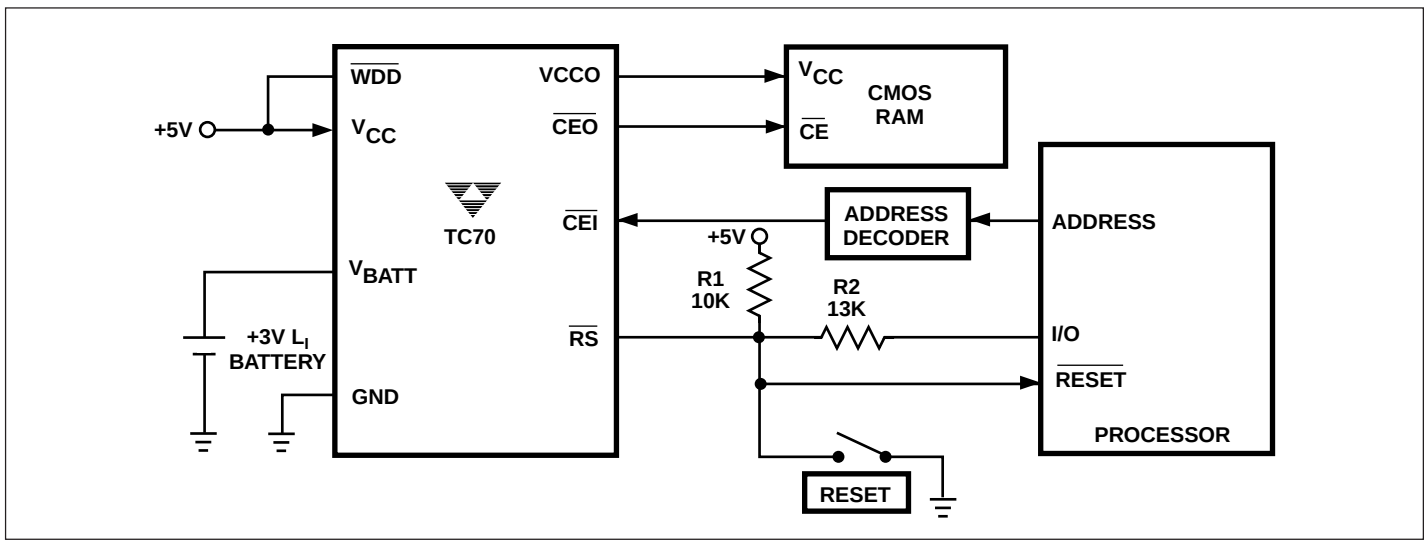


Figure 1. TC70 Typical Application

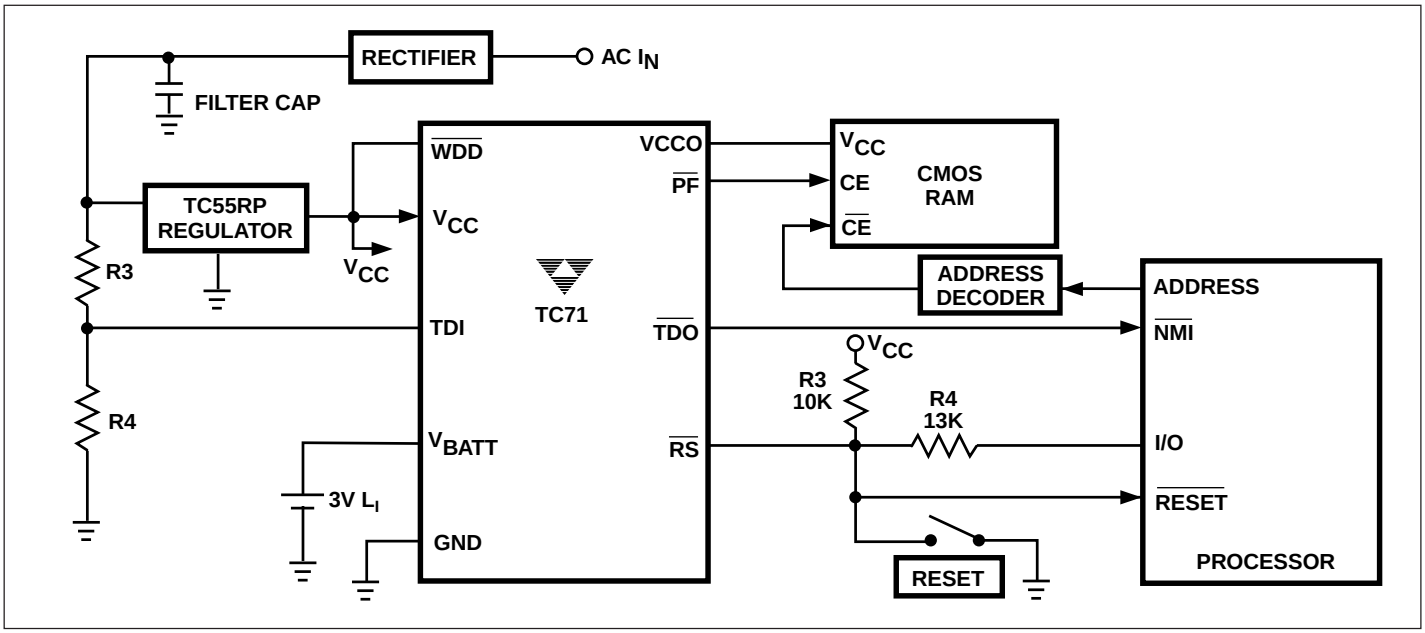
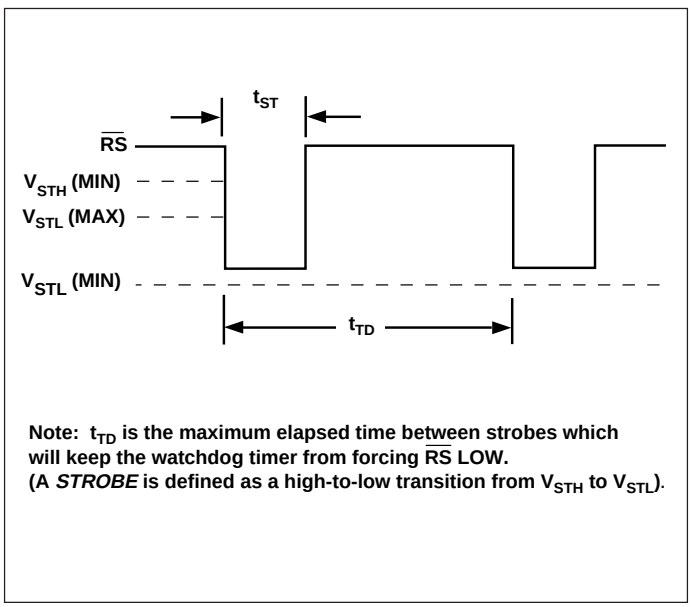


Figure 2. TC71 Typical Application



Note: t_{TD} is the maximum elapsed time between strobes which will keep the watchdog timer from forcing $\overline{RS}$ LOW.
(A *STROBE* is defined as a high-to-low transition from V_{STH} to V_{STL}).

Figure 3. Watchdog Strobe

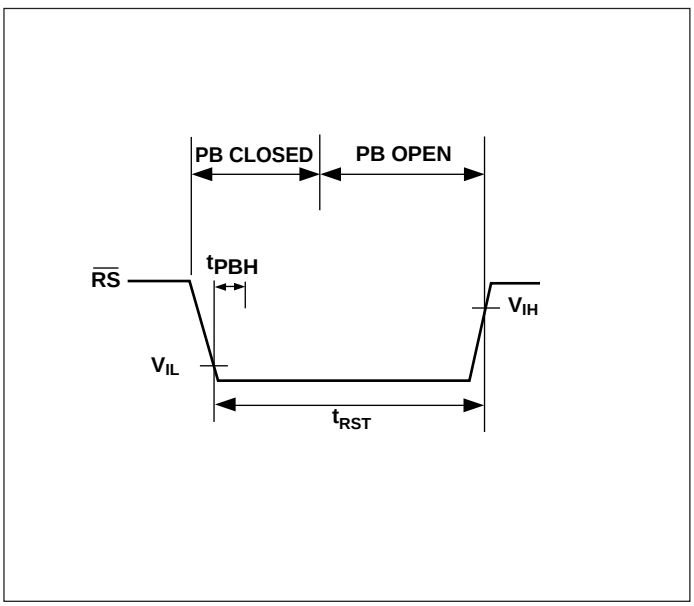


Figure 4. $\overline{RS}$ Override Reset

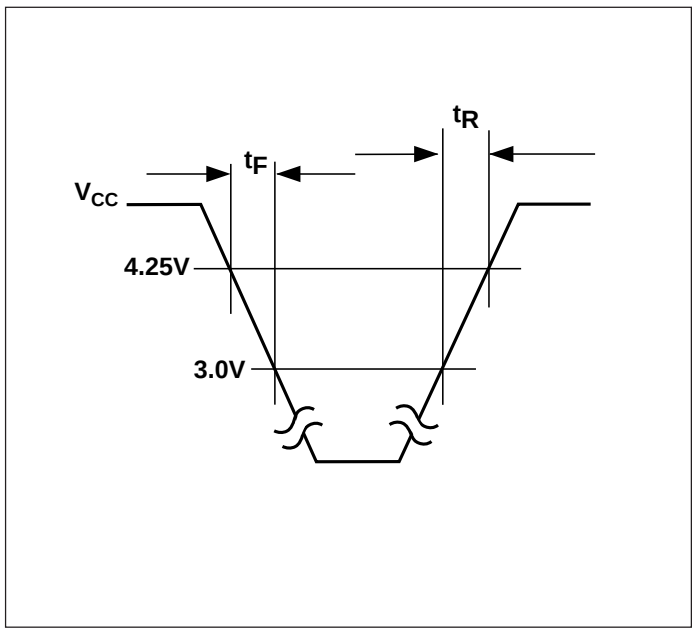


Figure 5. Power Up/Down Slew Rate

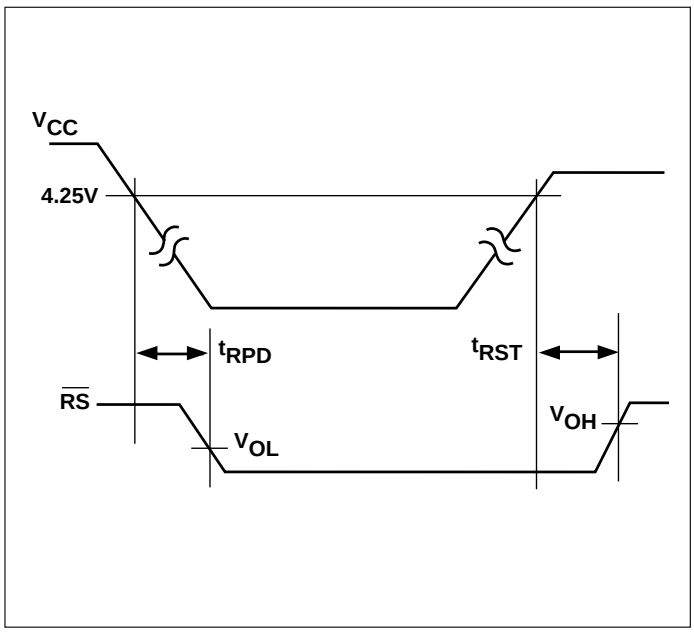


Figure 6. Power Up/Down Reset Timing

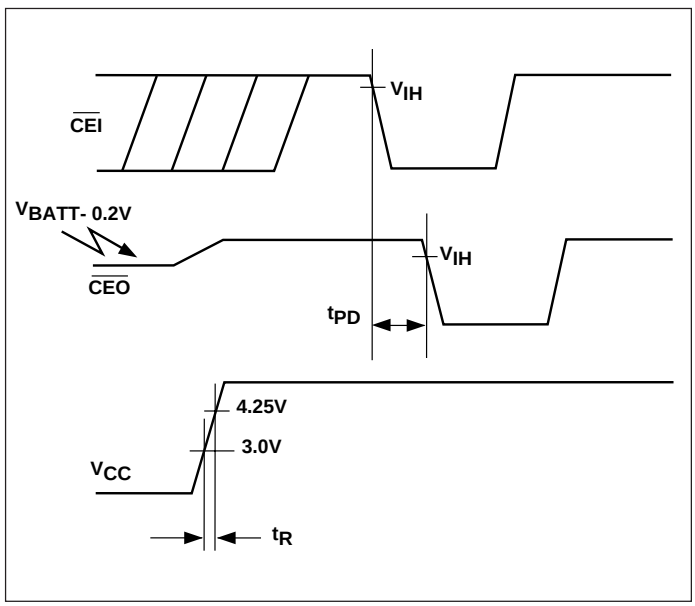


Figure 7. Battery Backup (Power-Up)

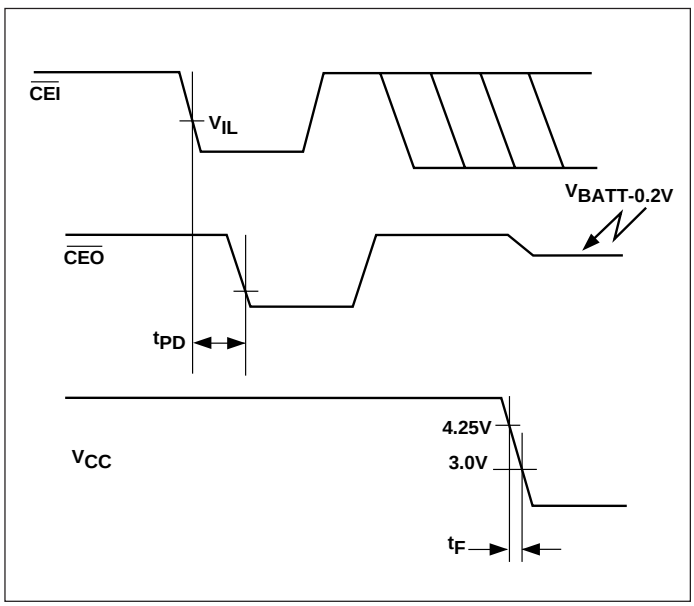


Figure 8. Battery Backup (Power-Down)

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