

#### FEATURES

- High-Performance Voltage Controlled Amplifier
- High-Performance RMS-Level Detector
- Three General-Purpose Opamps
- Wide Dynamic Range: >115 dB
- Low THD: <0.03%
- Low Cost: \$4.39 ('000s)
- DIP & Surface-Mount Packages

#### APPLICATIONS

- Compressors
- Limiters
- Gates
- Expanders
- De-Essers
- Duckers
- Noise Reduction Systems
- Wide-Range Level Meters

#### Description

THAT 4301 Dynamics Processor, dubbed "THAT Analog Engine," combines in a single IC all the active circuitry needed to construct a wide range of dynamics processors. The 4301 includes a high-performance, exponentially-controlled VCA, a log-responding RMS-level sensor and three general-purpose opamps.

The VCA provides two opposing-polarity, voltage-sensitive control ports. Dynamic range exceeds 115 dB, and THD is typically 0.003% at 0 dB gain. In the 4301A, the VCA is selected for low THD at extremely high levels. The RMS detector provides accurate rms-to-dc conversion over an 80 dB dynamic range for signals with

crest factors up to 10. One opamp is dedicated as a current-to-voltage converter for the VCA, while the other two may be used for the signal path or control voltage processing.

The combination of exponential VCA gain control and logarithmic detector response — "decibel-linear" response — simplifies the mathematics of designing the control paths of dynamics processors. This makes it easy to design audio compressors, limiters, gates, expanders, de-essers, duckers, noise reduction systems and the like. The high level of integration ensures excellent temperature tracking between the VCA and the detector, while minimizing the external parts count.

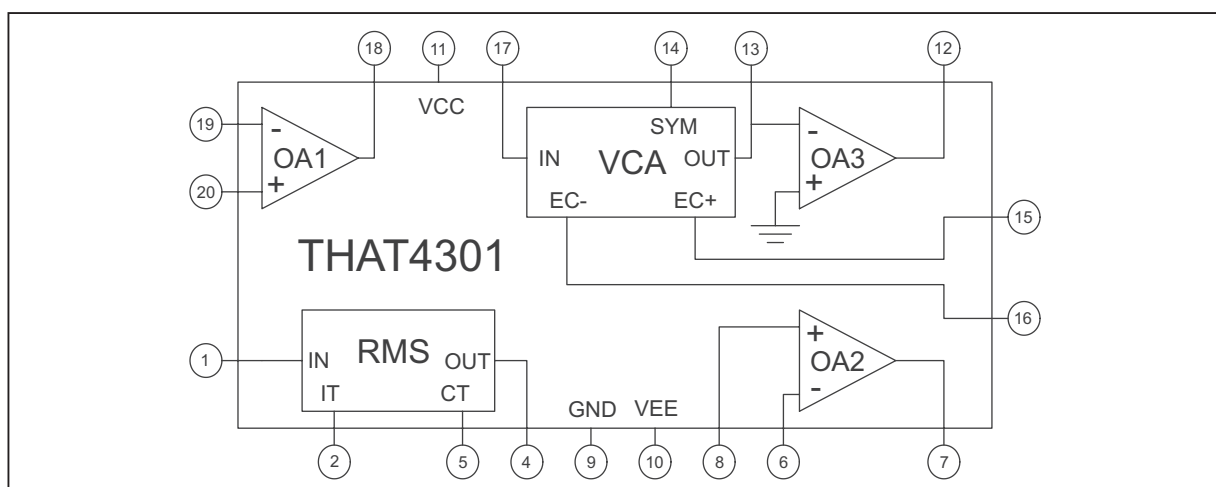


Figure 1. Block Diagram (pin numbers are for DIP only)

## SPECIFICATIONS<sup>1,2</sup>

<b>Absolute Maximum Ratings (T<sub>A</sub> = 25°C)</b>			
Positive Supply Voltage (V <sub>CC</sub> )	+18 V	Power Dissipation (P <sub>D</sub> ) (T <sub>A</sub> = 75°C)	700 mW
Negative Supply Voltage (V <sub>EE</sub> )	-18 V	Operating Temperature Range (T <sub>OP</sub> )	0 to +70°C
Supply Current (I <sub>CC</sub> )	20 mA	Storage Temperature Range (T <sub>ST</sub> )	-40 to +125°C

<b>Overall Electrical Characteristics</b>						
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Positive Supply Voltage	V <sub>CC</sub>		+7	—	+15	V
Negative Supply Voltage	V <sub>EE</sub>		-7	—	-15	V
Positive Supply Current	I <sub>CC</sub>		—	12	18	mA
Negative Supply Current	I <sub>EE</sub>		—	-12	-18	mA
Thermal Resistance	θ <sub>J-C</sub>	SO-Package	—	140	—	°C/W

<b>VCA Electrical Characteristics<sup>3</sup></b>									
Parameter	Symbol	Conditions	4301			4301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I <sub>B(VCA)</sub>	No Signal	—	30	400	—	30	400	pA
Input Offset Voltage	V <sub>OFF(VCA In)</sub>	No Signal	—	±4	±15	—	±4	±15	mV
Input Signal Current	I <sub>IN(VCA)</sub> or I <sub>OUT(VCA)</sub>		—	175	750	—	175	750	μArms
Gain at 0V Control	G <sub>0</sub>	E <sub>C+</sub> = E <sub>C-</sub> = 0.000V	-0.4	0.0	+0.4	-0.4	0.0	+0.4	dB
Gain-Control Constant	T <sub>A</sub> = 25°C (T <sub>CHIP</sub> ≅ 55°C) -60 dB < gain < +40dB								
	E <sub>C+</sub> /Gain (dB)	E <sub>C+</sub> & SYM	6.4	6.5	6.6	6.4	6.5	6.6	mV/dB
	E <sub>C-</sub> /Gain (dB)	E <sub>C-</sub>	-6.4	-6.5	-6.6	-6.4	-6.5	-6.6	mV/dB
Gain-Control TempCo	ΔE <sub>C</sub> / ΔT <sub>CHIP</sub>	Ref T <sub>CHIP</sub> = 27°C	—	+0.33	—	—	+0.33	—	%/°C
Gain-Control Linearity		-60 to +40 dB gain	—	0.5	2	—	0.5	2	%
Off Isolation		E <sub>C+</sub> =SYM=-375mV, E <sub>C-</sub> =+375mV	110	115	—	110	115	—	dB
Output Offset Voltage Change	ΔV <sub>OFF(OUT)</sub>	R <sub>out</sub> = 20kΩ							
		0 dB gain	—	1	3	—	1	3	mV
		+15 dB gain	—	2	10	—	2	10	mV
		+30 dB gain	—	5	25	—	5	25	mV
Gain Cell Idling Current	I <sub>IDLE</sub>		—	20	—	—	20	—	μA
Output Noise	e <sub>n(OUT)</sub>	20 Hz-20 kHz							
		R <sub>out</sub> = 20kΩ							
		0 dB gain	—	-96	-94	—	-96	-94	dBV
		+15 dB gain	—	-85	-83	—	-85	-83	dBV
Total Harmonic Distortion	THD	V <sub>IN</sub> = 0 dBV, 1 kHz							
		0 dB gain	—	0.003	0.007	—	0.003	0.007	%

1. All specifications subject to change without notice.

2. Unless otherwise noted, T<sub>A</sub>=25°C, V<sub>CC</sub> = +15V, V<sub>EE</sub> = -15V; VCA<sub>SYM</sub> adjusted for min THD @ 1 V, 1 kHz, 0 dB gain.

3. Test circuit is the VCA section only from Figure 2.

**SPECIFICATIONS<sup>1,2</sup> (Cont'd.)**

<b>VCA Electrical Characteristics<sup>3</sup> (Cont'd.)</b>									
Parameter	Symbol	Conditions	4301			4301A			Units
			Min	Typ	Max	Min	Typ	Max	
Total Harmonic Distortion (cont'd.) THD		$V_{IN} = +10$ dBV, 1 kHz							
		0 dB gain	—	0.03	0.07	—	0.03	0.07	%
		-15 dB gain	—	0.035	0.09	—	0.035	0.09	%
		$V_{OUT} = +10$ dBV, 1 kHz							
		+15 dB gain	—	0.035	0.09	—	0.035	0.09	%
		$V_{IN} = +19.5$ dBV, 1 kHz							
		0 dB gain	—	—	—	—	0.05	0.09	%
Symmetry Control Voltage	$V_{SYM}$	minimum THD	-2.5	0	+2.5	-2.5	0	+2.5	mV

<b>RMS Detector Electrical Characteristics<sup>4</sup></b>						
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Bias Current	$I_{B(RMS)}$	No Signal	—	30	400	pA
Input Offset Voltage	$V_{OFF(RMS IN)}$	No Signal	—	±4	±15	mV
Input Signal Current	$I_{IN(RMS)}$		—	175	750	μA
Input Current for 0 V Output	$I_{in0}$	$I_T = 7.5\mu A$	6	8.5	12	μA
Output Scale Factor	$E_O / 20\log(I_{in}/I_{in0})$	$31.6nA < I_{IN} < 1mA$ $T_A = 25^\circ C$ ( $T_{CHIP} \approx 55^\circ C$ )	6.4	6.5	6.6	mV/dB
Scale Factor Match (RMS to VCA)		-20 dB < VCA Gain < +20 dB $1\mu A < I_{in(DET)} < 100\mu A$	.985	1	1.015	
Output Linearity		$f_{IN} = 1kHz$				
		$1\mu A < I_{in} < 100\mu A$	—	0.1	—	dB
		$100nA < I_{in} < 316\mu A$	—	0.5	—	dB
		$31.6nA < I_{in} < 1mA$	—	1.5	—	dB
Rectifier Balance		$f_{IN} = 100 Hz$ , $\tau = .001 s$ $1\mu A < I_{in} < 100\mu A$	-20	—	20	%
Crest Factor		1ms pulse repetition rate				
		0.2 dB error	—	3.5	—	
		0.5 dB error	—	5	—	
Maximum Frequency for 2 dB Additional Error		$I_{in} \geq 10\mu A$	—	100	—	kHz
		$I_{in} \geq 3\mu A$	—	45	—	kHz
		$I_{in} \geq 300nA$	—	7	—	kHz
Timing Current Set Range	$I_T$		1.5	7.5	15	μA
Voltage at $I_T$ Pin		$I_T = 7.5\mu A$	-10	+20	+50	mV
Timing Current Accuracy	$I_{CT}/I_T$	$I_T = 7.5\mu A$	0.90	1.1	1.30	
Filtering Time Constant	$\tau$	$T_{CHIP} = 55^\circ C$			$(0.026)^{C_T/I_T}$	s
Output Temp. Coefficient	$\Delta E_O / \Delta T_{CHIP}$	Re: $T_{CHIP} = 27^\circ C$	—	0.33	—	%/°C
Output Current	$I_{OUT}$	-300mV < $V_{OUT}$ < +300mV	±90	±100	—	μA

4. Except as noted, test circuit is the RMS-Detector section only from Figure 2.

### Specifications<sup>1,2</sup> (Cont'd)

<b>Opamp Electrical Characteristics<sup>5</sup></b>												
Parameter	Symbol	Conditions	OA1			OA2			OA3			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$		—	±0.5	±6	—	±0.5	±6	—	±0.5	±6	mV
Input Bias Current	$I_b$		—	150	500	—	150	500	—	150	500	nA
Input Offset Current	$I_{OS}$		—	15	50	—	15	50	—	N/A		nA
Input Voltage Range	$I_{VR}$		—	±13.5	—	—	±13.5	—	—	N/A		V
Common Mode Rej. Ratio	CMRR	$R_S < 10k$	—	100	—	—	100	—	—	N/A		
Power Supply Rej. Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	100	—	—	100	—	—	100	—	
Gain Bandwidth Product	GBW	(@50kHz)	—	5	—	—	5	—	—	5	—	MHz
Open Loop Gain	$A_{VO}$	$R_L = 10k$	—	115	—	—	110	—	—	125	—	
		$R_L = 2k$	—	N/A	—	—	N/A	—	—	120	—	
Output Voltage Swing	$V_O @ R_L = 5k\Omega$		—	±13	—	—	±13	—	—	±14	—	V
		$V_O @ R_L = 2k\Omega$	—	N/A	—	—	N/A	—	—	±13	—	V
Short Circuit Output Current			—	4	—	—	4	—	—	12	—	mA
Slew Rate	SR		—	2	—	—	2	—	—	2	—	V/ $\mu s$
Total Harmonic Distortion	THD	1kHz, $A_V = 1$ , $R_L = 10k\Omega$	—	0.0007	0.003	—	0.0007	0.003	—	0.0007	0.003	%
		1kHz, $A_V = -1$ , $R_L = 2k\Omega$	—	N/A	—	—	N/A	—	—	0.0007	0.003	%
Input Noise Voltage Density	$e_n$	$f_o = 1kHz$	—	6.5	10	—	7.5	12	—	7.5	12	$nV/\sqrt{Hz}$
Input Noise Current Density	$i_n$	$f_o = 1kHz$	—	0.3	—	—	0.3	—	—	0.3	—	$pA/\sqrt{Hz}$

5. Test circuit for opamps is a unity-gain follower configuration, with load resistor  $R_L$  as specified.

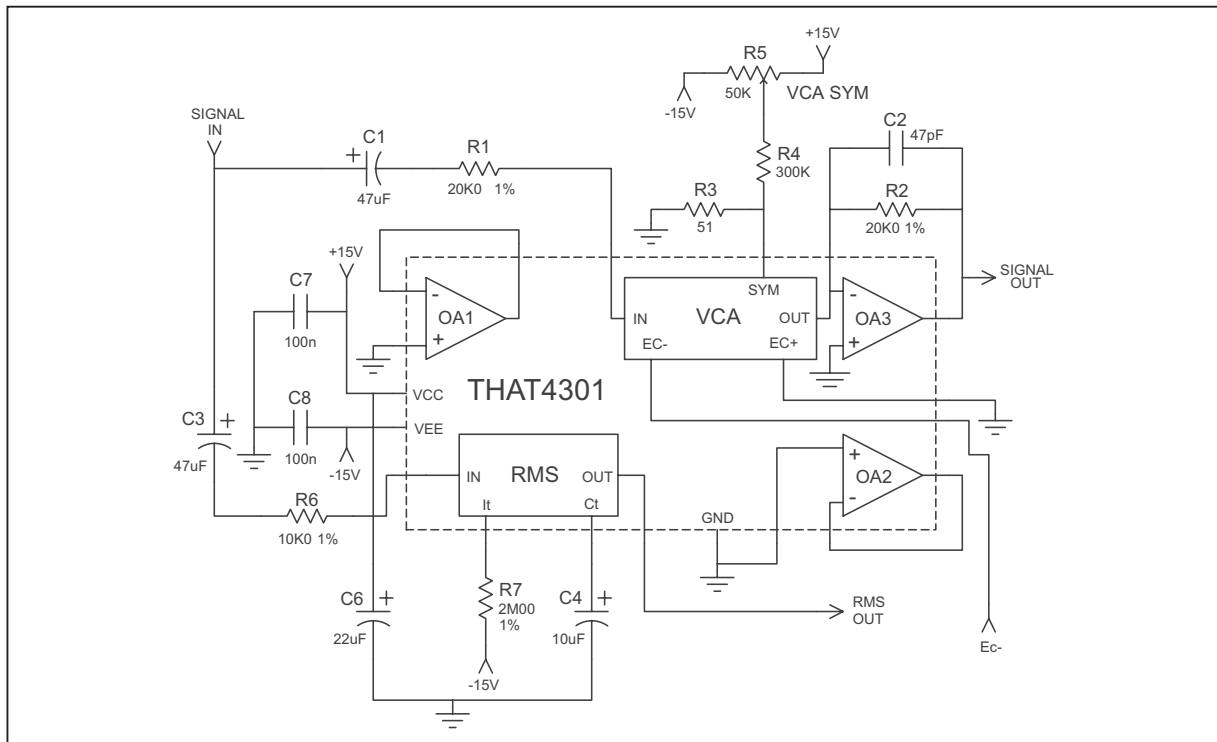


Figure 2. VCA and RMS detector test circuit

Pin Name	DIP P in	SO Pin
RMS In	1	3
I <sub>T</sub> (I <sub>Time</sub> )	2	4
No Connection	3	5
RMS Out	4	6
C <sub>T</sub> (C <sub>Time</sub> )	5	7
OA2 -In	6	9
OA2 Out	7	10
OA2 +In	8	11
GND	9	12
VEE	10	13
VCC	11	18
OA3 Out	12	19
VCA Out	13	20
SYM	14	22
E <sub>C+</sub>	15	23

Pin Name	DIP P in	SO Pin
E <sub>C-</sub>	16	24
VCA In	17	25
OA1 Out	18	26
OA1 -In	19	27
OA1 +In	20	28
No Connection		1
No Connection		2
No Connection		8
No Connection		14
No Connection		15
No Connection		16
No Connection		17
No Connection		21
No Connection		29
No Connection		30

Table 1. Pin Connections

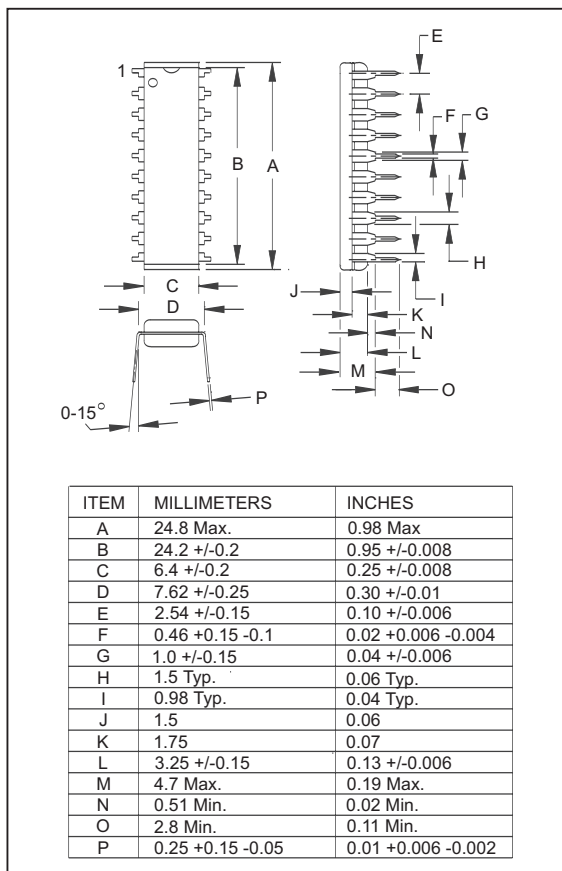


Figure 3. Plastic dual in-line package outline

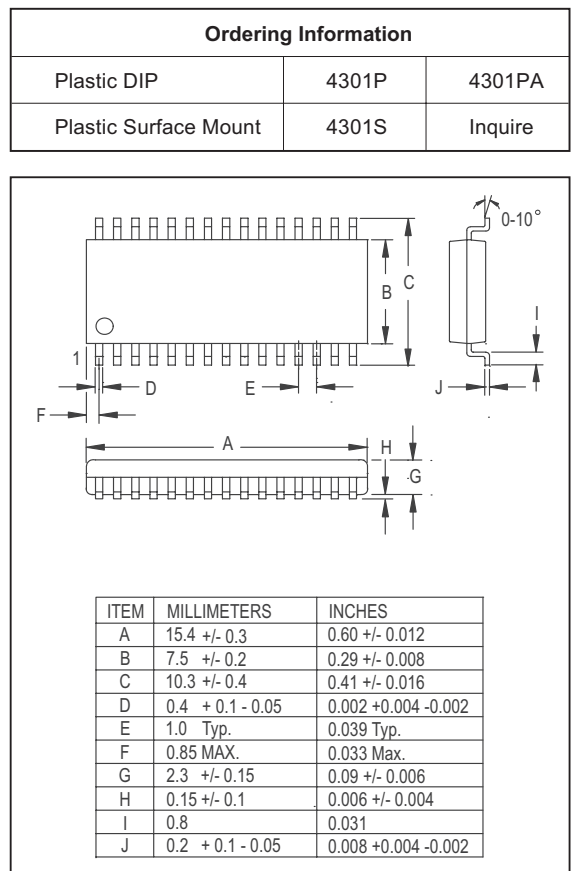


Figure 4. Plastic surface-mount package outline

### Representative Data

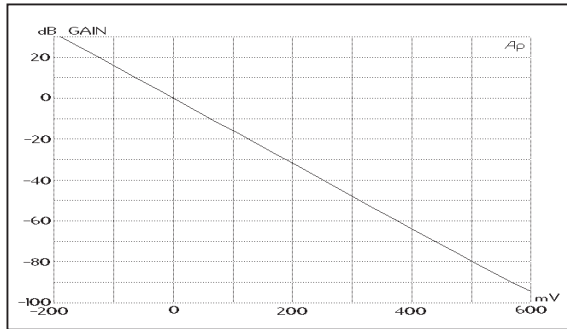


Figure 5. VCA Gain vs. Control Voltage (Ec-) at 25°C

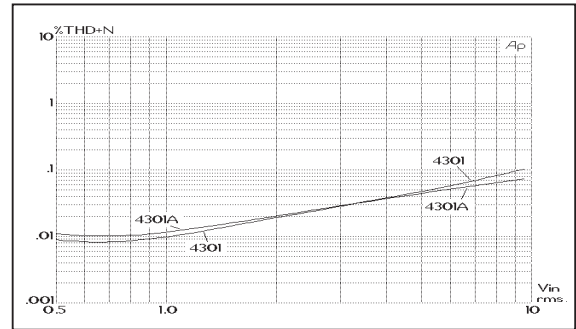


Figure 6. VCA 1kHz THD+Noise vs. Input, -15 dB Gain

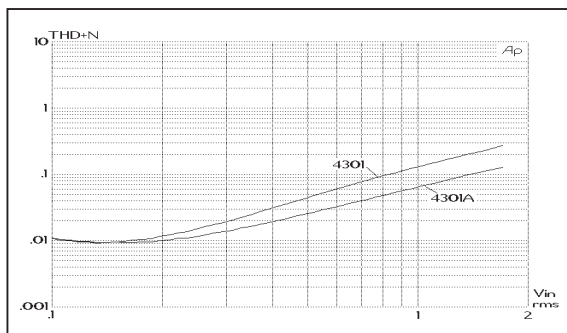


Figure 7. VCA 1kHz THD+Noise vs. Input, +15 dB Gain

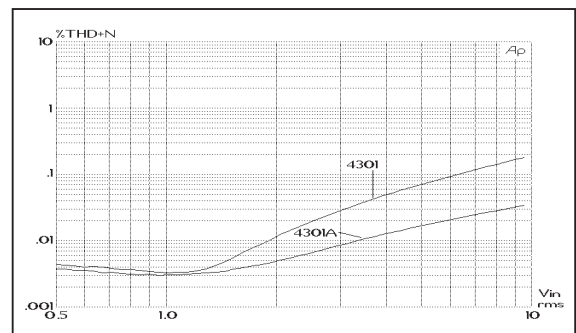


Figure 8. VCA 1kHz THD+Noise vs. Input, 0 dB Gain

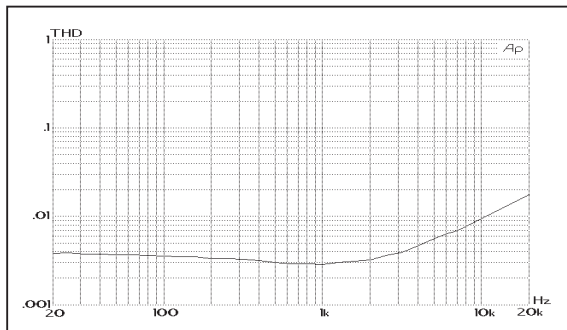


Figure 9. VCA THD vs. Frequency, 0 dB Gain, 1Vrms Input

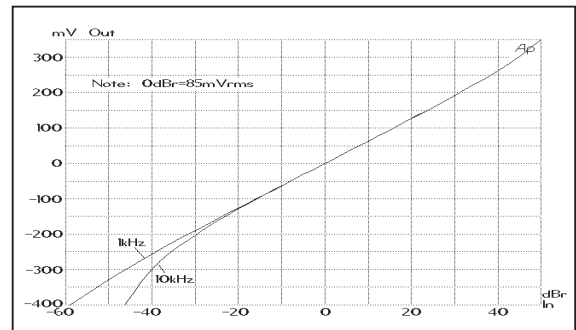


Figure 10. RMS Output vs. Input Level, 1 kHz & 10 kHz

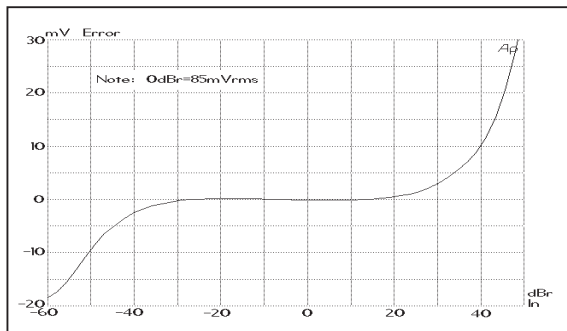


Figure 11. Departure from Ideal Detector Law vs. Level

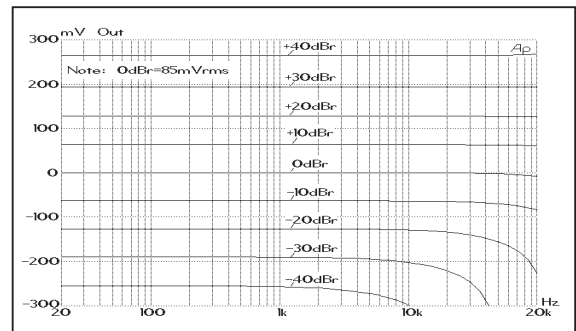


Figure 12. Detector Output vs. Frequency at Various Levels

## Theory of Operation

THAT 4301 Dynamics Processor combines THAT Corporation's proven Voltage-Controlled Amplifier (VCA) and RMS-Level Detector designs with three general-purpose opamps to produce an *Analog Engine* useful in a variety of dynamics processor applications. For details of the theory of operation of the VCA and RMS-Detector building blocks, the interested reader is referred to THAT Corporation's data sheets on the 2150 Series VCAs and the 2252 RMS-Level Detector. Theory of the interconnection of exponentially-controlled VCAs and log-responding level detectors is covered in THAT Corporation's application note AN101, *The Mathematics of Log-Based Dynamic Processors*.

### The VCA — in Brief

THAT 4301 VCA is based on THAT Corporation's highly successful complementary log-antilog gain cell topology, as used in THAT 2150-Series IC VCAs, and the modular 202 Series VCAs. THAT 4301 is integrated using a fully complementary, BiFET process. The combination of FETs with high-quality, complementary bipolar transistors (NPNs and PNPs) allows additional flexibility in the design of the VCA over previous efforts.

Input signals are *currents* to the VCA IN pin. This pin is a virtual ground, so in normal operation an input voltage is converted to input current via an appropriately sized resistor ( $R_1$  in Figure 2, Page 4). Because dc offsets present at the input pin and any dc offset in preceding stages will be modulated by gain changes (thereby becoming audible as thumps), the input pin is normally ac-coupled ( $C_1$  in Figure 2).

The VCA output signal is also a *current*, inverted with respect to the input current. In normal operation, the output current is converted to a voltage via inverter  $OA_3$ , where the ratio of the conversion is determined by the feedback resistor ( $R_2$ , Figure 2) connected between  $OA_3$ 's output and its inverting input. The signal path through the VCA and  $OA_3$  is noninverting.

The gain of the VCA is controlled by the voltage applied to  $E_{C-}$ ,  $E_{C+}$ , and SYM. Gain (in decibels) is proportional to  $E_{C+} - E_{C-}$ , provided  $E_{C+}$  and SYM are at essentially the same voltage (see below). The constant of proportionality is  $-6.5$  mV/dB for the voltage at  $E_{C-}$ , and  $6.5$  mV/dB for the voltage at  $E_{C+}$  and SYM.

As mentioned, for proper operation, the same voltage must be applied to  $E_{C+}$  and SYM, except for a small ( $\pm 2.5$  mV) dc bias applied *between* these pins. This bias voltage adjusts for internal mismatches in the VCA gain cell which would otherwise cause small differences between the gain of positive and negative half-cycles of the signal. The voltage is usually applied via an external trim potentiometer ( $R_5$  in Figure

2), which is adjusted for minimum signal distortion at unity (0 dB) gain.

The VCA may be controlled via  $E_{C-}$ , as shown in Figure 2, or via the combination of  $E_{C+}$  and SYM. This connection is illustrated in Figure 13. Note that this figure shows only that portion of the circuitry needed to drive the positive VCA control port; circuitry associated with  $OA_1$ ,  $OA_2$  and the RMS detector has been omitted.

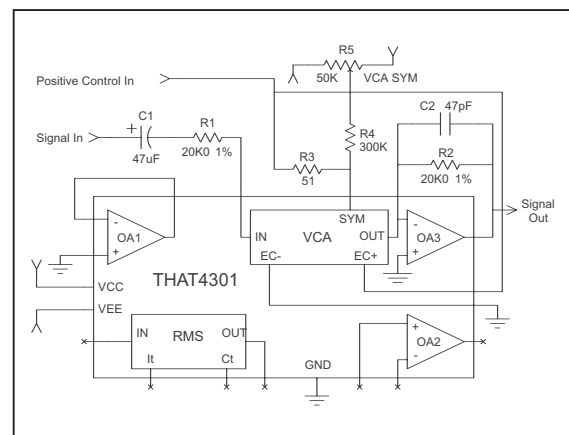


Figure 13. Driving the VCA via the Positive Control Port

While the 4301's VCA circuitry is very similar to that of the THAT 2150 Series VCAs, there are several important differences, as follows:

- 1) Supply current for the VCA is fixed internally. Approximately 2mA is available for the sum of input and output signal currents. (This is also the case in a 2150 Series VCA when biased as recommended.)
- 2) The signal current output of the VCA is internally connected to the inverting input of an on-chip opamp. In order to provide external feedback around this opamp, this node is brought out to a pin.
- 3) The control-voltage constant is approximately 6.5 mV/dB, due primarily to the higher internal operating temperature of the 4301 compared to that of the 2150 Series.
- 4) The input stage of the 4301 VCA uses integrated P-channel FETs rather than a bias-current corrected bipolar differential amplifier. Input bias currents have therefore been reduced.

### The RMS Detector — in Brief

The 4301's detector computes rms level by rectifying input current signals, converting the rectified current to a logarithmic voltage, and applying that voltage to a log-domain filter. The output signal is a dc voltage proportional to the decibel-level of the rms

value of the input signal current. Some ac component (at twice the input frequency) remains superimposed on the dc output. The ac signal is attenuated by a log-domain filter, which constitutes a single-pole rolloff with cutoff determined by an external capacitor and a programmable dc current.

As in the VCA, input signals are *currents* to the RMS IN pin. This input is a virtual ground, so a resistor ( $R_6$  in Figure 2) is normally used to convert input voltages to the desired current. The level detector is capable of accurately resolving signals well below 10 mV (with a 10 k $\Omega$  input resistor). However, if the detector is to accurately track such low-level signals, ac coupling is normally required.

The log-domain filter cutoff frequency is usually placed well below the frequency range of interest. For an audio-band detector, a typical value would be 5 Hz, or a 32 ms time constant ( $\tau$ ). The filter's time constant is determined by an external capacitor attached to the  $C_T$  pin, and an internal current source ( $I_{CT}$ ) connected to  $C_T$ . The current source is programmed via the  $I_T$  pin: current in  $I_T$  is mirrored to  $I_{CT}$  with a gain of approximately 1.1. The resulting time constant  $\tau$  is approximately equal to  $0.026 C_T/I_T$ . Note that, as a result of the mathematics of RMS detection, the attack and release time constants are fixed in their relationship to each other.

The dc output of the detector is scaled with the same constant of proportionality as the VCA gain control: 6.5 mV/dB. The detector's 0 dB reference ( $I_{ino}$ , the input current which causes 0 V output), is determined by  $I_T$  as follows:  $I_{ino} = \sqrt{9.6 \text{ mA } I_T}$ . The detector output stage is capable of sinking or sourcing 100  $\mu$ A.

Differences between the 4301's RMS-Level Detector circuitry and that of the THAT 2252 RMS Detector are as follows:

- 1) The rectifier in the 4301 RMS Detector is internally balanced by design, and cannot be balanced via an external control. The 4301 will typically balance positive and negative halves of the input signal within  $\pm 1.5\%$ , but in extreme cases the mismatch may reach  $\pm 15\%$ . However, a 15% mismatch will not significantly increase ripple-induced distortion in dynamics processors over that caused by signal

ripple alone.

- 2) The time constant of the 4301's RMS detector is determined by the combination of an external capacitor (connected to the  $C_T$  pin) and an internal, programmable current source. The current source is equal to  $1.1 I_T$ . Normally, a resistor is not connected directly to the  $C_T$  pin on the 4301.

- 3) The 0 dB reference point, or *level match*, is not adjustable via an external current source. However, as in the 2252, the level match is affected by the timing current, which, in this case, is drawn from the  $I_T$  pin and mirrored internally to  $C_T$ .

- 4) The input stage of the 4301 RMS detector uses integrated P-channel FETs rather than a bias-current corrected bipolar differential amplifier. Input bias currents are therefore negligible, improving performance at low signal levels.

### The Opamps — in Brief

The three opamps in the 4301 are intended for general purpose applications. All are 5 MHz opamps with slew rates of approximately 2V/ $\mu$ s. All use bipolar PNP input stages. However, the design of each is optimized for its expected use. Therefore, to get the most out of the 4301, it is useful to know the major differences among these opamps.

OA<sub>3</sub>, being internally connected to the output of the VCA, is intended for current-to-voltage conversion. Its input noise performance, at  $7.5^{nV} \sqrt{\text{Hz}}$ , complements that of the VCA, adding negligible noise at unity gain. Its output section is capable of driving a 2 k $\Omega$  load to within 2V of the power supply rails, making it possible to use this opamp directly as the output stage in single-ended designs.

OA<sub>1</sub> is the quietest opamp of the three. Its input noise voltage, at  $6.5^{nV} \sqrt{\text{Hz}}$ , makes it the opamp of choice for input stages. Note that its output drive capability is limited (in order to reduce the chip's power dissipation) to approximately  $\pm 3$  mA. It is comfortable driving loads of 5 k $\Omega$  or more to within 1V of the power supply rails.

OA<sub>2</sub> is intended primarily as a control-voltage processor. Its input noise parallels that of OA<sub>3</sub>, and its output drive capability parallels that of OA<sub>1</sub>.



## Applications

The circuit of Figure 14, Page 9, shows a typical application for THAT 4301. This simple compressor/limiter design features adjustable hard-knee threshold, compression ratio, and static gain<sup>1</sup>. The applications discussion in this data sheet will center on this circuit for the purpose of illustrating important design issues. However, it is possible to configure many other types of dynamics processors with THAT 4301. Hopefully, the following discussion will imply some of these possibilities.

### Signal Path

As mentioned in the section on theory, the VCA input pin is a virtual ground with negative feedback provided internally. An input resistor ( $R_1$ , 20k $\Omega$ ) is required to convert the ac input voltage to a current within the linear range of the 4301. (Peak VCA input currents should be kept under 1 mA for best distortion performance.) The coupling capacitor ( $C_1$ , 47  $\mu$ f) is strongly recommended to block dc current from preceding stages (and from offset voltage at the input of the VCA). Any dc current into the VCA will be modulated by varying gain in the VCA, showing up in the output as "thumps". Note that  $C_1$ , in conjunction with  $R_1$ , will set the low frequency limit of the circuit.

The VCA output is connected to  $OA_3$ , configured as an inverting current-to-voltage converter.  $OA_3$ 's feedback components ( $R_2$ , 20 k $\Omega$ , and  $C_2$ , 47 pf) determine the constant of current-to-voltage conversion. The simplest way to deal with this is to recognize that when the VCA is set for unity (0 dB) gain, the input to output voltage gain is simply  $R_2/R_1$ , just as in the case of a single in-

verting stage. If, for some reason, more than 0 dB gain is required when the VCA is set to unity, then the resistors may be skewed to provide it. Note that the feedback capacitor ( $C_2$ ) is required for stability. The VCA output has approximately 45 pf of capacitance to ground, which must be neutralized via the 47 pf feedback capacitor across  $R_2$ .

The VCA gain is controlled via the  $E_{C-}$  terminal, whereby gain will be proportional to the negative of the voltage at  $E_{C-}$ . The  $E_{C+}$  terminal is grounded, and the SYM terminal is returned nearly to ground via a small resistor ( $R_3$ , 51  $\Omega$ ). The VCA SYM trim ( $R_5$ , 50 k $\Omega$ ) allows a small voltage to be applied to the SYM terminal via  $R_4$  (300 k $\Omega$ ). This voltage adjusts for small mismatches within the VCA gain cell, thereby reducing even-order distortion products. To adjust the trim, apply to the input a middle-level, middle-frequency signal (1 kHz at 1 V is a good

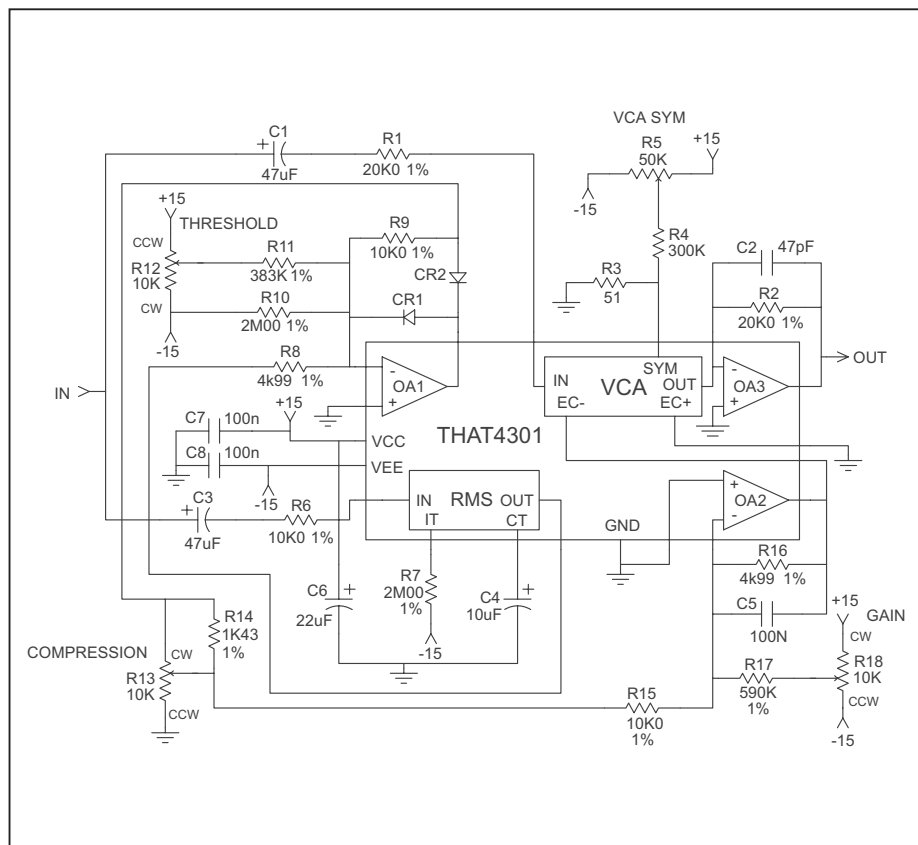


Figure 14. Typical Compressor/Limiter Application Circuit

1. More information on this compressor design, along with suggestions for converting it to soft-knee operation, is given in AN100, *Basic Compressor Limiter Design*. The designs in AN100 are based on THAT Corporation's 2150-Series VCAs and 2252 RMS Detector, but are readily adaptable to the 4301 with only minor modifications. In fact, the circuit presented here is functionally identical to the hard-knee circuit published in AN100.

choice with this circuit) and observe THD at the signal output. Set the trim for minimum THD.

### RMS-Level Detector

The RMS detector's input is similar to that of the VCA. An input resistor ( $R_6$ , 10 k $\Omega$ ) converts the ac input voltage to a current within the linear range of the 4301. (Peak detector input currents should be kept under 1 mA for best linearity.) The coupling capacitor ( $C_3$ , 47  $\mu$ f) is recommended to block dc current from preceding stages (and from offset voltage at the input of the detector). Any dc current into the detector will limit the low-level resolution of the detector, and will upset the rectifier balance at low levels. Note that, as with the VCA input circuitry,  $C_3$  in conjunction with  $R_6$  will set the lower frequency limit of the detector.

The time response of the RMS detector is determined by the capacitor attached to  $C_T$  ( $C_4$ , 10  $\mu$ f) and the size of the current in pin  $I_T$  (determined by  $R_7$ , 2 M $\Omega$  and the negative power supply, -15V). Since the voltage at  $I_T$  is approximately 0 V, the circuit of Figure 14 produces 7.5  $\mu$ A in  $I_T$ . The current in  $I_T$  is mirrored with a gain of 1.1 to the  $C_T$  pin, where it is available to discharge the timing capacitor ( $C_4$ ). The combination produces a log filter with time constant equal to approximately 0.026  $C_T/I_T$  (~35 ms in the circuit shown).

The waveform at  $C_T$  will follow the logged (decibel) value of the input signal envelope, plus a dc offset of about 1.3 V (2  $V_{BE}$ ). This allows a polarized capacitor to be used for the timing capacitor, usually an electrolytic. The capacitor used should be a low-leakage type in order not to add significantly to the timing current.

The output stage of the RMS detector serves to buffer the voltage at  $C_T$  and remove the 1.3 V dc offset, resulting in an output centered around 0 V for input signals of about 85 mV. The output voltage increases 6.5 mV for every 1 dB increase in input signal level. This relationship holds over more than a 60 dB range in input currents.

### Control Path

A compressor/limiter is intended to reduce its gain as signals rise above a threshold. The output of the RMS detector represents the input signal level over a wide range of levels, but compression only occurs when the level is above the threshold.  $OA_1$  is configured as a variable threshold detector to block envelope information for low-level signals, passing only information for signals above threshold.

$OA_1$  is an inverting stage with gain of 2 above threshold and 0 below threshold. Neglecting the action of the THRESHOLD control ( $R_{12}$ ) and its associated resistors ( $R_{11}$  and  $R_{10}$ ), positive signals from the RMS detector output drive the output of  $OA_1$  negative. This forward biases  $CR_2$ , closing the feedback

loop such that the junction of  $R_9$  and  $CR_2$  (the output of the threshold detector) sits at  $-(R_9/R_8)$   $RMS_{OUT}$ . For the circuit of Figure 14, this is  $-2 RMS_{OUT}$ . Negative signals from the RMS detector drive the output of  $OA_1$  positive, reverse biasing  $CR_2$  and forward biasing  $CR_1$ . In this case, the junction of  $R_9$  and  $CR_2$  rests at 0 V, and no signal level information is passed to the threshold detector's output.

In order to vary the threshold,  $R_{12}$ , the THRESHOLD control, is provided. Via  $R_{11}$  (383 k $\Omega$ ),  $R_{12}$  adds up to  $\pm 39.2 \mu$ A of current to  $OA_1$ 's summing junction, requiring the same amount of opposite-polarity current from the RMS detector output to counterbalance it. At 4.99 k $\Omega$ , the voltage across  $R_8$  required to produce a counterbalancing current is  $\pm 195$  mV, which represents a  $\pm 30$  dB change in RMS detector input level.

Since the RMS detector's 0 dB reference level is 85 mV, the center of the THRESHOLD pot's range would be 85 mV, were it not for  $R_{10}$  (2 M $\Omega$ ), which provides an offset.  $R_{10}$  adds an extra  $-7.5 \mu$ A to  $OA_1$ 's summing junction, which would be counterbalanced by 37.4 mV at the detector output. This corresponds to 5.8 dB, offsetting the THRESHOLD center by this much to 165 mV, or approximately -16 dBV.

The output of the threshold detector represents the signal level above the determined threshold, at a constant of about 13 mV/dB (from  $[R_9/R_8]$  6.5 mV/dB). This signal is passed on to the COMPRESSION control ( $R_{13}$ ), which variably attenuates the signal passed on to  $OA_2$ . Note that the gain of  $OA_2$ , from the wiper of the COMPRESSION control to  $OA_2$ 's output, is  $R_{16}/R_{15}$  (0.5), precisely the inverse of the gain of  $OA_1$ . Therefore, the COMPRESSION control lets the user vary the above-threshold gain between the RMS detector output and the output of  $OA_1$  from zero to a maximum of unity.

The gain control constant of the VCA, 6.5 mV/dB, is *exactly* equal to the output scaling constant of the RMS detector. Therefore, at maximum COMPRESSION, above threshold, every dB increase in input signal level causes a 6.5 mV increase in the output of  $OA_2$ , which in turn causes a 1 dB decrease in the VCA gain. With this setting, the output will not increase despite large increases in input level above threshold. This is infinite compression. For intermediate settings of COMPRESSION, a 1 dB increase in input signal level will cause less than a 1 dB decrease in gain, thereby varying the compression ratio.

The resistor  $R_{14}$  is included to alter the taper of the COMPRESSION pot to better suit common use. If a linear taper pot is used for  $R_{13}$ , the compression ratio will be 1:2 at the middle of the rotation. However, 1:2 compression in an above-threshold compressor is not very strong processing, so 1:4 is often preferred at the midpoint.  $R_{14}$  warps the taper of  $R_{13}$  so that 1:4 compression occurs at approximately the midpoint of  $R_{13}$ 's rotation.

The GAIN control ( $R_{18}$ ) is used to provide static gain or attenuation in the signal path. This control adds up to  $\pm 130$  mV offset to the output of  $OA_2$  (from  $-V_+ R_{16}/R_{17}$  to  $-V_- R_{16}/R_{17}$ ), which is approximately  $\pm 20$  dB change in gain of the VCA.  $C_5$  is used to attenuate the noise of  $OA_2$ ,  $OA_1$  and the resistors  $R_8$  through  $R_{16}$  used in the control path. All these active and passive components produce noise which is passed on to the control port of the VCA, causing modulation of the signal. By itself, the 4301 VCA produces very little noise modulation, and its performance can be significantly degraded by the use of noisy components in the control voltage path.

### Overall Result

The resulting compressor circuit provides hard-knee compression above threshold with three essential user-adjustable controls. The threshold of compression may be varied over a  $\pm 30$  dB range from about  $-46$  dBV to  $+14$  dBV. The compression ratio

may be varied from 1:1 (no compression) to  $\infty$ :1. And, static gain may be added up to  $\pm 20$  dB. Audio performance is excellent, with THD running below 0.05% at middle frequencies even with 10 dB of compression, and an input dynamic range of over 115 dB.

Perhaps most important, this example design only scratches the surface of the large body of applications circuits which may be constructed with THAT 4301. The combination of an accurate, wide-dynamic-range, log-responding level detector with a high-quality, exponentially-responding VCA produces a versatile and powerful analog engine. The opamps provided in the 4301 enable the designer to configure these building blocks with few external components to construct gates, expanders, de-essers, noise reduction systems and the like.

For further information, samples and pricing, please contact us at the address below.

## Notes