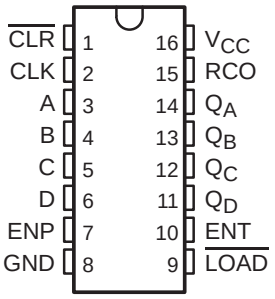
CD54AC163, CD74AC163
4-BIT SYNCHRONOUS BINARY COUNTERS

SCHS299 – APRIL 2000

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (M), Standard Plastic (E) and Ceramic (F) DIPs**

CD54AC163 . . . F PACKAGE
CD74AC163 . . . E OR M PACKAGE
(TOP VIEW)



description

The CD54AC163 and CD74AC163 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These devices feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The CD54AC163 is characterized for operation over the full military temperature range of –55°C to 125°C. The CD74AC163 is characterized for operation from –40°C to 85°C.

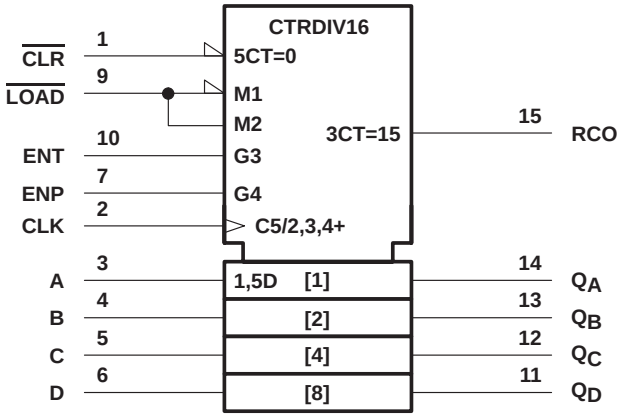
FUNCTION TABLE

INPUTS						OUTPUTS		FUNCTION
$\overline{CLR}$	CLK	ENP	ENT	$\overline{LOAD}$	A,B,C,D	Q_n	RCO	
L	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	Note 1	
h	↑	h	h	h	X	Count	Note 1	Count
h	X	l	X	h	X	q_n	Note 1	Inhibit
h	X	X	l	h	X	q_n	L	

H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, l = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, ↑ = CLK low-to-high transition.

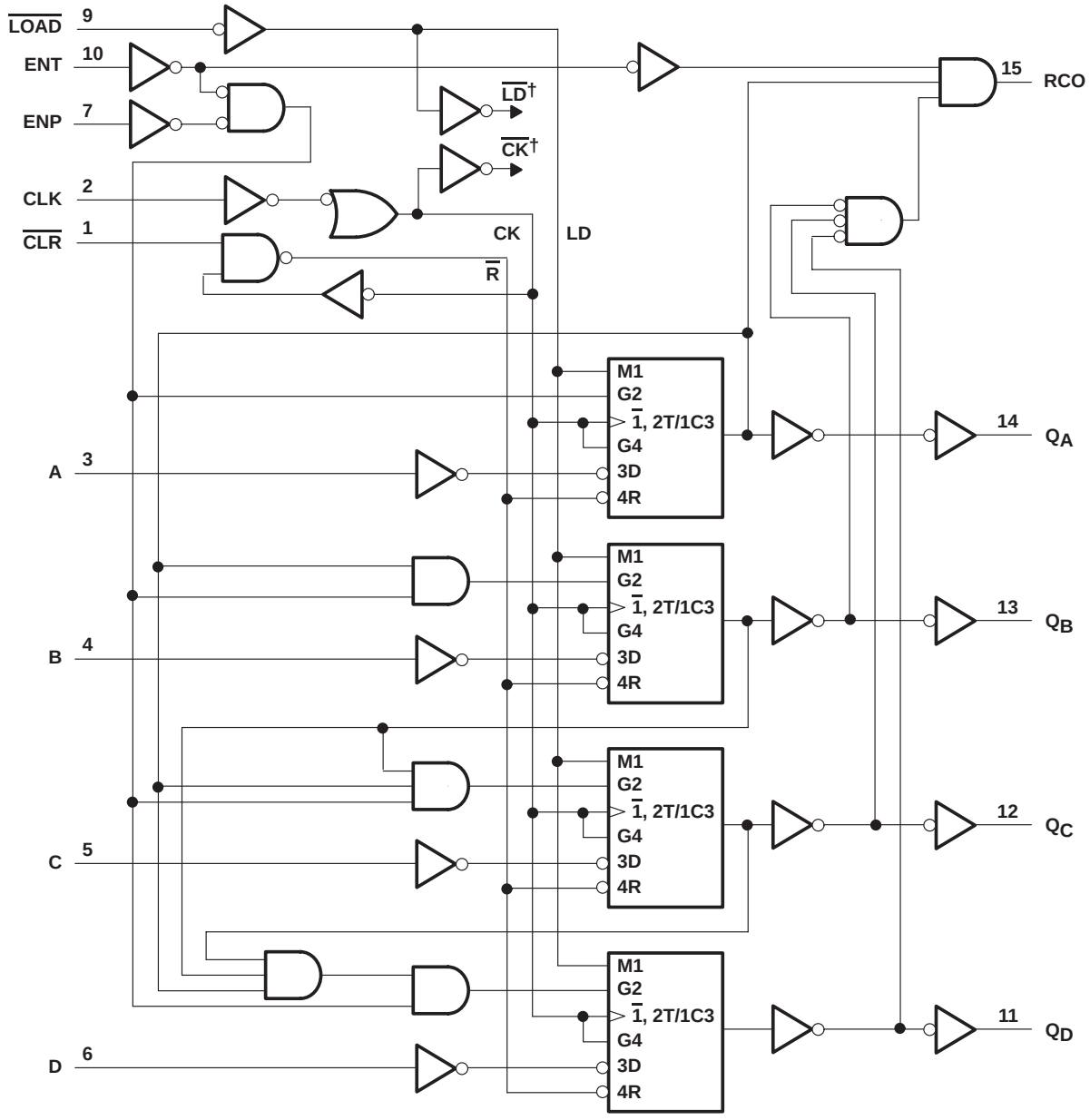
NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).

logic symbol†



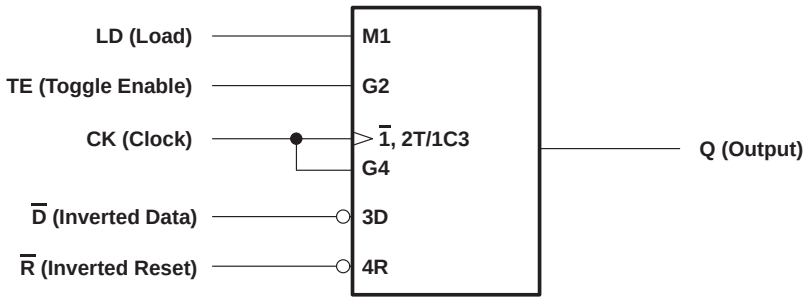
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

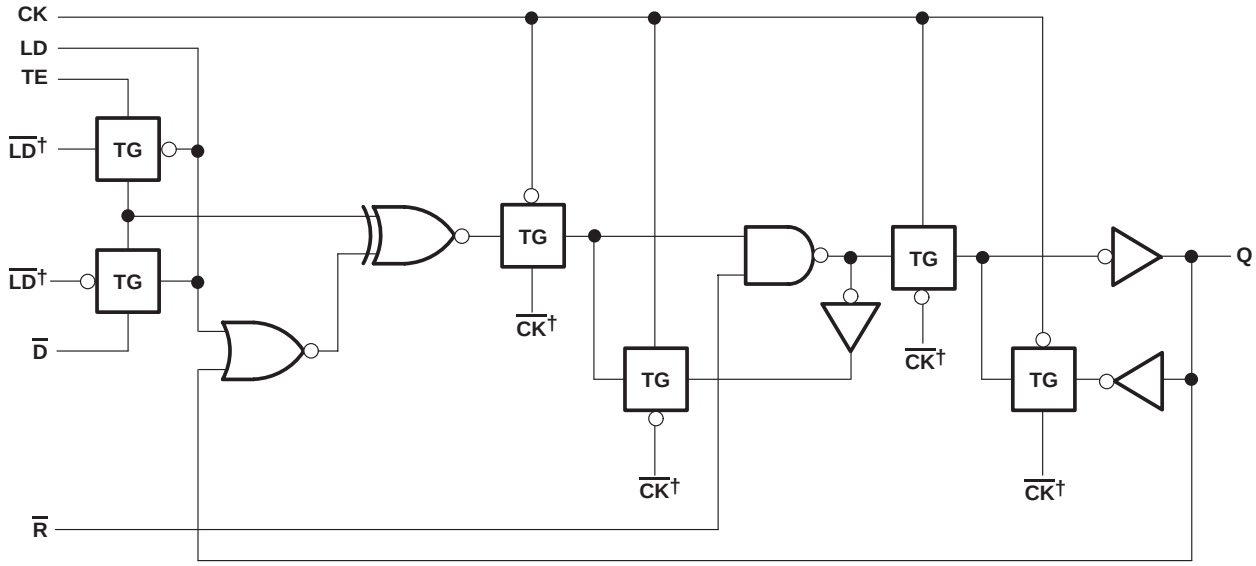


† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)



† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

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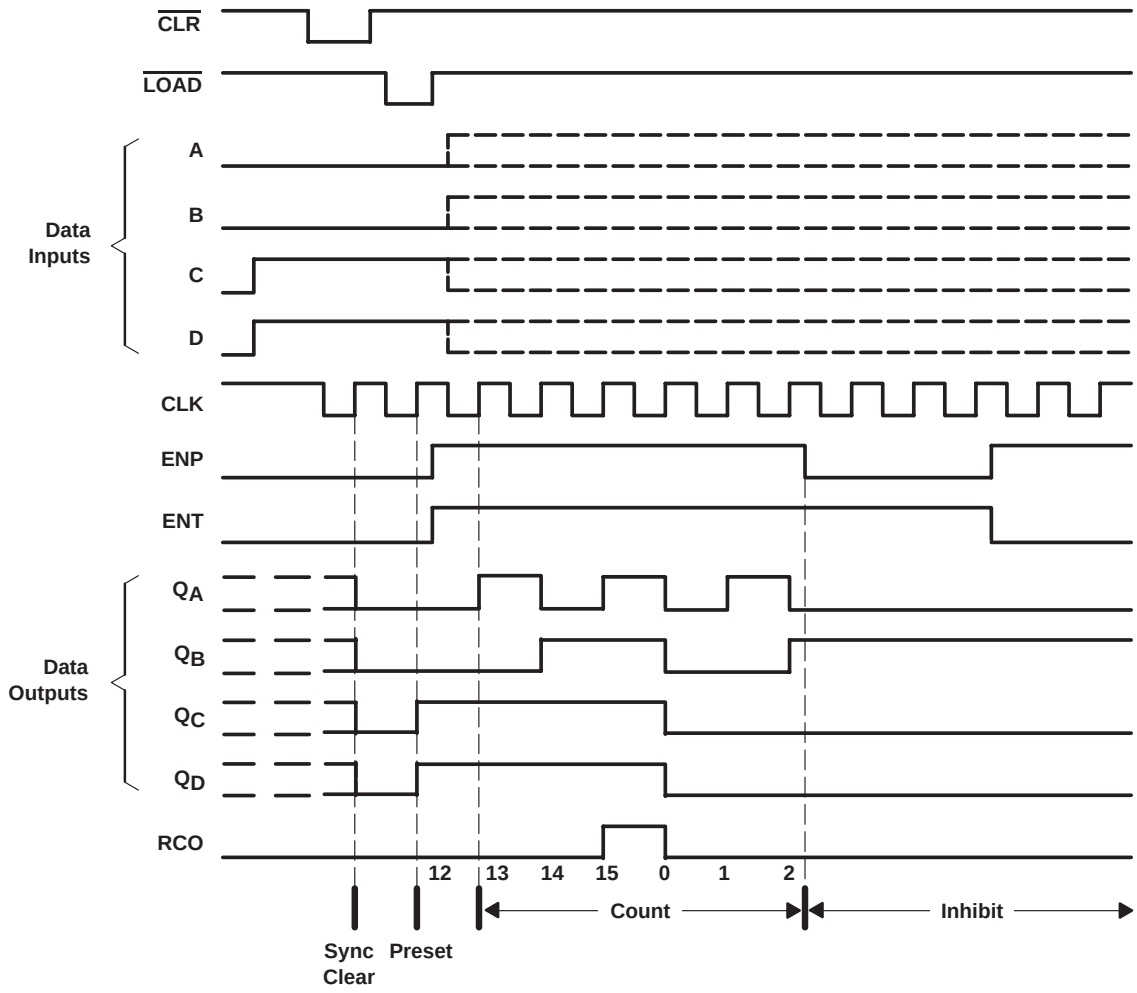
typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 2) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2) . . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): E package . . . . . 67°C/W
M package . . . . . 73°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			T_A = 25°C		CD54AC163		CD74AC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–24		–24	mA
I_{OL}	Low-level output current			24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V	0	50	0	50	0	50	ns
		V_{CC} = 3.6 V to 5.5 V	0	20	0	20	0	20	
T_A	Operating free-air temperature				– 55	125	– 40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		CD54AC163		CD74AC163		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –50 μA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58		2.4		2.48		
		I_{OH} = –24 mA	4.5 V	3.94		3.7		3.8		
		I_{OH} = –50 mA†	5.5 V	–		3.85		–		
		I_{OH} = –75 mA†	5.5 V	–		–		3.85		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 50 μA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V		0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V		0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V		–		1.65		–	
		I_{OL} = 75 mA†	5.5 V		–		–		1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V		8		160		80	μA
C_i					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	CD54AC163		CD74AC163		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		1.5 V		7		8	MHz
			3.3 V ± 0.3 V		64		73	
			5 V ± 0.5 V		90		103	
t_w	Pulse duration	CLK high or low	1.5 V	69		61		ns
			3.3 V ± 0.3 V	7.7		6.8		
			5 V ± 0.5 V	5.5		4.8		
t_{su}	Setup time, before CLK↑	A, B, C, or D	1.5 V	63		55		ns
			3.3 V ± 0.3 V	7		6.1		
			5 V ± 0.5 V	5		4.4		
		ENP or ENT	1.5 V	63		55		
			3.3 V ± 0.3 V	9.6		8.2		
			5 V ± 0.5 V	5		4.4		
		$\overline{LOAD}$ low	1.5 V	75		66		
			3.3 V ± 0.3 V	8.4		7.4		
			5 V ± 0.5 V	6		5.3		
		$\overline{CLR}$ inactive	1.5 V	75		66		
			3.3 V ± 0.3 V	8.4		7.4		
			5 V ± 0.5 V	6		5.3		
t_h	Hold time, after CLK↑	A, B, C, or D	1.5 V	0		0		ns
			3.3 V ± 0.3 V	0		0		
			5 V ± 0.5 V	0		0		
		ENP or ENT	1.5 V	0		0		
			3.3 V ± 0.3 V	0		0		
			5 V ± 0.5 V	0		0		
		$\overline{LOAD}$ low	1.5 V	0		0		
			3.3 V ± 0.3 V	0		0		
			5 V ± 0.5 V	0		0		
		$\overline{CLR}$ inactive	1.5 V	0		0		
			3.3 V ± 0.3 V	0		0		
			5 V ± 0.5 V	0		0		

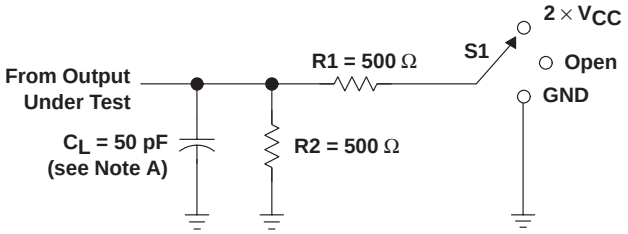
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	CD54AC163		CD74AC163		UNIT
				MIN	MAX	MIN	MAX	
f_{max}			1.5 V	7		8		MHz
			3.3 V ± 0.3 V	64		73		
			5 V ± 0.5 V	90		103		
t_{pd}	CLK	RCO	1.5 V	–	209	–	190	ns
			3.3 V ± 0.3 V	6	23.4	6	21	
			5 V ± 0.5 V	4.3	16.7	4.3	15.2	
		Any Q	1.5 V	–	207	–	188	
			3.3 V ± 0.3 V	5.9	23.1	5.9	21	
			5 V ± 0.5 V	4.2	16.5	4.2	15	
	ENT	RCO	1.5 V	–	129	–	117	
			3.3 V ± 0.3 V	3.6	14.4	3.7	13.1	
			5 V ± 0.5 V	2.6	10.3	2.7	9.4	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	66	pF

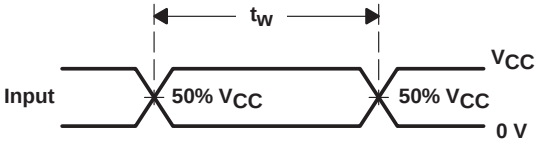
PARAMETER MEASUREMENT INFORMATION



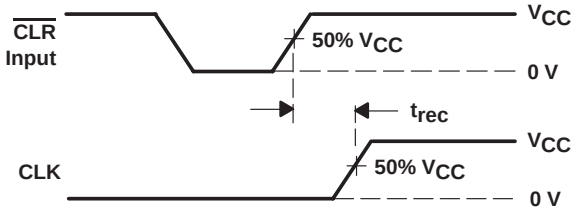
NOTE When V_{CC} = 1.5 V, R1 and R2 = 1 kΩ.

LOAD CIRCUIT

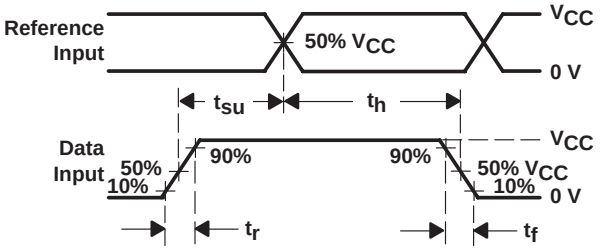
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



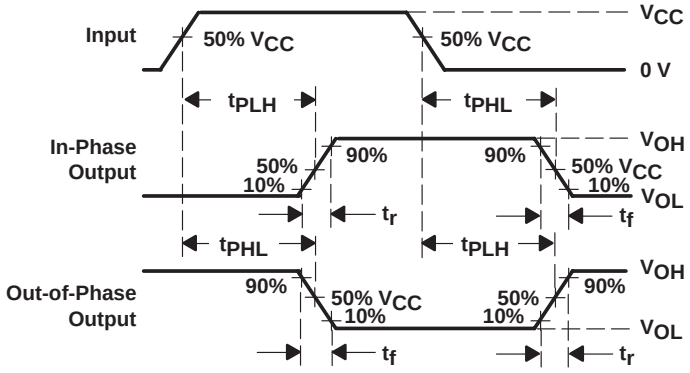
VOLTAGE WAVEFORMS
PULSE DURATION



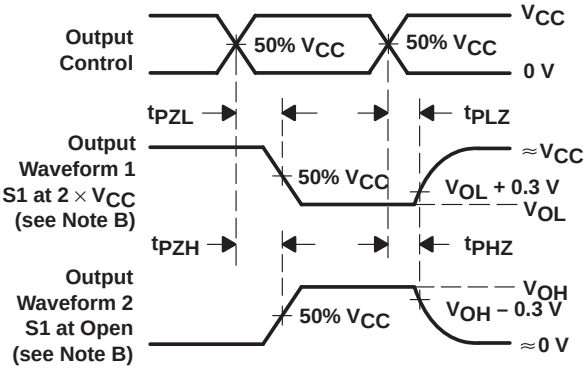
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 1. Load Circuit and Voltage Waveforms

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