

# CD74HC4518, CD74HC4520, CD74HCT4520

## High Speed CMOS Logic Dual Synchronous Counters

### Features

- Positive or Negative Edge Triggering
- Synchronous Internal Carry Propagation
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC4518 is a dual BCD up-counter. The Harris CD74HC4520 and CD74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting  $Q_3$  to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

### Ordering Information

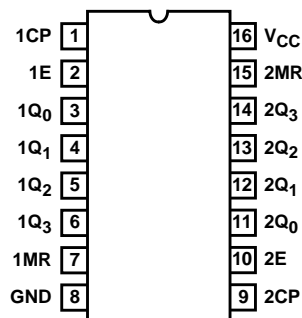
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4518E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4520E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4520E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4520M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4520M	-55 to 125	16 Ld SOIC	M16.15

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

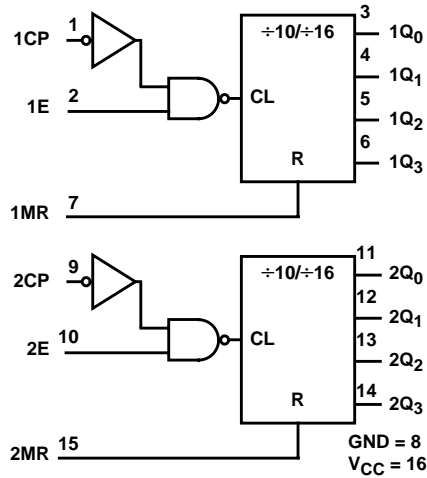
### Pinout

CD74HC4518  
CD74HC4520, CD74HCT4520  
(PDIP, SOIC)  
TOP VIEW



CD74HC4518, CD74HC4520, CD74HCT4520

Functional Diagram



TRUTH TABLE

CP	E	MR	OUTPUT STATE
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q <sub>0</sub> thru Q <sub>3</sub> = L

NOTE:

- H = High State.
- L = Low State.
- ↑ = High-to-Low Transition.
- ↓ = Low-to-High Transition.
- X = Don't Care.

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### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
PDIP Package .....	90
SOIC Package .....	160
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	.4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

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**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
MR	1.2
CP	0.25
ENABLE	0.5

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

**Prerequisite for Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
Maximum Clock Frequency	f <sub>MAX</sub>	2	6	-	-	5	-	4	-	MHz
		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
CP Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR Pulse Width	t <sub>W</sub>	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns

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**Prerequisite for Switching Specifications (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Set-up Time, Enable to CP	t <sub>SU</sub>	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time, MR to CP	t <sub>REM</sub>	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Set-up Time, CP to Enable	t <sub>SU</sub>	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time, MR to Enable	t <sub>REM</sub>	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns

**HCT TYPES**

Maximum Clock Frequency	f <sub>MAX</sub>	4.5	25	-	-	20	-	17	-	MHz
Clock Pulse Width	t <sub>W</sub>	4.5	20	-	-	25	-	30	-	ns
MR Pulse Width	t <sub>W</sub>	4.5	20	-	-	25	-	30	-	ns
Set-up, Time Enable to CP	t <sub>SU</sub>	4.5	16	-	-	20	-	24	-	ns
Removal Time, MR to Enable	t <sub>REM</sub>	4.5	0	-	-	0	-	0	-	ns

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay CP to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	240	-	300	-	360	ns
		C <sub>L</sub> = 50pF	4.5	-	-	48	-	60	-	72	ns
		C <sub>L</sub> = 15pF	5	-	20	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	41	-	51	-	61	ns
Enable to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	240	-	300	-	360	ns
		C <sub>L</sub> = 50pF	4.5	-	-	48	-	60	-	72	ns
		C <sub>L</sub> = 15pF	5	-	20	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	41	-	51	-	61	ns
MR to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	150	-	190	-	225	ns
		C <sub>L</sub> = 50pF	4.5	-	-	30	-	38	-	45	ns
		C <sub>L</sub> = 15pF	5	-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
		C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
		C <sub>L</sub> = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Note 4, 5)	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	33	-	-	-	-	-	pF

## CD74HC4518, CD74HC4520, CD74HCT4520

### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>											
Propagation Delay CP to $Q_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	53	-	66	-	80	ns
		$C_L = 15\text{pF}$	5	-	22	-	-	-	-	-	ns
Enable to $Q_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
MR to $Q_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Note 4,5)	$C_{PD}$	-	5	-	33	-	-	-	-	-	pF

**NOTES:**

4.  $C_{PD}$  is used to determine the dynamic power consumption, per counter.
5.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Timing Diagram

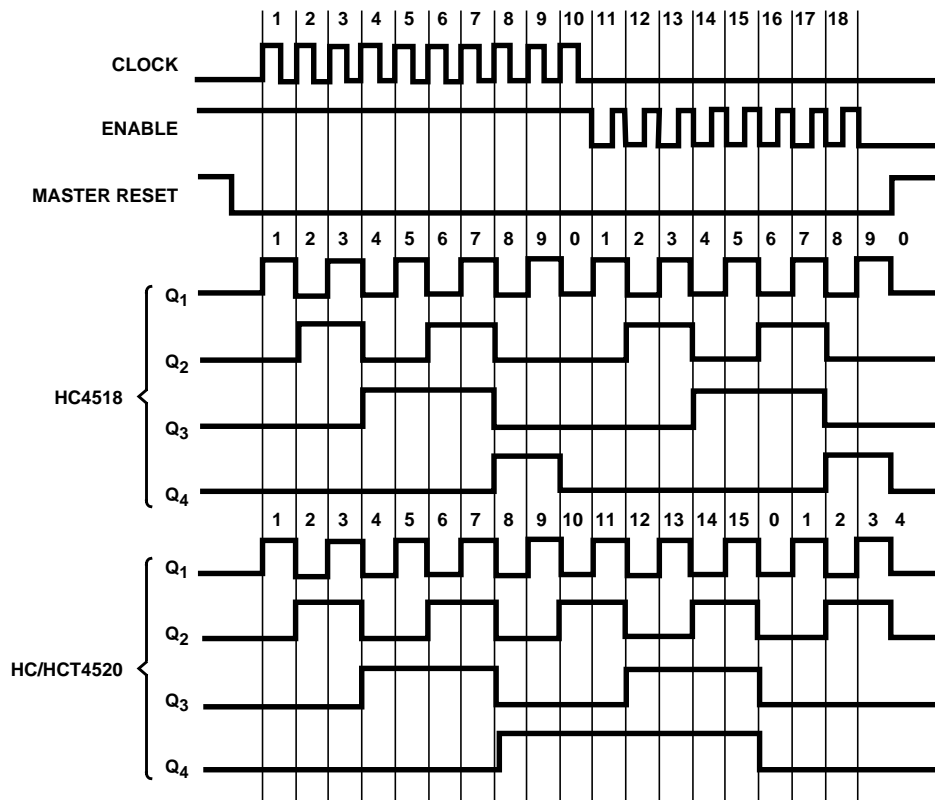
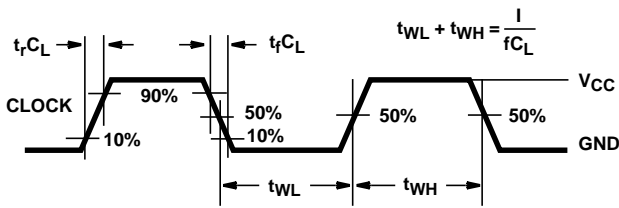


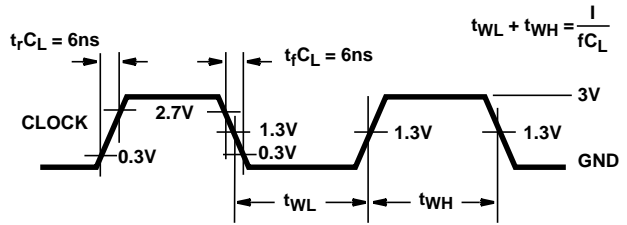
FIGURE 6.

Waveforms



NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For f<sub>MAX</sub>, input duty cycle = 50%.

FIGURE 7. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For f<sub>MAX</sub>, input duty cycle = 50%.

FIGURE 8. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

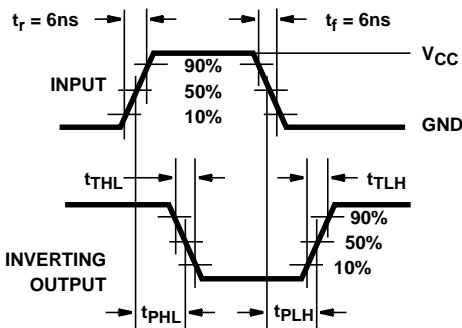


FIGURE 9. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

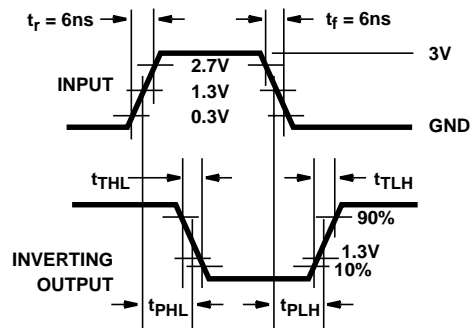


FIGURE 10. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

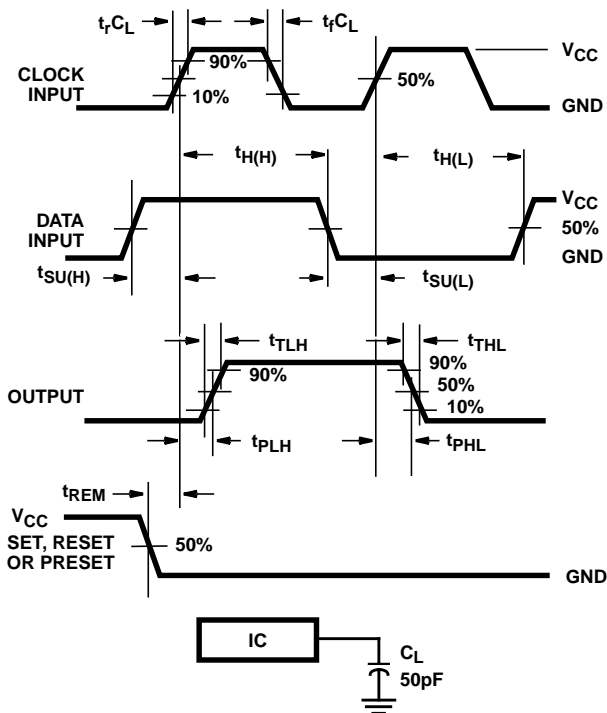


FIGURE 11. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

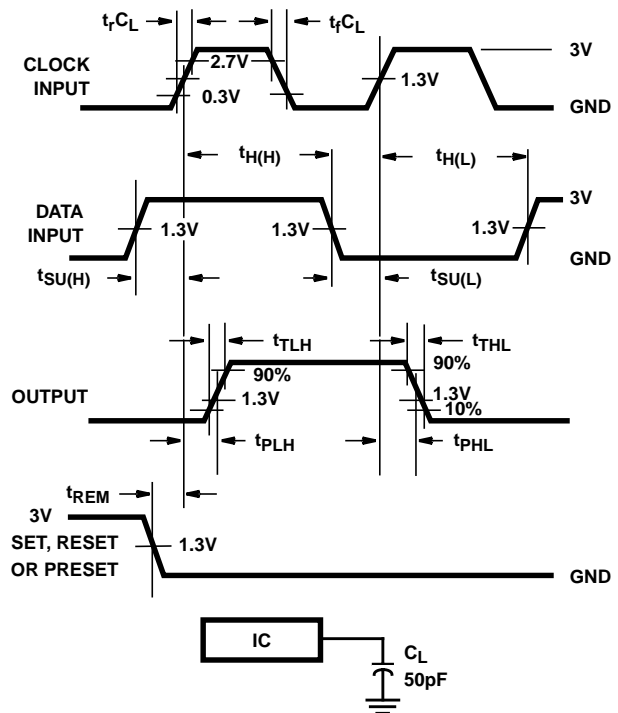


FIGURE 12. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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