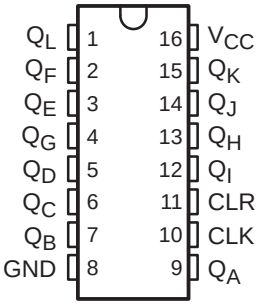
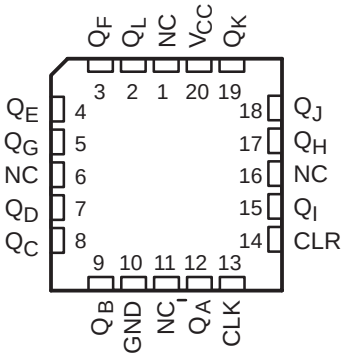
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic (J) DIPs**

SN54LV4040A . . . J OR W PACKAGE
SN74LV4040A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV4040A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

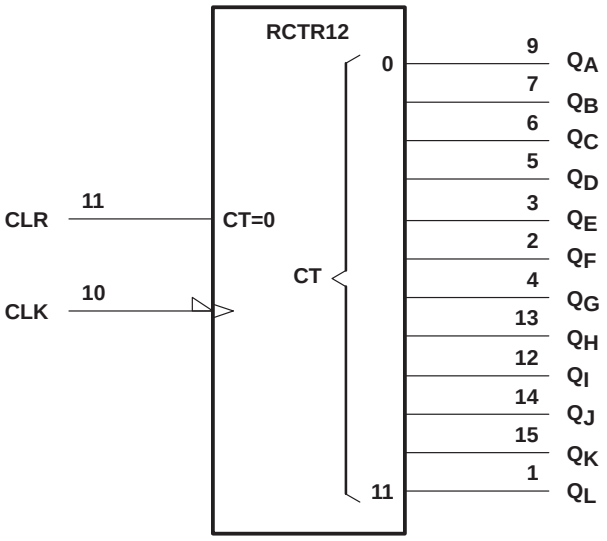
The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN54LV4040A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV4040A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

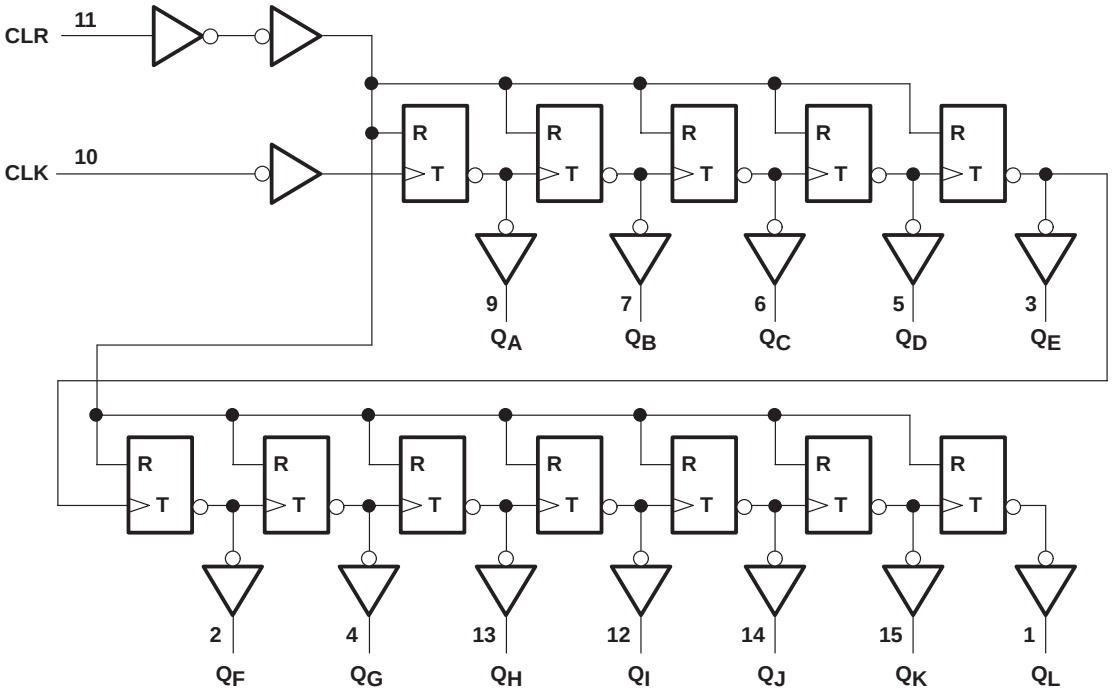
INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
DGV package . . . . . 120°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV4040A			SN74LV4040A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –6 mA	3 V	2.48			2.48			
	I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	5.5 V			±1			±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		1.9			1.9		pF
		5 V		1.8			1.8		

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C	SN54LV4040A	SN74LV4040A	UNIT
			MIN MAX	MIN MAX	MIN MAX	
t_w	Pulse duration	CLK high or low	7	7	7	ns
		CLR high	6.5	6.5	6.5	
t_{su}	Setup time	CLR inactive before CLK↓	6.5	6.5	6.5	ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C	SN54LV4040A	SN74LV4040A	UNIT
			MIN MAX	MIN MAX	MIN MAX	
t_w	Pulse duration	CLK high or low	5	5	5	ns
		CLR high	5	5	5	
t_{su}	Setup time	CLR inactive before CLK↓	5	5	5	ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C	SN54LV4040A	SN74LV4040A	UNIT
			MIN MAX	MIN MAX	MIN MAX	
t_w	Pulse duration	CLK high or low	5	5	5	ns
		CLR high	5	5	5	
t_{su}	Setup time	CLR inactive before CLK↓	5	5	5	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	50	115		40		40		MHz
			C_L = 50 pF	40	95		35		35		
t_{PLH}*	CLK	Q_A	C_L = 15 pF		8.7	19.4	1	23	1	23	ns
t_{PHL}*					8.7	19.4	1	23	1	23	
t_{PHL}*	CLR	Any Q	C_L = 15 pF		9.3	19.9	1	24	1	24	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		10.5	24.1	1	28	1	28	ns
t_{PHL}					10.5	24.1	1	28	1	28	
t_{PHL}	CLR	Any Q	C_L = 50 pF		11.7	24.5	1	28	1	28	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.7	5.9		7		7	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	75	160		75		75		MHz
			C_L = 50 pF	55	130		50		50		
t_{PLH}*	CLK	Q_A	C_L = 15 pF		6.1	11.9	1	14	1	14	ns
t_{PHL}*					6.1	11.9	1	14	1	14	
t_{PHL}*	CLR	Any Q	C_L = 15 pF		7.1	12.8	1	15	1	15	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		7.5	15.4	1	17.5	1	17.5	ns
t_{PHL}					7.5	15.4	1	17.5	1	17.5	
t_{PHL}	CLR	Any Q	C_L = 50 pF		9	16.3	1	18.5	1	18.5	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.2	4.4		5		5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	150	235		125		125		MHz
			C_L = 50 pF	95	185		80		80		
t_{PLH}*	CLK	Q_A	C_L = 15 pF		4.2	7.3	1	8.5	1	8.5	ns
t_{PHL}*					4.2	7.3	1	8.5	1	8.5	
t_{PHL}*	CLR	Any Q	C_L = 15 pF		5.3	8.6	1	10	1	10	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		5.3	9.3	1	10.5	1	10.5	ns
t_{PHL}					5.3	9.3	1	10.5	1	10.5	
t_{PHL}	CLR	Any Q	C_L = 50 pF		6.8	10.6	1	12	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		0.8	3.1		3.5		3.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

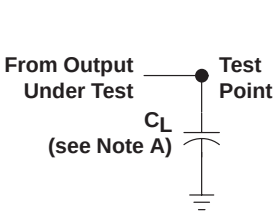
PARAMETER		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

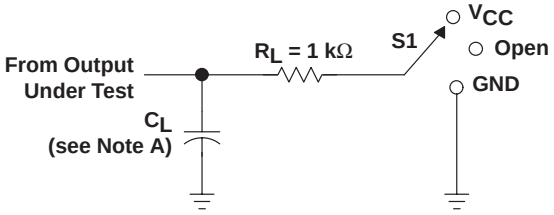
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	11.9	pF
			5 V	13.1	

PARAMETER MEASUREMENT INFORMATION

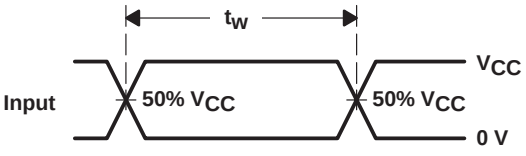


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

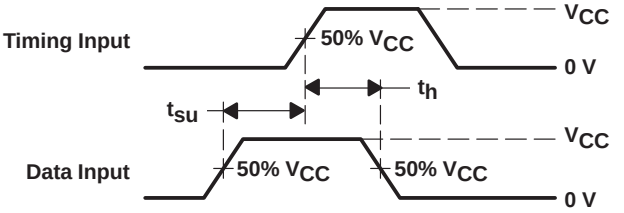


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

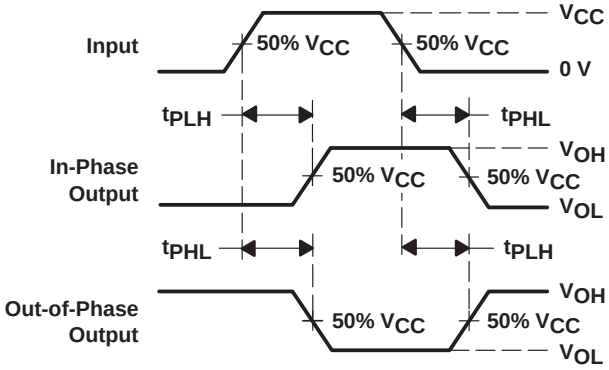
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



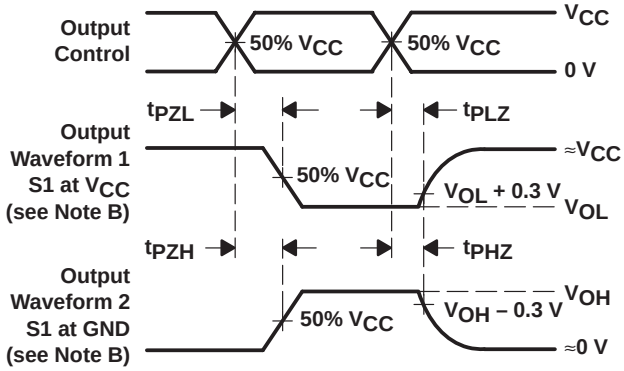
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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