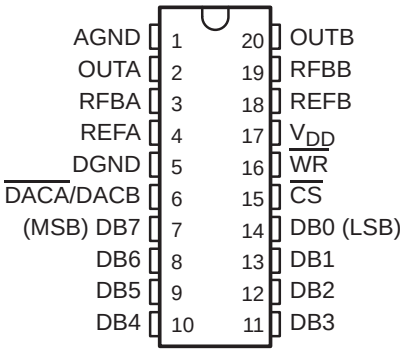
# TLC7628C, TLC7628E, TLC7628I
# DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS063A – APRIL 1989 – REVISED MAY 1995

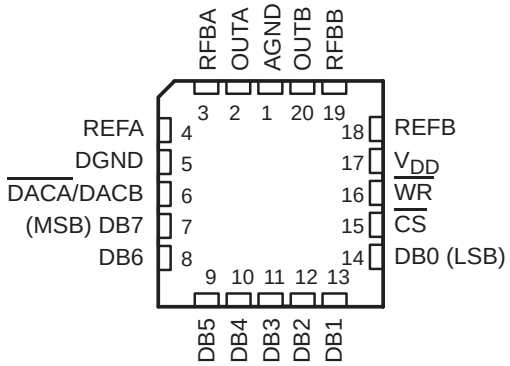
- **Easy Microprocessor Interface**
- **On-Chip Data Latches**
- **Digital Inputs Are TTL-Compatible With 10.8-V to 15.75-V Power Supply**
- **Monotonic Over the Entire A/D Conversion Range**
- **Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320**
- **CMOS Technology**

| KEY PERFORMANCE SPECIFICATIONS | |
|---|---|
| Resolution | 8 bits |
| Linearity Error | 1/2 LSB |
| Power Dissipation | 20 mW |
| Settling Time | 100 ns |
| Propagation Delay Time | 80 ns |

**DW OR N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




## description

The TLC7628C, TLC7628E, and TLC7628I are dual, 8-bit, digital-to-analog converters (DACs) designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit input port. Control input $\overline{\text{DACA}}$/DACB determines which DAC is loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The TLC7628C operates from a 10.8-V to 15.75-V power supply and is TTL-compatible over this range. 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7628C is characterized for operation from 0°C to 70°C. The TLC7628I is characterized for operation from –25°C to 85°C. The TLC7628E is characterized for operation from –40°C to 85°C.

**AVAILABLE OPTIONS**

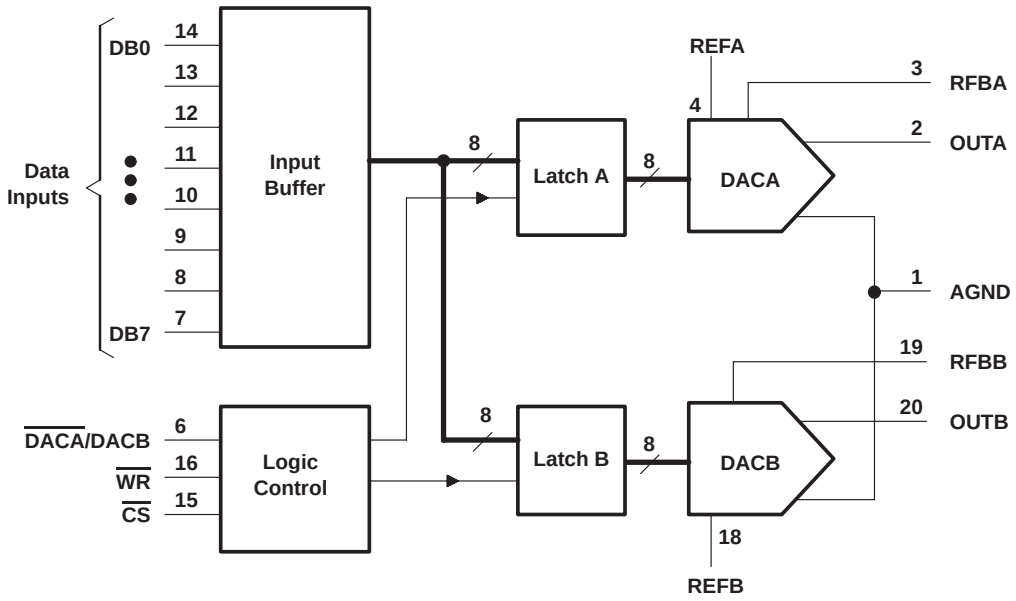
| $T_A$ | PACKAGE | | |
|---|---|---|---|
| | SMALL OUTLINE PLASTIC DIP (DW) | PLASTIC CHIP CARRIER (FN) | PLASTIC DIP (N) |
| 0°C to 70°C | TLC7628CDW | TLC7628CFN | TLC7628CN |
| –25°C to 85°C | TLC7628IDW | TLC7628IFN | TLC7628IN |
| –40°C to 85°C | TLC7628EDW | TLC7628EFN | TLC7628EN |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1995, Texas Instruments Incorporated

## functional block diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ (to AGND or DGND) . . . . . –0.3 V to 17 V
Voltage between AGND and DGND . . . . . $V_{DD}$
Input voltage range, $V_I$ (to DGND) . . . . . –0.3 V to $V_{DD}$ + 0.3 V
Reference voltage range, $V_{refA}$ or $V_{refB}$ (to AGND) . . . . . ±25 V
Feedback voltage range, $V_{RFBA}$ or $V_{RFBB}$ (to AGND) . . . . . ±25 V
Output voltage range, $V_{OA}$ or $V_{OB}$ (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 µA
Operating free-air temperature range, $T_A$: TLC7628C . . . . . 0°C to 70°C
TLC7628I . . . . . –25°C to 85°C
TLC7628E . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Case temperature for 10 seconds, $T_C$: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 10.8 | | 15.75 | V |
| Reference voltage, $V_{refA}$ or $V_{refB}$ | | | ±10 | | V |
| High-level input voltage, $V_{IH}$ | | 2.4 | | | V |
| Low-level input voltage, $V_{IL}$ | | | | 0.8 | V |
| $\overline{CS}$ setup time, $t_{su(CS)}$ | | 50 | | | ns |
| $\overline{CS}$ hold time, $t_{h(CS)}$ (see Figure 1) | | 0 | | | ns |
| DAC select setup time, $t_{su(DAC)}$ (see Figure 1) | | 60 | | | ns |
| DAC select hold time, $t_{h(DAC)}$ (see Figure 1) | | 10 | | | ns |
| Data bus input setup time $t_{su(D)}$ (see Figure 1) | | 25 | | | ns |
| Data bus input hold time $t_{h(D)}$ (see Figure 1) | | 10 | | | ns |
| Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$ (see Figure 1) | | 50 | | | ns |
| Operating free-air temperature, $T_A$ | TLC7628C | 0 | | 70 | °C |
| | TLC7628I | –25 | | 85 | |
| | TLC7628E | –40 | | 85 | |

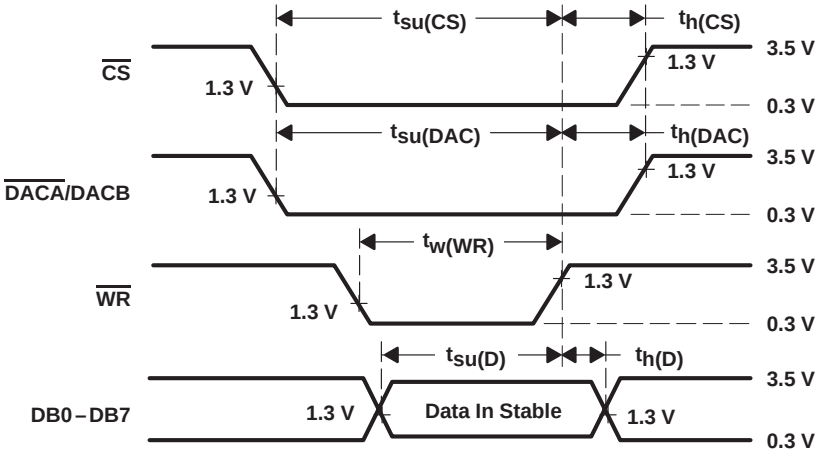
## electrical characteristics over recommended ranges of operating free-air temperature and $V_{DD}$, $V_{refA} = V_{refB} = 10$ V, $V_{OA}$ and $V_{OB}$ at 0 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | High-level input current | | $V_I = V_{DD}$ | Full range | | 10 | µA |
| | | | | 25°C | | 1 | |
| $I_{IL}$ | Low-level input current | | $V_I = 0$ | Full range | | –10 | µA |
| | | | | 25°C | | –1 | |
| | Reference input impedance REFA or REFB to AGND | | | | 5 | 20 | kΩ |
| $I_{kg}$ | Output leakage current | OUTA | DAC data latch loaded with 00000000, $V_{refA}$ = ±10 V | Full range | | ±200 | nA |
| | | | | 25°C | | ±50 | |
| | | OUTB | DAC data latch loaded with 00000000, $V_{refB}$ = ±10 V | Full range | | ±200 | |
| | | | | 25°C | | ±50 | |
| | Input resistance match (REFA to REFB) | | | | | ±1% | |
| | DC supply sensitivity Δgain/Δ$V_{DD}$ | | Δ$V_{DD}$ = ± 5 % | Full range | | 0.02 | %/% |
| | | | | 25°C | | 0.01 | |
| $I_{DD}$ | Supply current | Quiescent | All digital inputs at $V_{IH}$min or $V_{IL}$max | | | 2 | mA |
| | | Standby | All digital inputs at 0 V or $V_{DD}$ | Full range | | 0.5 | |
| | | | | 25°C | | 0.1 | |
| $C_i$ | Input capacitance | DB0–DB7 | | | | 10 | pF |
| | | $\overline{WR}$, $\overline{CS}$, DACA/DACB | | | | 15 | |
| $C_o$ | Output capacitance (OUTA, OUTB) | | DAC data latches loaded with 00000000 | | | 25 | pF |
| | | | DAC data latches loaded with 11111111 | | | 60 | |

## operating characteristics over recommended ranges of operating free-air temperature and $V_{DD}$, $V_{refA} = V_{refB} = 10$ V, $V_{OA}$ and $V_{OB}$ at 0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Linearity error | | | | | | ±1/2 | LSB |
| Settling time (to 1/2 LSB) | | See Note 1 | | | | 100 | ns |
| Gain error | | See Note 2 | Full range | | | ±3 | LSB |
| | | | 25°C | | | ±2 | |
| AC feedthrough | REFA to OUTA | See Note 3 | Full range | | | –65 | dB |
| | REFB to OUTB | | 25°C | | | –75 | |
| Temperature coefficient of gain | | | | | | ±0.0035 | %FSR/°C |
| Propagation delay (from digital input to 90% of final analog output current) | | See Note 4 | | | | 80 | ns |
| Channel-to-channel isolation | REFA to OUTB | See Note 5 | 25°C | | 80 | | dB |
| | REFB to OUTA | See Note 6 | 25°C | | 80 | | |
| Digital-to-analog glitch impulse area | | Measured for code transition from 00000000 to 11111111, $T_A$ = 25°C | | | 330 | | nV•s |
| Digital crosstalk | | Measured for code transition from 00000000 to 11111111, $T_A$ = 25°C | | | 60 | | nV•s |
| Harmonic distortion | | $V_i$ = 6 V, f = 1 kHz, $T_A$ = 25°C | | | –85 | | dB |

NOTES: 1. OUTA, OUTB load = 100 Ω, $C_{ext}$ = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to $V_{DD}$ or $V_{DD}$ to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) = $V_{ref}$ – 1 LSB. Both DAC latches are loaded with 11111111.
3. $V_{ref}$ = 20 V peak-to-peak, 10-kHz sine wave
4. $V_{refA} = V_{refB}$ = 10 V; OUTA/OUTB load = 100 Ω, $C_{ext}$ = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0–DB7 at 0 V to $V_{DD}$ or $V_{DD}$ to 0 V.
5. $V_{refA}$ = 20 V peak-to-peak, 10-kHz sine wave; $V_{refB}$ = 0
6. $V_{refB}$ = 20 V peak-to-peak, 10-kHz sine wave; $V_{refA}$ = 0

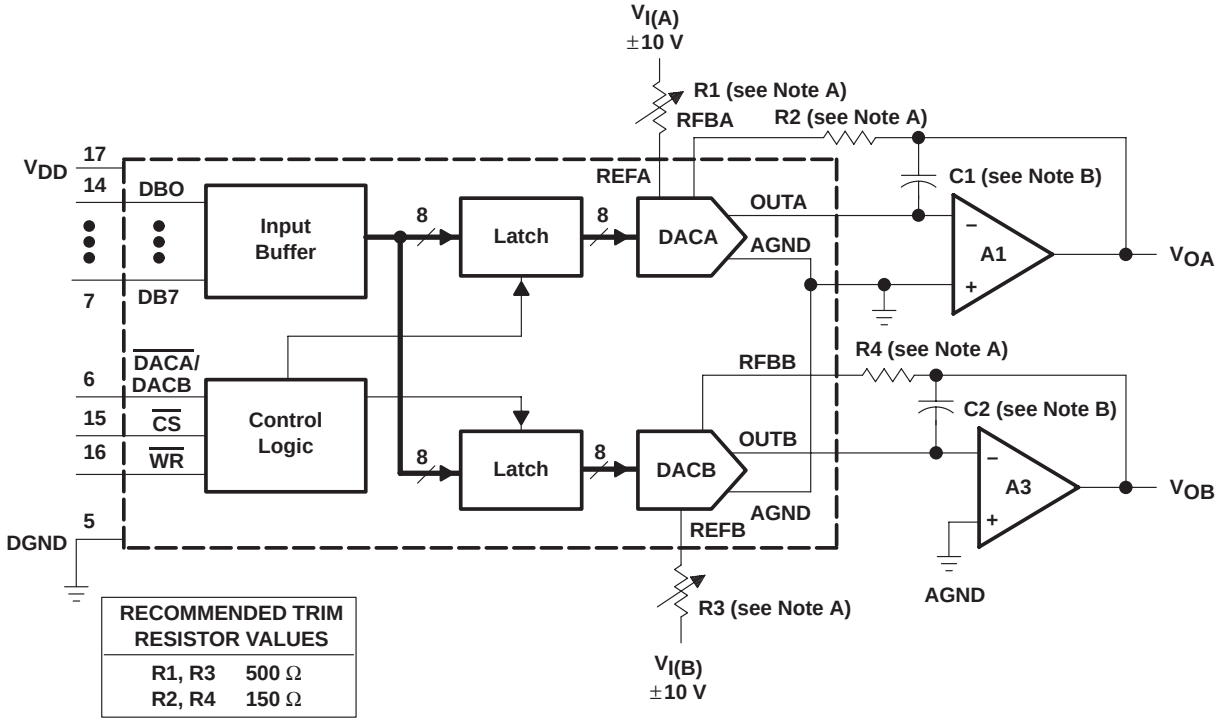



For all input signals, $t_r = t_f$ = 5 ns (10% to 90% points).

**Figure 1. Setup and Hold Times**

## APPLICATION INFORMATION

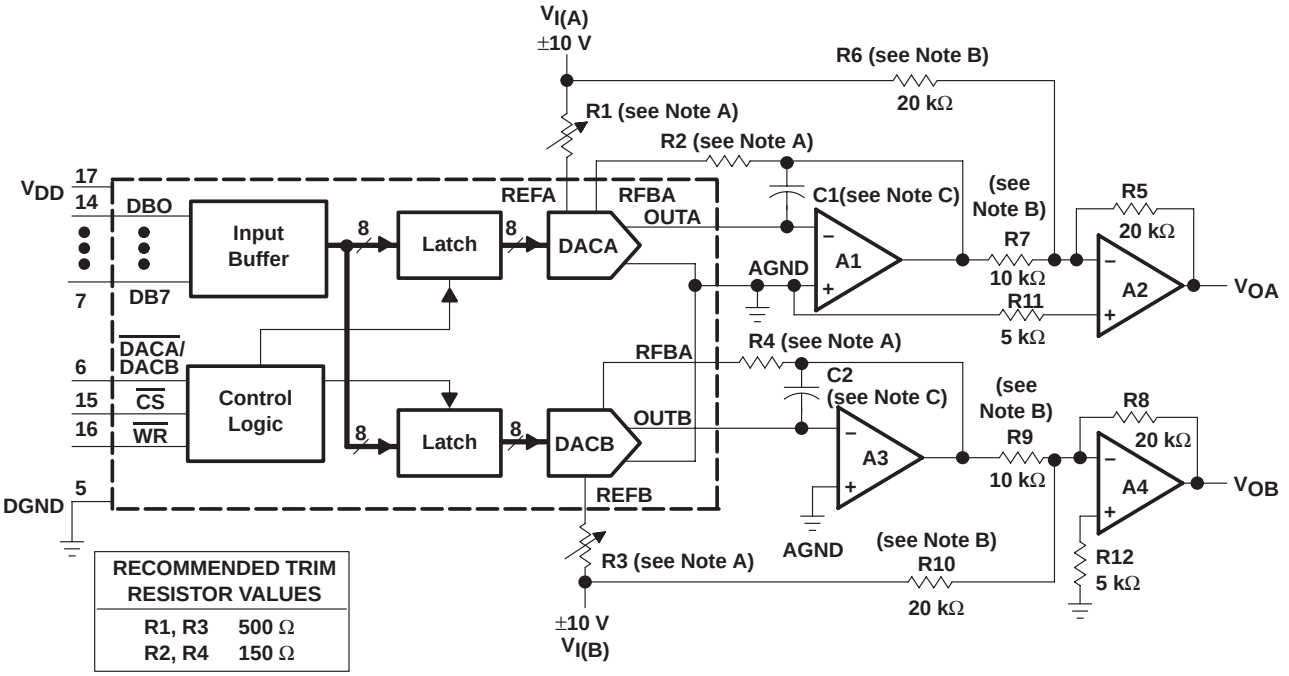
These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 2 and 3, respectively.




NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
B. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

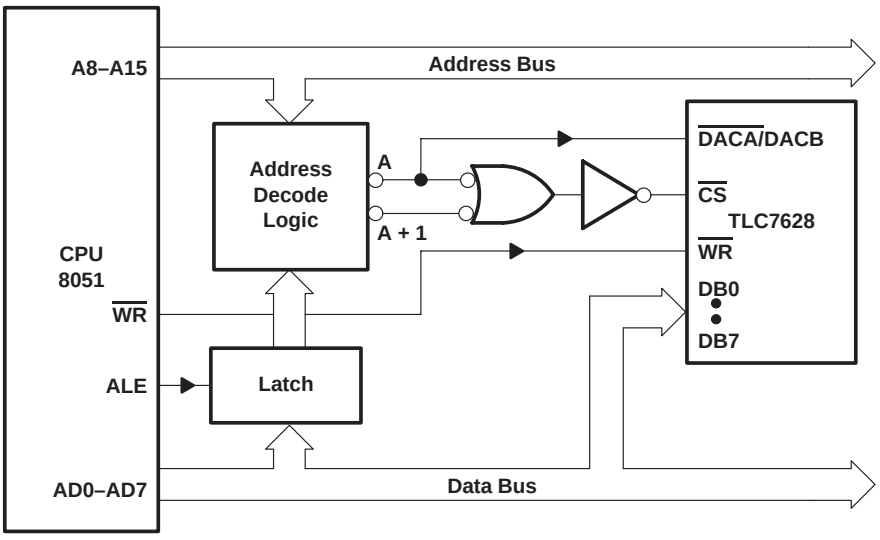
**Figure 2. Unipolar Operation (2-Quadrant Multiplication)**

## APPLICATION INFORMATION




NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Adjust R1 for $V_{OA}$ = 0 V with code 10000000 in DACA latch. Adjust R3 for $V_{OB}$ = 0 V with 10000000 in DACB latch.
B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
C. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

**Figure 3. Bipolar Operation (4-Quadrant Operation)**

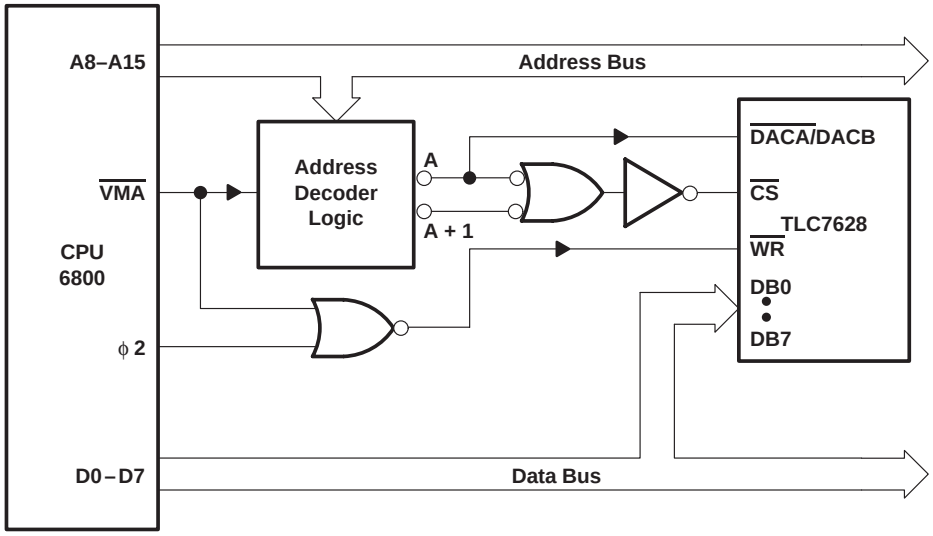



NOTE D: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

**Figure 4. TLC7628 — Intel 8051 Interface**


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## APPLICATION INFORMATION




NOTE D: A = decoded address for TLC7628 DACA
A + 1 = decoded address for TLC7628 DACB

**Figure 5. TLC7628 – 6800 Interface**

### voltage-mode operation

The current-multiplying DAC in these devices can be operated in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. An example of a current-multiplying DAC operating in voltage mode is shown in Figure 6. The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

Analog output voltage = fixed input voltage (D/256)

where D = the digital input. In voltage-mode operation, these devices meet the following specification:

| LINEARITY ERROR | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Analog output voltage for REFA, REFB | $V_{DD}$ = 12 V, OUTA or OUTB at 5 V, $T_A$ = 25°C | | 1 | LSB |

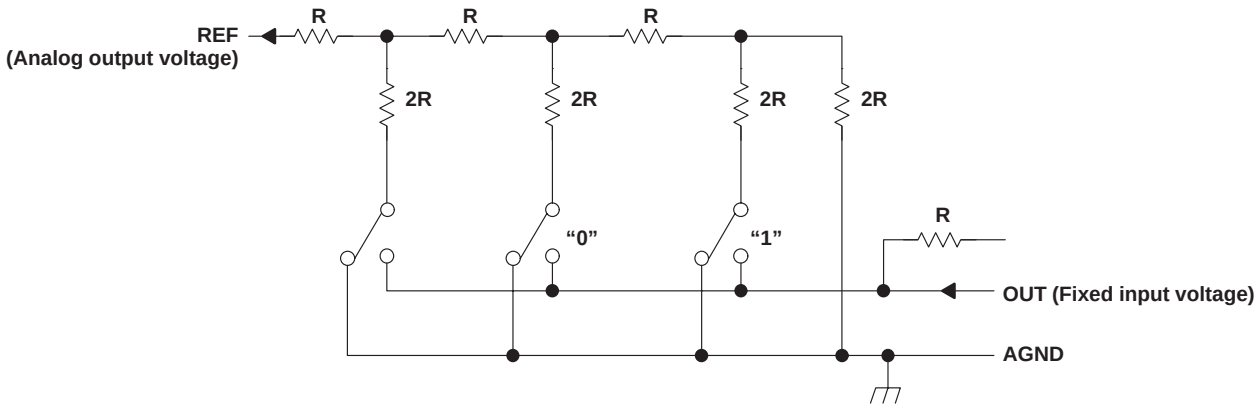



**Figure 6. Current-Multiplying DAC Operating in Voltage Mode**

## PRINCIPLES OF OPERATION

These devices contain two, identical, 8-bit, multiplying DACs: DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between the DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA or DACB with all digital inputs low is shown in Figure 7.

Figure 8 shows the DACA or DACB equivalent circuit. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the reference current flows to OUTA. A small leakage current ($I_{lkg}$) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. The $C_o$ is caused by the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of $C_o$ is 25 pF to 60 pF maximum. The equivalent output resistance ($r_o$) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the analog output on these devices, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled, regardless of the state of the $\overline{WR}$ signal.

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 10.8 V to 15.75 V.

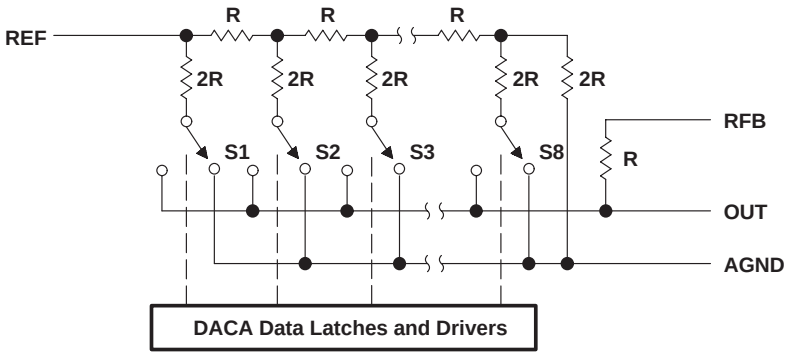



**Figure 7. Simplified Functional Circuit for DACA or DACB**

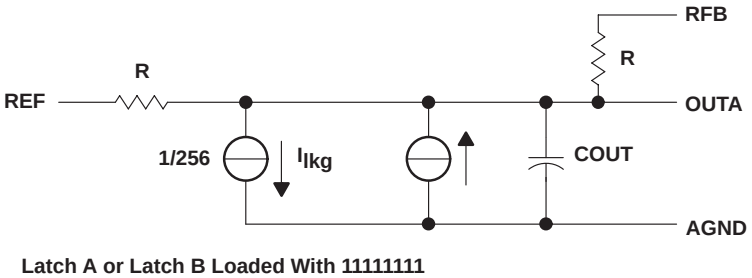



**Figure 8. TLC7628 Equivalent Circuit for DACA or DACB**

## PRINCIPLES OF OPERATION

**Table 1. Mode Selection Table**

| $\overline{DACA}$/DACB | $\overline{CS}$ | $\overline{WR}$ | DACA | DACB |
|---|---|---|---|---|
| L | L | L | Write | Hold |
| H | L | L | Hold | Write |
| X | H | X | Hold | Hold |
| X | X | H | Hold | Hold |

L = low level, H = high level, X = don't care

**Table 2. Unipolar Binary Code**

| DAC LATCH CONTENTS (see Note 7) MSB LSB | ANALOG OUTPUT |
|---|---|
| 1 1 1 1 1 1 1 1 | $-V_I$ (255/256) |
| 1 0 0 0 0 0 0 1 | $-V_I$ (129/256) |
| 1 0 0 0 0 0 0 0 | $-V_I$ (128/256) = $-V_i/2$ |
| 0 1 1 1 1 1 1 1 | $-V_I$ (127/256) |
| 0 0 0 0 0 0 0 1 | $-V_I$ (1/256) |
| 0 0 0 0 0 0 0 0 | $-V_I$ (0/256) = 0 |

**Table 3. Bipolar (Offset Binary) Code**

| DAC LATCH CONTENTS (see Note 8) MSB LSB | ANALOG OUTPUT |
|---|---|
| 1 1 1 1 1 1 1 1 | $V_I$ (127/128) |
| 1 0 0 0 0 0 0 1 | $V_I$ (1/128) |
| 1 0 0 0 0 0 0 0 | 0 V |
| 0 1 1 1 1 1 1 1 | $-V_I$ (1/128) |
| 0 0 0 0 0 0 0 1 | $-V_I$ (127/128) |
| 0 0 0 0 0 0 0 0 | $-V_I$ (128/128) |

NOTES: 7. 1 LSB = $(2^{-8})V_I$
8. 1 LSB = $(2^{-7})V_I$

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated