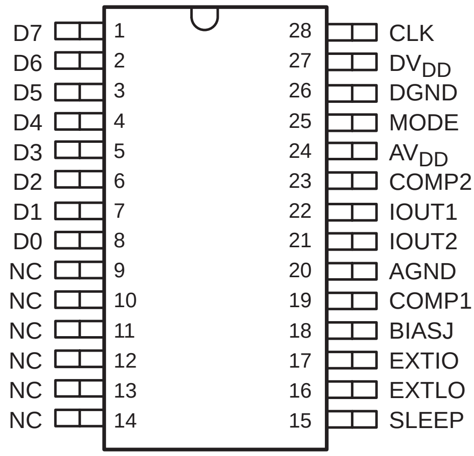
- **Member of the Pin-Compatible CommsDAC™ Product Family**
- **100 MSPS Update Rate**
- **8-Bit Resolution**
- **Signal-to-Noise and Distortion Ratio (SINAD) at 5 MHz: 50 dB**
- **Integral Nonlinearity INL: 0.25 LSB**
- **Differential Nonlinearity DNL: 0.25 LSB**
- **1 ns Setup/Hold Time**
- **Glitch Energy: 5 pV-s**
- **Settling Time to 0.1%: 35 ns**
- **Differential Scalable Current Outputs: 2 mA to 20 mA**
- **On-Chip 1.2-V Reference**
- **3-V and 5-V Single Supply Operation**
- **Straight Binary or Twos Complement Input**
- **Power Dissipation: 100 mW at 3.3 V, Sleep Mode: 17 mW at 3.3 V**
- **Package: 28-Pin SOIC and TSSOP**

SOIC (DW) OR TSSOP (PW) PACKAGE
(TOP VIEW)



NC – No internal connection

description

The THS5641 is an 8-bit resolution digital-to-analog converter (DAC) optimized for video applications and digital data transmission in wired and wireless communication systems. The 8-bit DAC is a member of the CommsDAC series of high-speed, low-power CMOS digital-to-analog converters. The CommsDAC family consists of pin compatible 14-, 12-, 10-, and 8-bit DACs. All devices offer identical interface options, small outline package and pinout. The THS5641 offers superior ac and dc performance while supporting update rates up to 100 MSPS.

The THS5641 operates from an analog and digital supply of 3 V to 5.5 V. Its inherent low power dissipation of 100 mW ensures that the device is well suited for portable and low power applications. Lowering the full-scale current output reduces the power dissipation without significantly degrading performance. The device features a SLEEP mode, which reduces the standby power to approximately 17 mW, thereby optimizing the power consumption for system needs.

The THS5641 is manufactured in Texas Instruments advanced high-speed mixed-signal CMOS process. A current-source-array architecture combined with simultaneous switching shows excellent dynamic performance. On-chip edge-triggered input latches and a 1.2 V temperature compensated bandgap reference provide a complete monolithic DAC solution. The digital supply range of 3 V to 5.5 V supports 3 V and 5 V CMOS logic families. Minimum data input setup and hold times allow for easy interfacing with external logic. The THS5641 supports both a straight binary and twos complement input word format, enabling flexible interfacing with digital signal processors.

description (continued)

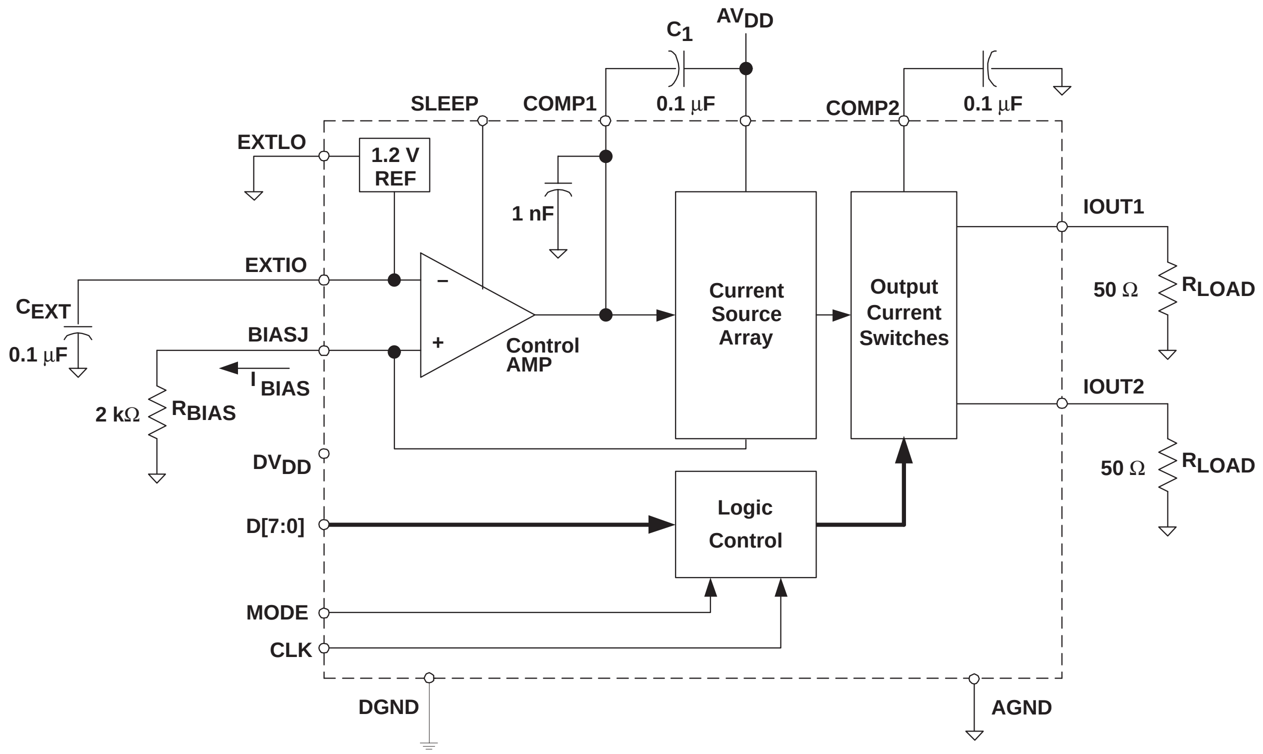
The THS5641 provides a nominal full-scale differential output current of 20 mA and >300 kΩ output impedance, supporting both single-ended and differential applications. The output current can be directly fed to the load (e.g., external resistor load or transformer), with no additional external output buffer required. An accurate on-chip reference and control amplifier allows the user to adjust this output current from 20 mA down to 2 mA, with no significant degradation of performance. This reduces power consumption and provides 20 dB gain range control capabilities. Alternatively, an external reference voltage and control amplifier may be applied in applications using a multiplying DAC.

The THS5641 is available in both a 28-pin SOIC and TSSOP package. The device is characterized for operation over the industrial temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	28-TSSOP (PW)	28-SOIC (DW)
–40°C to 85°C	THS5641IPW	THS5641IDW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20	I	Analog ground return for the internal analog circuitry
AV_{DD}	24	I	Positive analog supply voltage (3 V to 5.5 V)
BIASJ	18	O	Full-scale output current bias
CLK	28	I	External clock input. Input data latched on rising edge of the clock.
COMP1	19	I	Compensation and decoupling node, requires a 0.1 μF capacitor to AV_{DD}.
COMP2	23	I	Internal bias node, requires a 0.1 μF decoupling capacitor to AGND.
D[7:0]	[1:8]	I	Data bits 0 through 7. D7 is most significant data bit (MSB), D0 is least significant data bit (LSB).
DGND	26	I	Digital ground return for the internal digital logic circuitry
DV_{DD}	27	I	Positive digital supply voltage (3 V to 5.5 V)
EXTIO	17	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO = AV_{DD}). Used as internal reference output when EXTLO = AGND, requires a 0.1 μF decoupling capacitor to AGND when used as reference output
EXTLO	16	O	Internal reference ground. Connect to AV_{DD} to disable the internal reference source
IOUT1	22	O	DAC current output. Full scale when all input bits are set 1
IOUT2	21	O	Complementary DAC current output. Full scale when all input bits are 0
MODE	25	I	Mode select. Internal pulldown. Mode 0 is selected if this pin is left floating or connected to DGND. See timing diagram.
NC	[9:14]	N	No connection
SLEEP	15	I	Asynchronous hardware power down input. Active High. Internal pulldown. Requires 5 μs to power down but 3 ms to power up.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, AV_{DD} (see Note 1) . . . –0.3 V to 6.5 V
DV_{DD} (see Note 2) . . . –0.3 V to 6.5 V
Voltage between AGND and DGND . . . –0.3 V to 0.5 V
Supply voltage range, AV_{DD} to DV_{DD} . . . –6.5 V to 6.5 V
CLK, SLEEP, MODE (see Note 2) . . . –0.3 V to DV_{DD} + 0.3 V
Digital input D7–D0 (see Note 2) . . . –0.3 V to DV_{DD} + 0.3 V
IOUT1, IOUT2 (see Note 1) . . . –1 V to AV_{DD} + 0.3 V
COMP1, COMP2 (see Note 1) . . . –0.3 V to AV_{DD} + 0.3 V
EXTIO, BIASJ (see Note 1) . . . –0.3 V to AV_{DD} + 0.3 V
EXTLO (see Note 1) . . . –0.3 V to 0.3 V
Peak input current (any input) . . . 20 mA
Peak total input current (all inputs) . . . –30 mA
Operating free-air temperature range, T_A: THS5641I . . . –40°C to 85°C
Storage temperature range . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Measured with respect to AGND.
2. Measured with respect to DGND.

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			8			Bits
DC accuracy†						
INL	Integral nonlinearity	T_A = –40°C to 85°C	–0.25	±0.1	0.25	LSB
DNL	Differential nonlinearity		–0.25	±0.05	0.25	LSB
Monotonicity				Monotonic		
Analog output						
	Offset error			0.02		%FSR
	Gain error	Without internal reference		2.3		%FSR
		With internal reference		1.3		
	Full scale output current‡		2		20	mA
	Output compliance range	AV_{DD} = 5 V, $IOUT_{FS}$ = 20 mA	–1		1.25	V
		AV_{DD} = 3.3 V $IOUT_{FS}$ = 20 mA	–1		0.6	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
Reference output						
	Reference voltage		1.18	1.22	1.32	V
	Reference output current§			100		nA
Reference input						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth¶	Without C_{COMP1}		1.3		MHz
	Input capacitance			100		pF
Temperature coefficients						
	Offset drift			0		ppm of FSR/°C
	Gain drift	Without internal reference		±40		
		With internal reference		±120		
	Reference voltage drift			±35		
Power supply						
AV_{DD}	Analog supply voltage		3		5.5	V
DV_{DD}	Digital supply voltage		3		5.5	V
I_{AVDD}	Analog supply current			25	30	mA
	Sleep mode supply current	Sleep mode		3	5	mA
I_{DVDD}	Digital supply current#			5	6	mA
	Power dissipation‖	AV_{DD} = 5 V, DV_{DD} = 5 V $IOUT_{FS}$ = 20 mA		175		mW
		AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $IOUT_{FS}$ = 20 mA		100		
AV_{DD}	Power supply rejection ratio			±0.4		%FSR/V
DV_{DD}				±0.025		
	Operating range		–40		85	°C

† Measured at IOUT1 in virtual ground configuration.
‡ Nominal full-scale current $IOUT_{FS}$ equals 32X the IBIAS current.
§ Use an external buffer amplifier with high impedance input to drive any external load.
¶ Reference bandwidth is a function of external cap at COMP1 pin and signal level.
# Measured at f_{CLK} = 50 MSPS and f_{OUT}= 1 MHz.
‖ Measured for 50 Ω R_{LOAD} at IOUT1 and IOUT2, f_{CLK} = 50 MSPS and f_{OUT} = 20 MHz.
Specifications subject to change

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load (unless otherwise noted)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output						
f_{CLK}	Maximum output update rate	DV_{DD} = 4.5 V to 5.5 V	100			MSPS
		DV_{DD} = 3 V to 3.6 V	67			
$t_{s(DAC)}$	Output settling time to 0.1%†			35		ns
t_{pd}	Output propagation delay			1		ns
GE	Glitch energy‡	Worst case LSB transition (code 127 – code 128)		5		pV–s
$t_{r(IOUT)}$	Output rise time 10% to 90%†			1		ns
$t_{f(IOUT)}$	Output fall time 90% to 10%†			1		ns
	Output noise	$IOUT_{FS}$ = 20 mA		15		$pA/\sqrt{HZ}$
		$IOUT_{FS}$ = 2 mA		10		
AC linearity (to Nyquist)						
SINAD	Signal-to-noise and distortion ratio	f_{CLK} = 5 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		50		dB
		f_{CLK} = 25 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		50		
		f_{CLK} = 25 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		50		
		f_{CLK} = 25 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		48		
		f_{CLK} = 50 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		50		
		f_{CLK} = 50 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		50		
		f_{CLK} = 50 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		47		
		f_{CLK} = 70 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		50		
		f_{CLK} = 70 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		50		
		f_{CLK} = 70 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		46		
		f_{CLK} = 100 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		47		
		f_{CLK} = 100 MSPS, f_{OUT} = 22 MHz, T_A = 25°C		47		
		f_{CLK} = 100 MSPS, f_{OUT} = 40 MHz, T_A = 25°C		45		
THD	Total harmonic distortion	f_{CLK} = 5 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		–69		dBc
		f_{CLK} = 25 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		–67		
		f_{CLK} = 25 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		–69		
		f_{CLK} = 25 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		–57		
		f_{CLK} = 50 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		–67		
		f_{CLK} = 50 MSPS, f_{OUT} = 1 MHz, T_A = –40°C to 85°C			–64	
		f_{CLK} = 50 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		–66		
		f_{CLK} = 50 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		–52		
		f_{CLK} = 70 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		–64		
		f_{CLK} = 70 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		–60		
		f_{CLK} = 70 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		–48		
		f_{CLK} = 100 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		–53		
		f_{CLK} = 100 MSPS, f_{OUT} = 22 MHz, T_A = 25°C		–53		
		f_{CLK} = 100 MSPS, f_{OUT} = 40 MHz, T_A = 25°C		–47		

† Measured single ended into 50 Ω load at IOUT1.
‡ Single-ended output IOUT1, 50 Ω doubly terminated load.

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC linearity (to Nyquist)						
SFDR	Spurious free dynamic range	f_{CLK} = 5 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		68		dBc
		f_{CLK} = 25 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		69		
		f_{CLK} = 25 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		68		
		f_{CLK} = 25 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		56		
		f_{CLK} = 50 MSPS, f_{OUT} = 1 MHz, T_A = 25°C		67		
		f_{CLK} = 50 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		67		
		f_{CLK} = 50 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		53		
		f_{CLK} = 70 MSPS, f_{OUT} = 5 MHz, T_A = 25°C		65		
		f_{CLK} = 70 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		63		
		f_{CLK} = 70 MSPS, f_{OUT} = 20 MHz, T_A = 25°C		48		
		f_{CLK} = 100 MSPS, f_{OUT} = 10 MHz, T_A = 25°C		55		
		f_{CLK} = 100 MSPS, f_{OUT} = 22 MHz, T_A = 25°C		55		
		f_{CLK} = 100 MSPS, f_{OUT} = 40 MHz, T_A = 25°C		48		

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Interface						
V_{IH}	High-level input voltage	DV_{DD} = 5 V	3.5	5		V
		DV_{DD} = 3.3 V	2.1	3.3		
V_{IL}	Low-level input voltage	DV_{DD} = 5 V		0	1.3	V
		DV_{DD} = 3.3 V		0	0.9	
I_{IH}	High-level input current	DV_{DD} = 3 V to 5.5 V	–10		10	µA
I_{IL}	Low-level input current	DV_{DD} = 3 V to 5.5 V	–10		10	µA
	Input capacitance		1		5	pF
Timing						
$t_{su(D)}$	Input setup time		1			ns
$t_{h(D)}$	Input hold time		1			ns
$t_{w(LPH)}$	Input latch pulse high time		4			ns
$t_{d(D)}$	Digital delay time				1	clk

Specifications subject to change

TYPICAL CHARACTERISTICS†

SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY

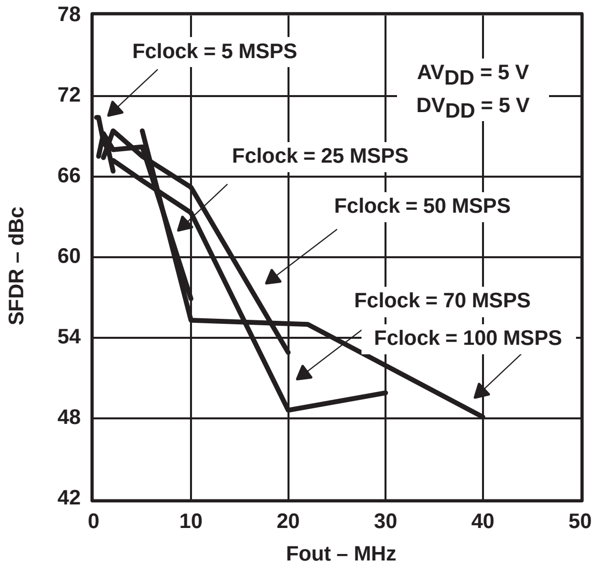


Figure 1

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

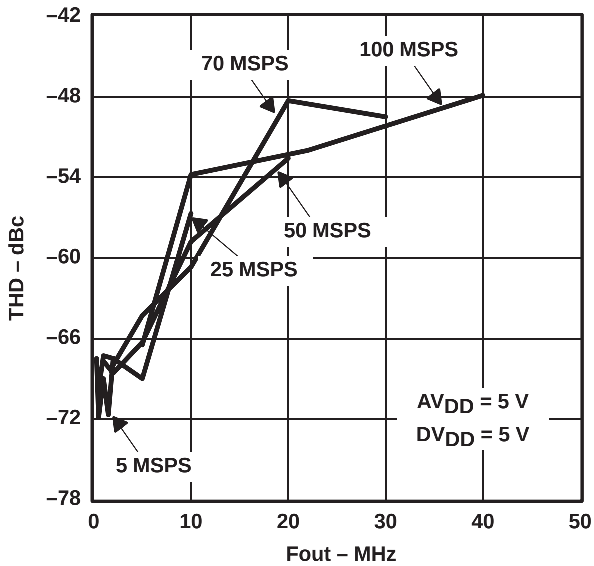


Figure 2

SIGNAL-TO-NOISE AND DISTORTION RATIO vs OUTPUT FREQUENCY

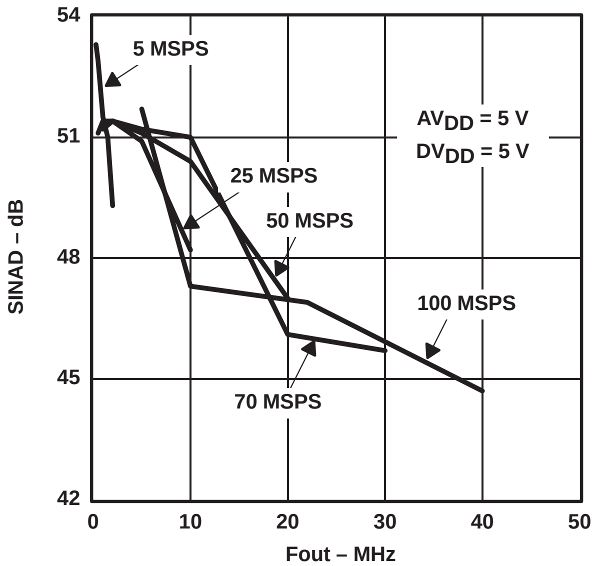


Figure 3

SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY

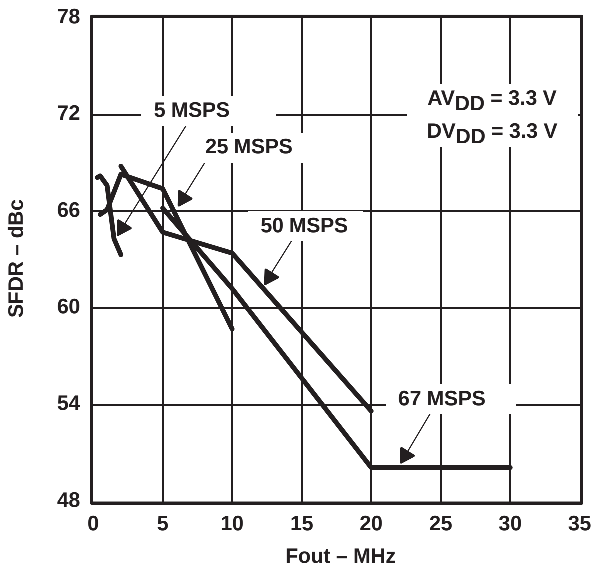


Figure 4

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
OUTPUT FREQUENCY

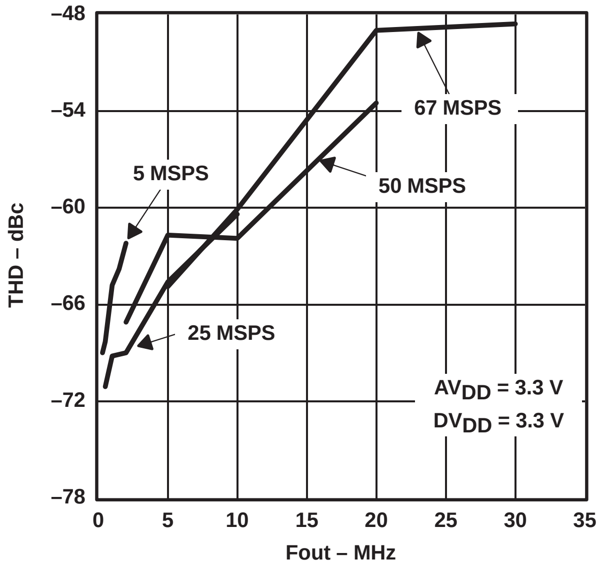


Figure 5

SIGNAL-TO-NOISE AND DISTORTION RATIO
vs
OUTPUT FREQUENCY

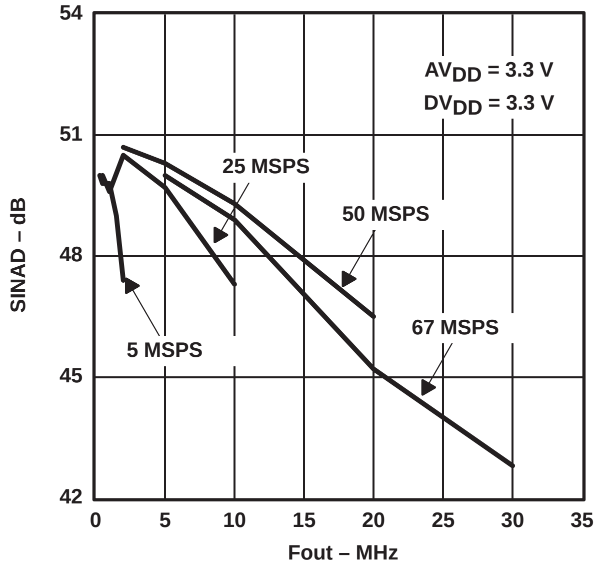


Figure 6

SIGNAL-TO-NOISE AND DISTORTION RATIO
vs
TEMPERATURE AT 70 MSPS

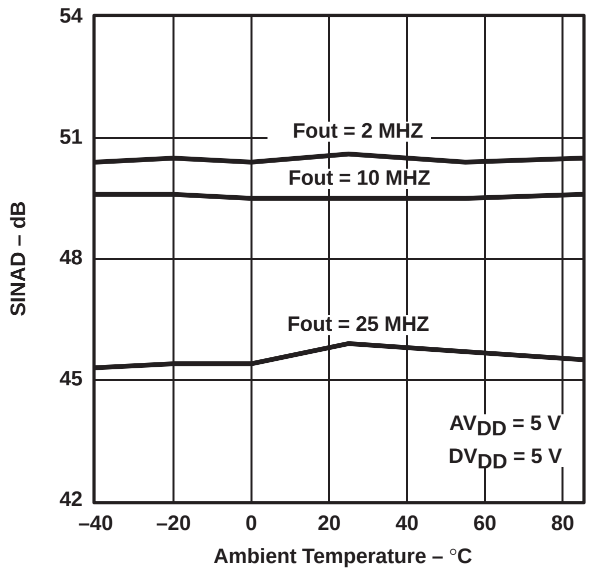


Figure 7

SIGNAL-TO-NOISE AND DISTORTION RATIO
vs
TEMPERATURE AT 70 MSPS

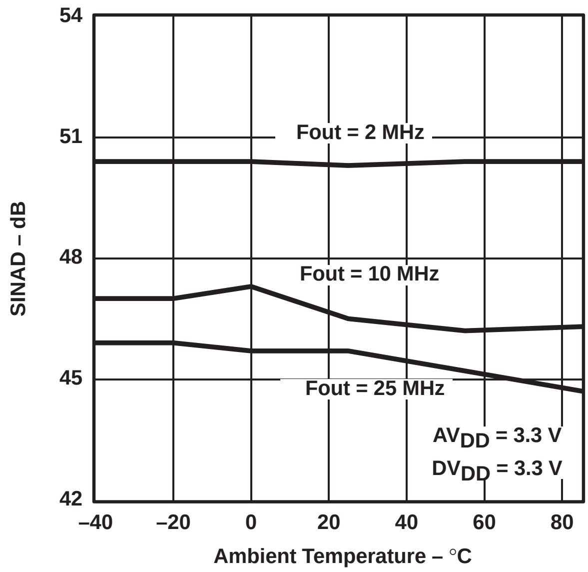


Figure 8

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

TYPICAL CHARACTERISTICS†

SPURIOUS FREE DYNAMIC RANGE vs FULL-SCALE OUTPUT CURRENT AT 100 MSPS

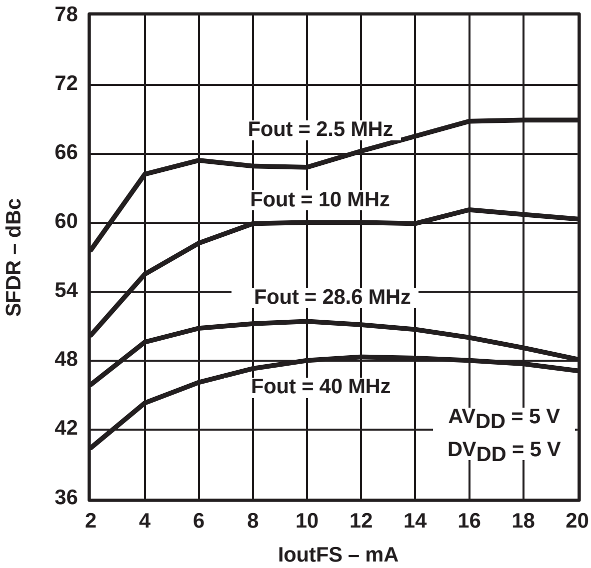


Figure 9

SIGNAL-TO-NOISE AND DISTORTION RATIO vs FULL-SCALE OUTPUT CURRENT AT 100 MSPS

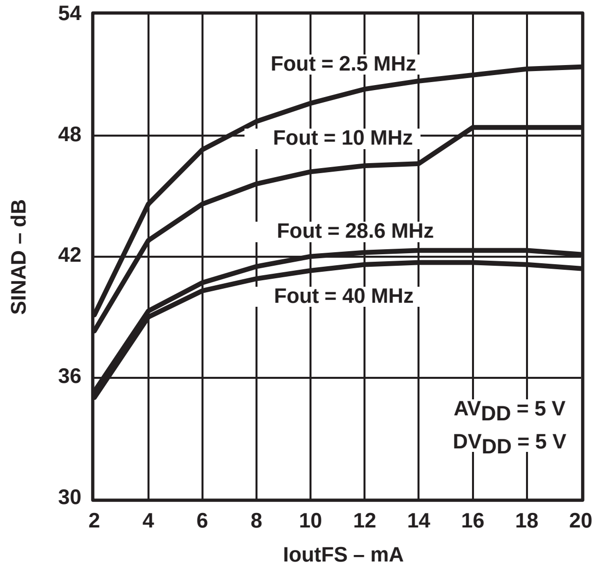


Figure 10

SPURIOUS FREE DYNAMIC RANGE vs OUTPUT FREQUENCY AT 50 MSPS

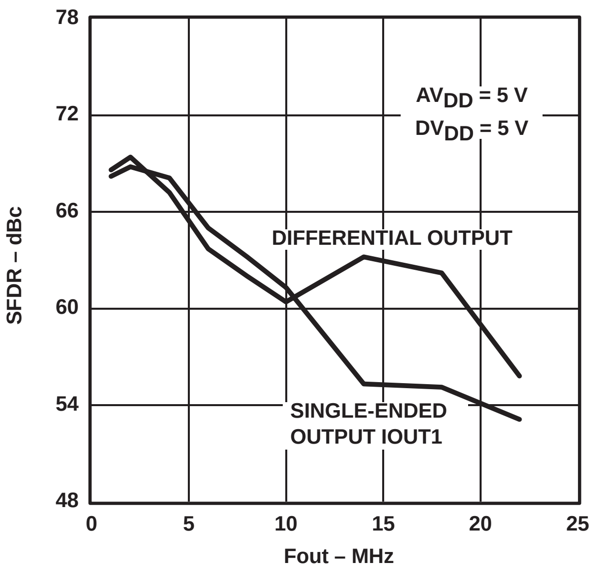


Figure 11

SIGNAL-TO-NOISE AND DISTORTION RATIO vs OUTPUT FREQUENCY AT 50 MSPS

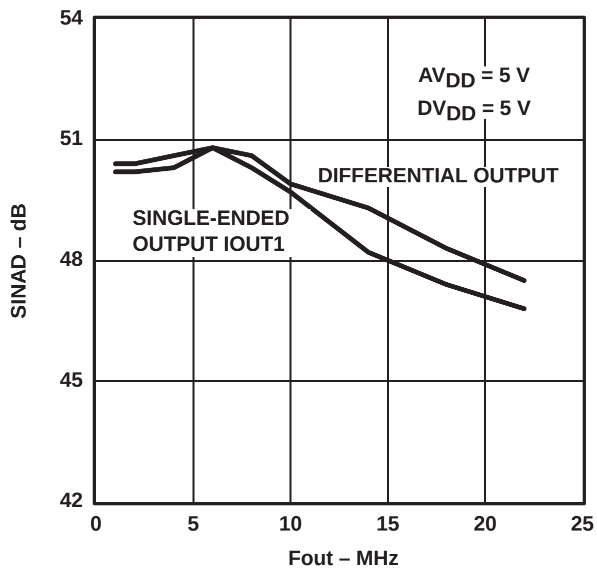


Figure 12

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

TYPICAL CHARACTERISTICS†

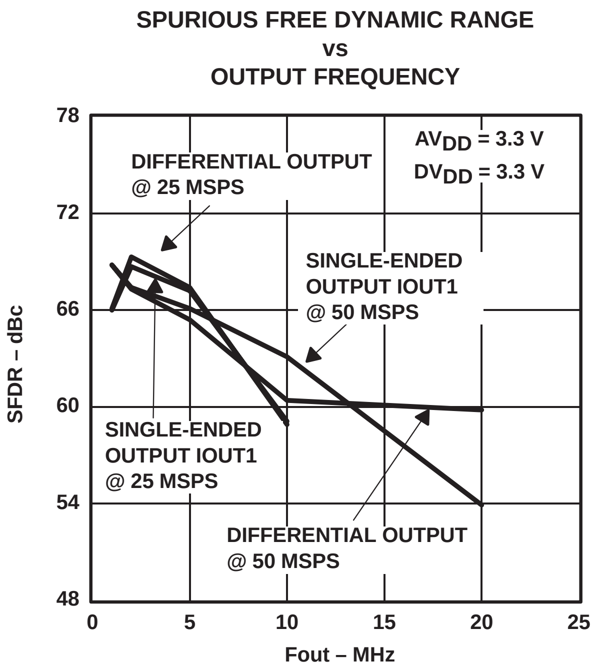


Figure 13

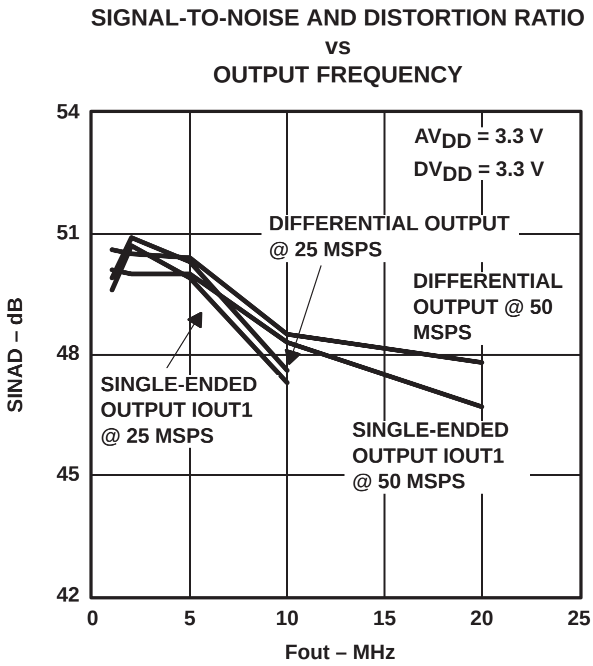


Figure 14

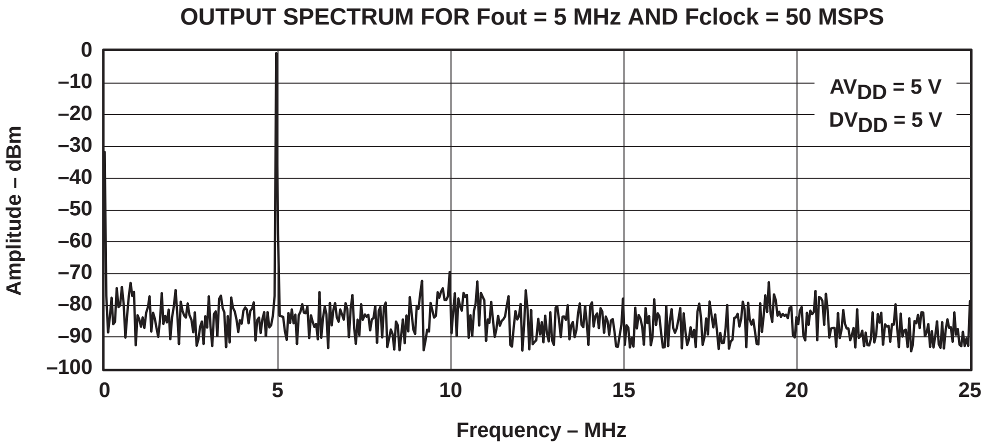


Figure 15

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

TYPICAL CHARACTERISTICS†

OUTPUT SPECTRUM FOR Fout = 10 MHz AND Fclock = 100 MSPS

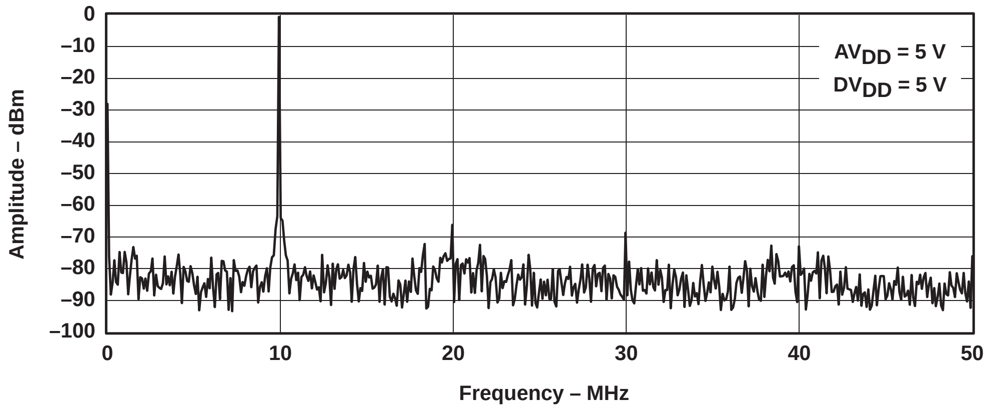


Figure 16

INTEGRAL NONLINEARITY

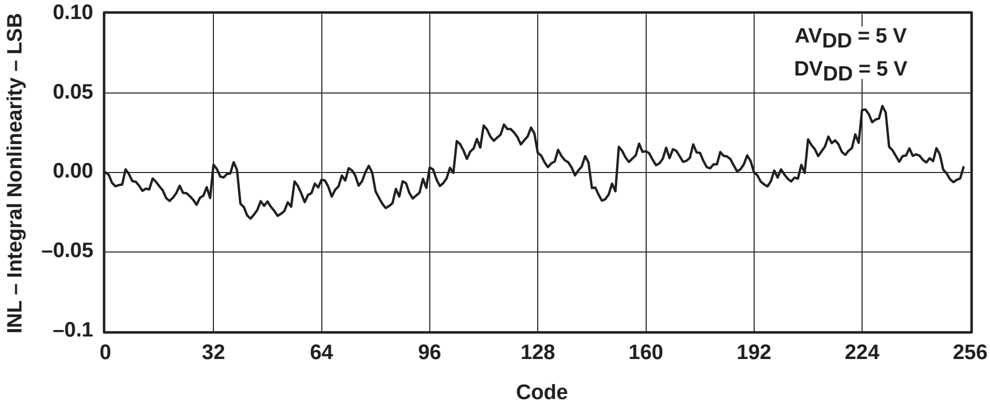


Figure 17

DIFFERENTIAL NONLINEARITY

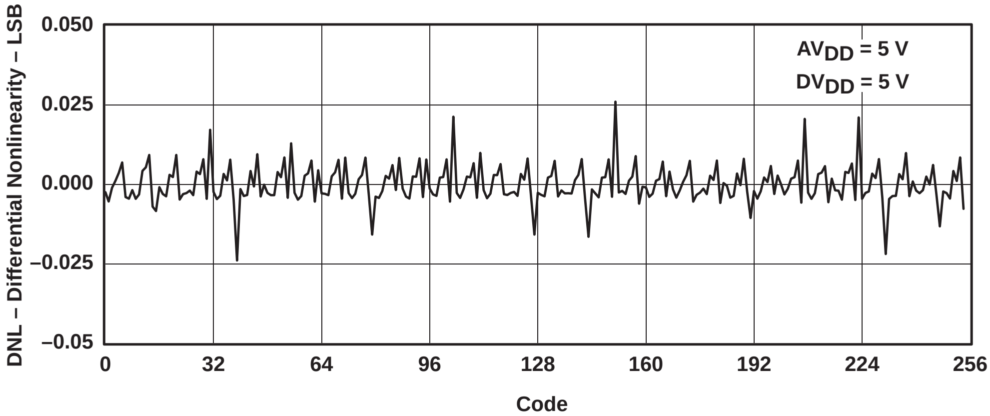


Figure 18

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

TYPICAL CHARACTERISTICS†

ANALOG SUPPLY CURRENT vs FULL-SCALE OUTPUT CURRENT

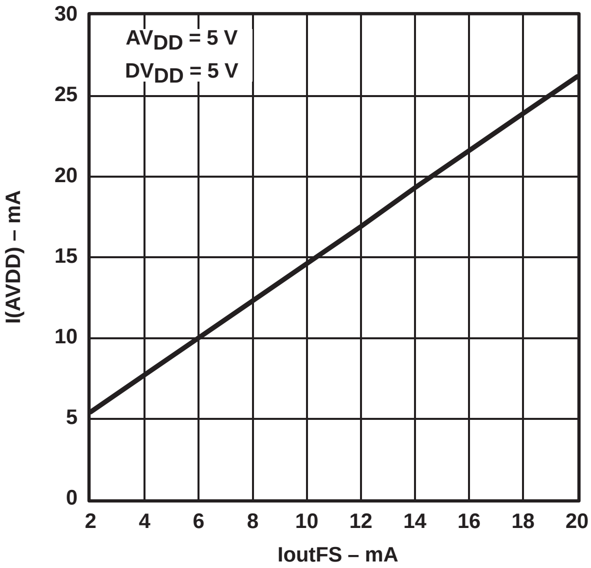


Figure 19

DIGITAL SUPPLY CURRENT vs RATIO (Fclock/Fout) AT DV_{DD} = 5 V

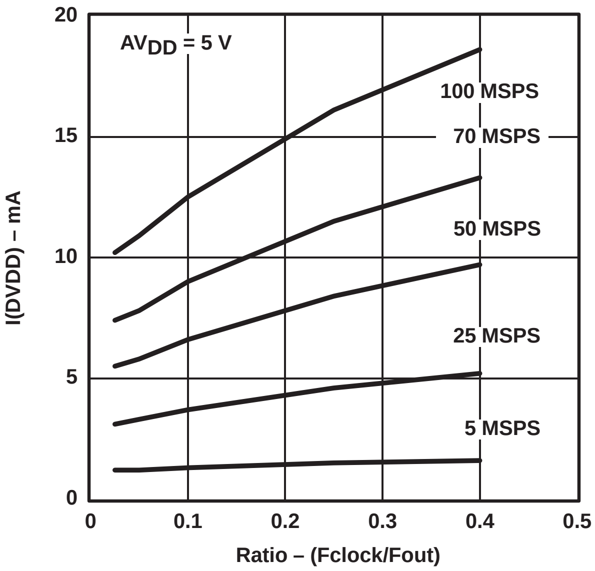


Figure 20

DIGITAL SUPPLY CURRENT vs RATIO (Fclock/Fout) AT DV_{DD} = 3.3 V

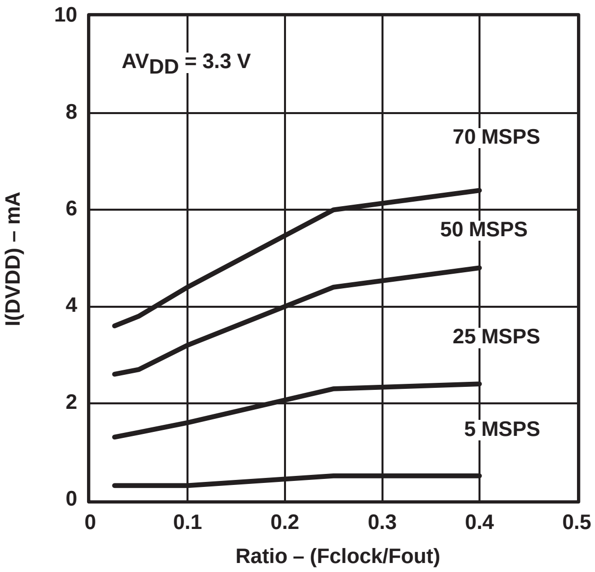


Figure 21

FULL-SCALE STEP REPONSE

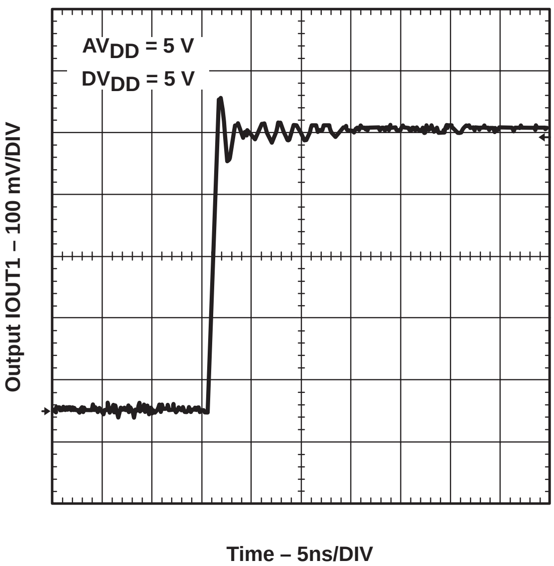


Figure 22

† AV_{DD} and DV_{DD} specified for each chart seperately, $IOUT_{FS}$ = 20 mA, single-ended output IOUT1, 50 Ω doubly terminated load, T_A = 25°C (unless otherwise noted.)

APPLICATION INFORMATION

The THS5641 architecture is based on current steering, combining high update rates with low power consumption. The CMOS device consists of a segmented array of PMOS transistor current sources, which are capable of delivering a full-scale current up to 20 mA. High-speed differential current switches direct the current of each current source to either one of the output nodes, IOUT1 or IOUT2. The complementary output currents thus enable differential operation, canceling out common mode noise sources (on-chip and PCB noise), dc offsets, even order distortion components, and increase signal output power by a factor of two. Major advantages of the segmented architecture are minimum glitch energy, excellent DNL, and very good dynamic performance. The DAC's high output impedance of >300 kΩ and fast switching result in excellent dynamic linearity (spurious free dynamic range SFDR).

The full-scale output current is set using an external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 32 times I_{BIAS}. The full-scale current can be adjusted from 20 mA down to 2 mA.

data interface and timing

The THS5641 comprises separate analog and digital supplies, i.e. AV_{DD} and DV_{DD}. The analog and digital supply voltage can be set independently from 5.5 V down to 3 V. The THS5641 provides two operating modes, as shown in Table 1. Mode 0 (mode pin connected to DGND) supports a straight binary input data word format, whereas mode 1 (mode pin connected to DV_{DD}) sets a twos complement input configuration.

Figure 23 shows the timing diagram. Internal edge-triggered flip-flops latch the input word on the rising edge of the input clock. The THS5641 provides for minimum setup and hold times (> 1 ns), allowing for noncritical external interface timing. Conversion latency is one clock cycle for both modes. The clock duty cycle can be chosen arbitrarily under the timing constraints listed in the digital specifications table. However, a 50% duty cycle will give optimum dynamic performance. Figure 24 shows a schematic of the equivalent digital inputs of the THS5641, valid for pins D7–D0, SLEEP, and CLK. The digital inputs are CMOS-compatible with logic thresholds of $DV_{DD}/2 \pm 20\%$. Since the THS5641 is capable of being updated up to 100 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the THS5641, as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feed-through and noise. Additionally, operating the THS5641 with reduced logic swings and a corresponding digital supply (DV_{DD}) will reduce data feed-through. Note that the update rate is limited to 67 MSPS for a digital supply voltage DV_{DD} of 3 V to 3.6 V.

APPLICATION INFORMATION

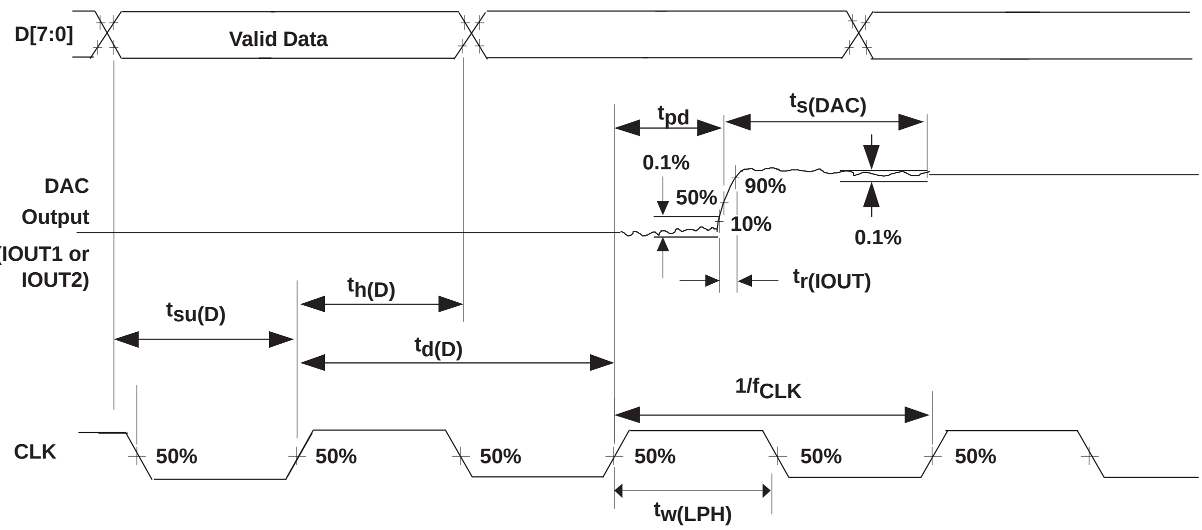


Figure 23. Timing Diagram

Table 1. Input Interface Modes

FUNCTION/MODE	MODE 0	MODE 1
	MODE PIN CONNECTED TO DGND	MODE PIN CONNECTED TO DV_{DD}
Input code format	Binary	Twos complement

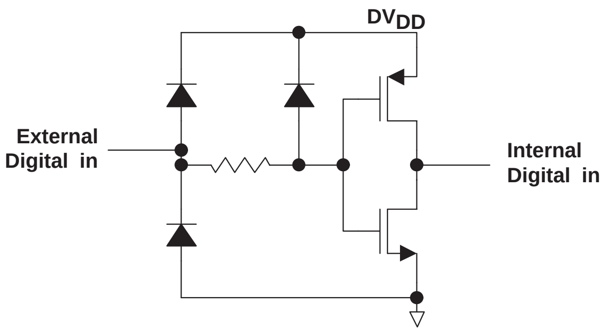


Figure 24. Digital Equivalent Input

APPLICATION INFORMATION

DAC transfer function

The THS5641 delivers complementary output currents IOUT1 and IOUT2. Output current IOUT1 equals the approximate full-scale output current when all input bits are set high in mode 0 (straight binary input), i.e. the binary input word has the decimal representation 255. For mode 1, the MSB is inverted (twos complement input format). Full-scale output current will flow through terminal IOUT2 when all input bits are set low (mode 0, straight binary input). The relation between IOUT1 and IOUT2 can thus be expressed as:

$$IOUT1 = IOUT_{FS} - IOUT2$$

where $IOUT_{FS}$ is the full-scale output current. The output currents can be expressed as:

$$IOUT1 = IOUT_{FS} \times \frac{CODE}{256}$$

$$IOUT2 = IOUT_{FS} \times \frac{(255 - CODE)}{256}$$

where CODE is the decimal representation of the DAC data input word. Output currents IOUT1 and IOUT2 drive resistor loads R_{LOAD} or a transformer with equivalent input load resistance R_{LOAD}. This would translate into single-ended voltages VOUT1 and VOUT2 at terminal IOUT1 and IOUT2, respectively, of:

$$VOUT1 = IOUT1 \times R_{LOAD} = \frac{CODE}{256} \times IOUT_{FS} \times R_{LOAD}$$

$$VOUT2 = IOUT2 \times R_{LOAD} = \frac{(255–CODE)}{256} \times IOUT_{FS} \times R_{LOAD}$$

The differential output voltage $VOUT_{DIFF}$ can thus be expressed as:

$$VOUT_{DIFF} = VOUT1–VOUT2 = \frac{(2CODE–255)}{256} \times IOUT_{FS} \times R_{LOAD}$$

The latter equation shows that applying the differential output will result in doubling of the signal power delivered to the load. Since the output currents of IOUT1 and IOUT2 are complementary, they become additive when processed differentially. Care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

APPLICATION INFORMATION

reference operation

The THS5641 comprises a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 32 times this bias current. The full-scale output current $IOUT_{FS}$ can thus be expressed as:

$$IOUT_{FS} = 32 \times I_{BIAS} = \frac{32 \times V_{EXTIO}}{R_{BIAS}}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AV_{DD}. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB. The bandwidth of the internal control amplifier is defined by the internal 1 nF compensation capacitor at pin COMP1 and the external compensation capacitor C1. The relatively weak internal control amplifier may be overridden by an externally applied amplifier with sufficient drive for the internal 1 nF load, as shown in Figure 25. This provides the user with more flexibility and higher bandwidths, which are specifically attractive for gain control and multiplying DAC applications. Pin SLEEP should be connected to AGND or left disconnected when an external control amplifier is used.

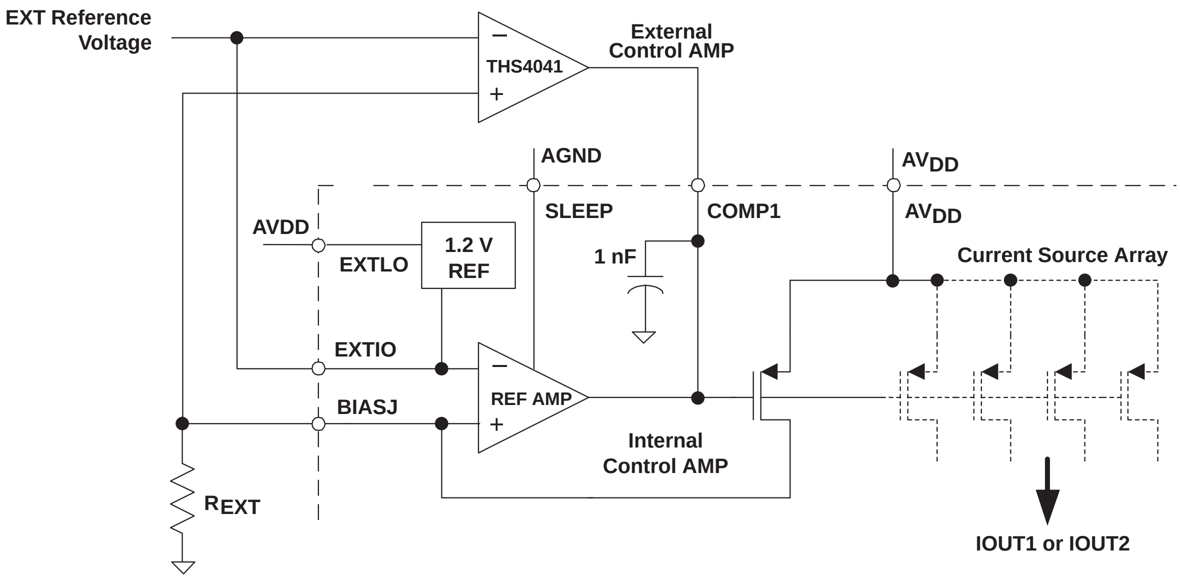


Figure 25. Bypassing the Internal Reference and Control Amplifier

APPLICATION INFORMATION

analog current outputs

Figure 26 shows a simplified schematic of the current source array output with corresponding switches. Differential PMOS switches direct the current of each individual PMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

Output nodes IOUT1 and IOUT2 have a negative compliance voltage of –1 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur, resulting in reduced reliability of the THS5641 device. The positive output compliance depends on the full-scale output current $IOUT_{FS}$ and positive supply voltage AV_{DD}. The positive output compliance equals 1.25 V for AV_{DD} = 5 V and $IOUT_{FS}$ = 20 mA. For AV_{DD} = 3.3 V the output compliance is limited to 0.6 V. Exceeding the positive compliance voltage adversely affects distortion performance and integral nonlinearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V (e.g. when applying a 50 Ω doubly terminated load for 20 mA full-scale output current). Applications requiring the THS5641 output (i.e., OUT1 and/or OUT2) to extend its output compliance should size R_{LOAD} accordingly.

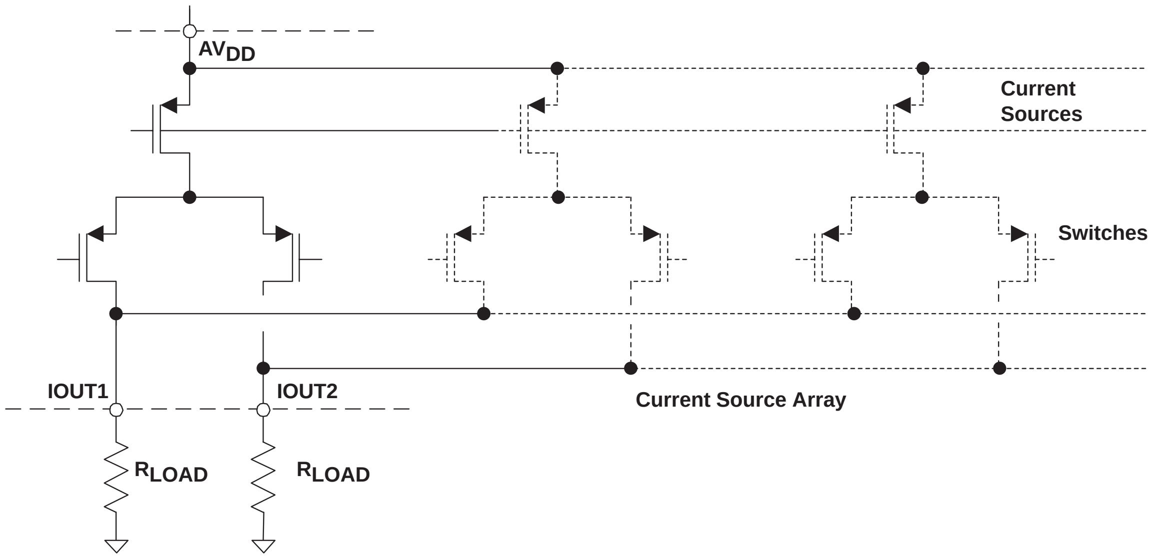


Figure 26. Equivalent Analog Current Output

Figure 27(a) shows the typical differential output configuration with two matched externally resistor loads. The nominal resistor load of 50 Ω will give a differential output swing of 2 V_{PP} when applying a 20 mA full-scale output current. The output impedance of the THS5641 depends slightly on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc integral nonlinearity, the configuration of Figure 27(b) should be chosen. In this I–V configuration, terminal IOUT1 is kept at virtual ground by the inverting operational amplifier. The complementary output should be connected to ground to provide a dc current path for the current sources switched to IOUT2. Note that the INL/DNL specifications for the THS5641 are measured with IOUT1 maintained at virtual ground. The amplifier's maximum output swing and the DAC's full-scale output current determine the value of the feedback resistor R_{FB}. Capacitor C_{FB} filters the steep edges of the THS5641 current output, thereby reducing the operational amplifier slew-rate requirements. In this configuration, the op amp should operate on a dual supply voltage due to its positive and negative output swing. Node IOUT1 should be selected if a single-ended unipolar output is desirable.

APPLICATION INFORMATION

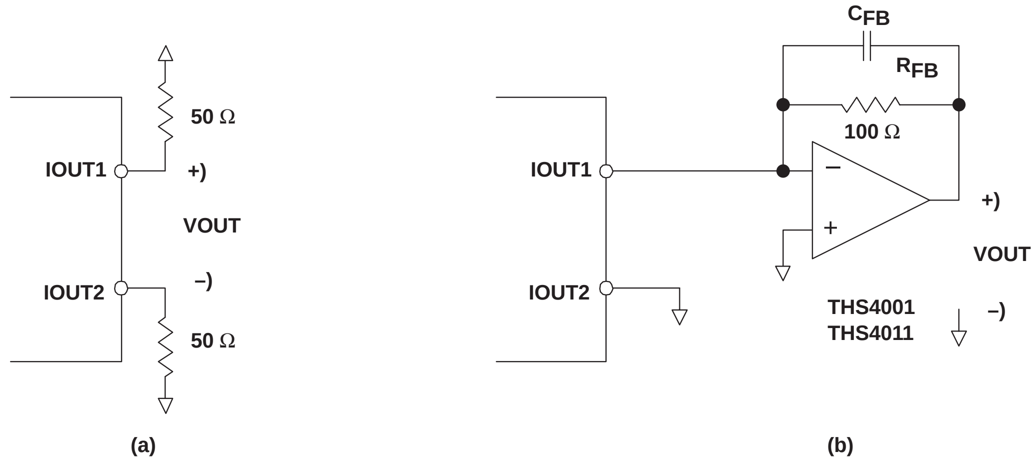


Figure 27. Differential and Single-Ended Output Configuration

The THS5641 can be easily configured to drive a doubly terminated 50 Ω cable. Figure 28(a) shows the single-ended output configuration, where the output current IOUT1 flows into an equivalent load resistance of 25 Ω. Node IOUT2 should be connected to ground or terminated with a resistor of 25 Ω. Differential-to-single conversion (e.g., for measurement purposes) can be performed using a properly selected RF transformer, as shown in Figure 28(b). This configuration provides maximum rejection of common-mode noise sources and even order distortion components, thereby doubling the power to the output. The center tap on the primary side of the transformer is connected to AGND, enabling a dc current flow for both IOUT1 and IOUT2. Note that the ac performance of the THS5641 is optimum using this differential transformer coupled output, limiting the voltage swing at IOUT1 and IOUT2 to ±0.5 V.

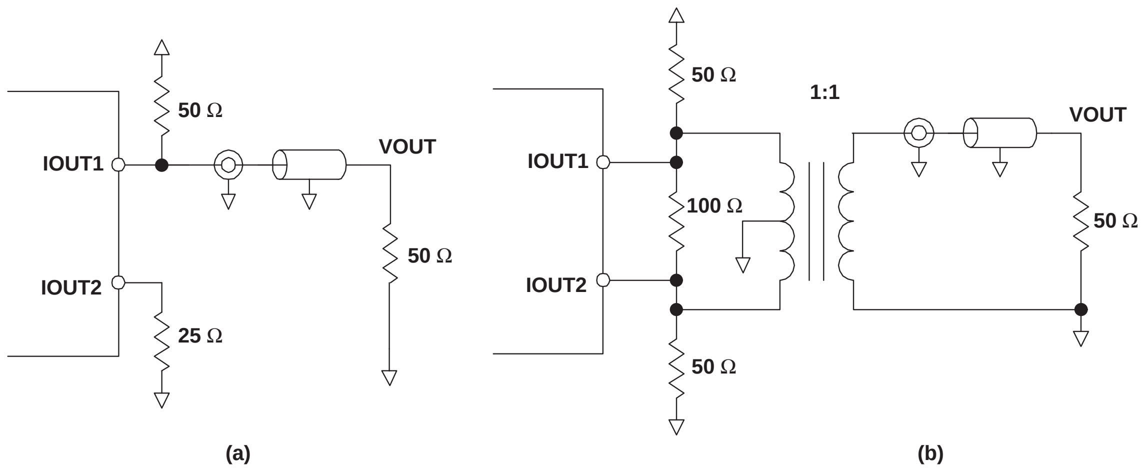


Figure 28. Driving a Doubly Terminated 50 Ω Cable

APPLICATION INFORMATION

sleep mode

The THS5641 features a power-down mode that turns off the output current and reduces the supply current to less than 5 mA over the analog supply range of 3 V to 5.5 V and temperature range. The power-down mode is activated by applying a logic level 1 to the SLEEP pin (e.g., by connecting pin SLEEP to AVDD). An internal pulldown circuit at node SLEEP ensures that the THS5641 is enabled if the input is left disconnected. Power-up and power-down activation times depend on the value of external capacitor at node SLEEP. For a nominal capacitor value of 0.1 μF power down takes less than 5 μs, and approximately 3 ms to power backup. The SLEEP mode should not be used when an external control amplifier is used, as shown in Figure 25.

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

offset error

Offset error is defined as the deviation of the output current from the ideal of zero at a digital input value of 0.

gain error

Gain error is the error in slope of the DAC transfer function.

signal-to-noise and distortion ratio (S/N+D or SINAD)

S/N+D or SINAD is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

output compliance range

The maximum and minimum allowable voltage of the output of the DAC, beyond which either saturation of the output stage or breakdown may occur.

settling time

The time required for the output to settle within a specified error band.

glitch energy

The time integral of the analog value of the glitch transient.

offset drift

The change in offset error versus temperature from the ambient temperature (T_A = 25°C) in ppm of full-scale range per °C.

gain drift

The change in gain error versus temperature from the ambient temperature (T_A = 25°C) in ppm of full-scale range per °C.

reference voltage drift

The change in reference voltage error versus temperature from the ambient temperature (T_A = 25°C) in ppm of full-scale range per °C.

THS5641 evaluation board

An evaluation module (EVM) board for the THS5641 digital-to-analog converter is available for evaluation. This board allows the user the flexibility to operate the THS5641 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and inverting/noninverting amplifier outputs. The digital inputs are designed to interface with the TMS320 C5000 or C6000 family of DSPs or to be driven directly from various pattern generators with the onboard option to add a resistor network for proper load termination.

See the *THS56x1 Evaluation Module User's Guide* for more details (SLAU032).

APPLICATION INFORMATION

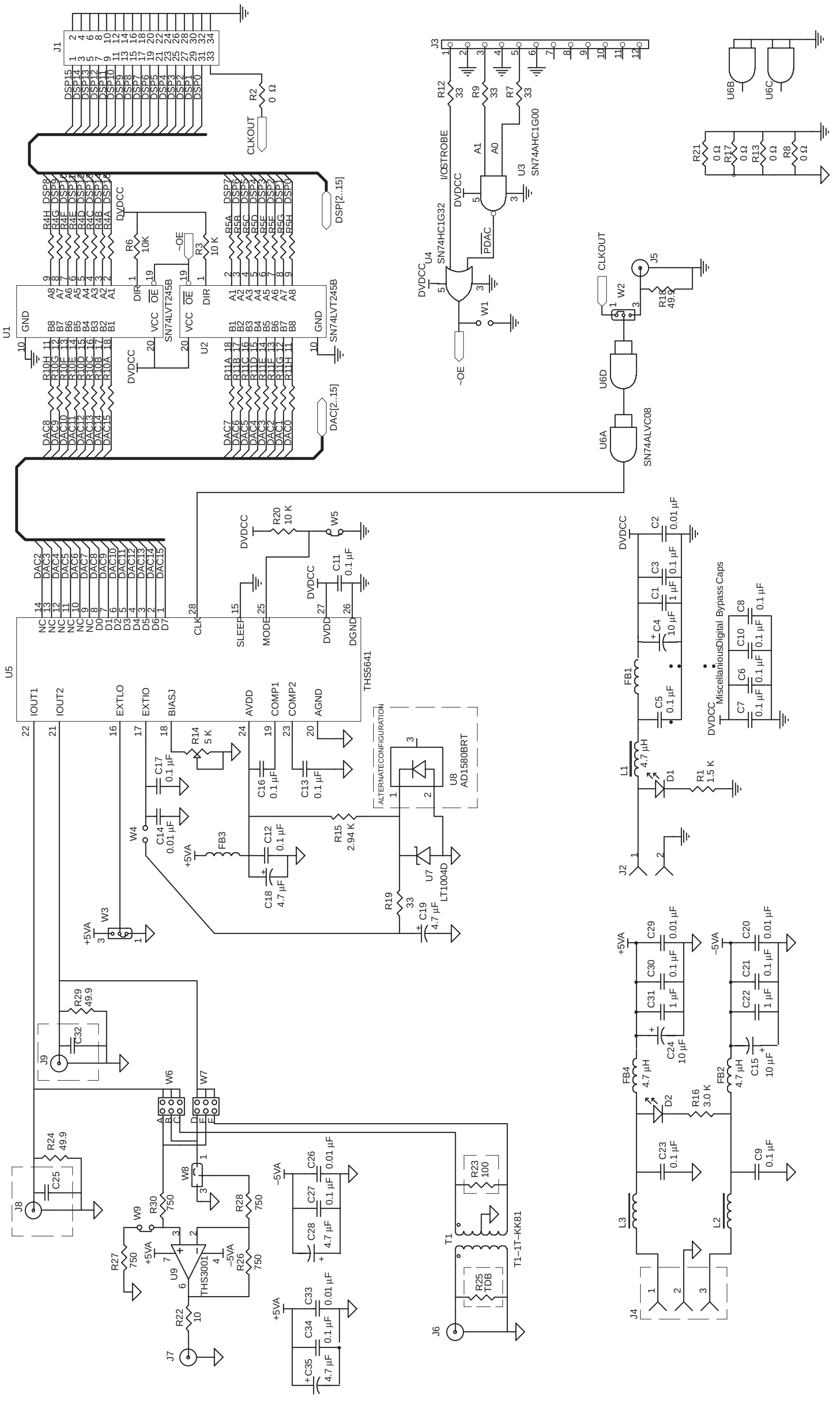


Figure 29. Schematic

APPLICATION INFORMATION

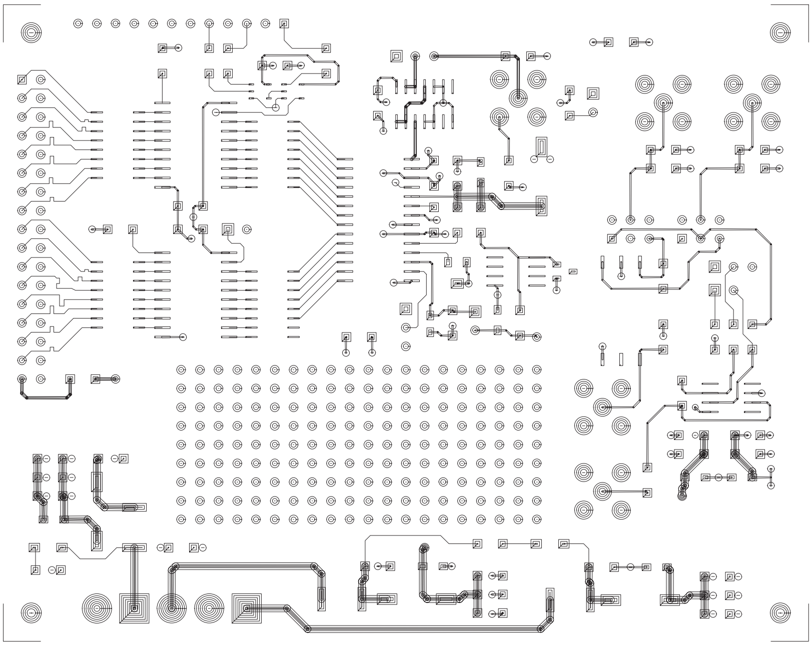


Figure 30. Board Layout, Layer 1

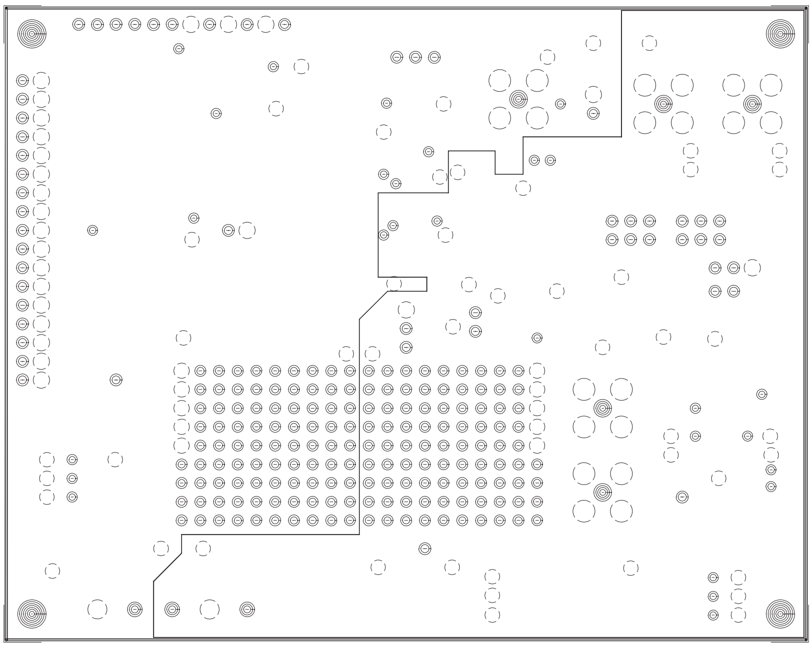


Figure 31. Board Layout, Layer 2

APPLICATION INFORMATION

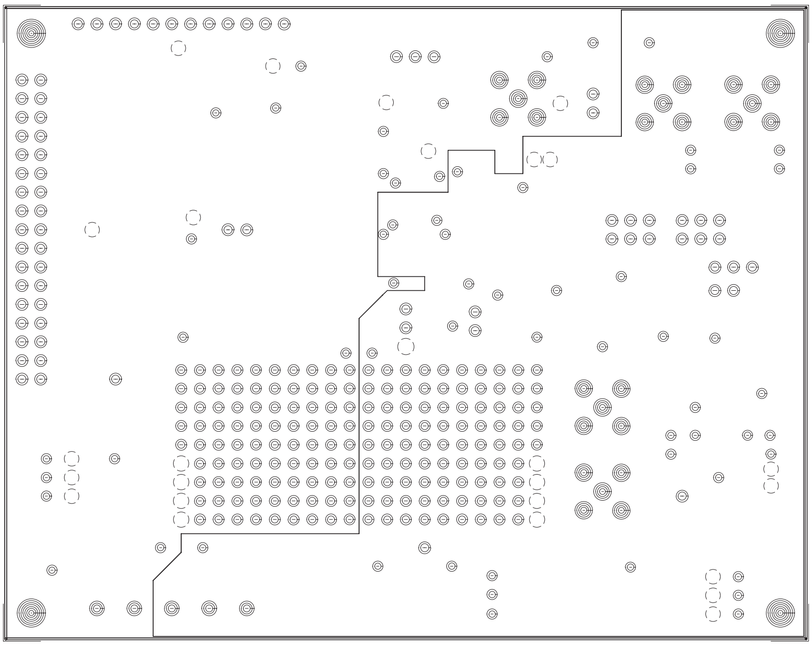


Figure 32. Board Layout, Layer 3

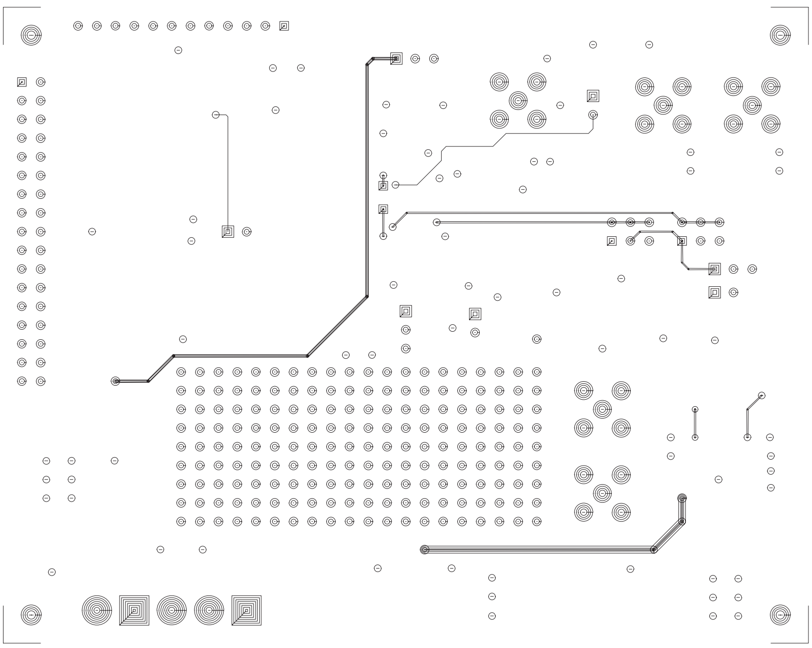


Figure 33. Board Layout, Layer 4

APPLICATION INFORMATION

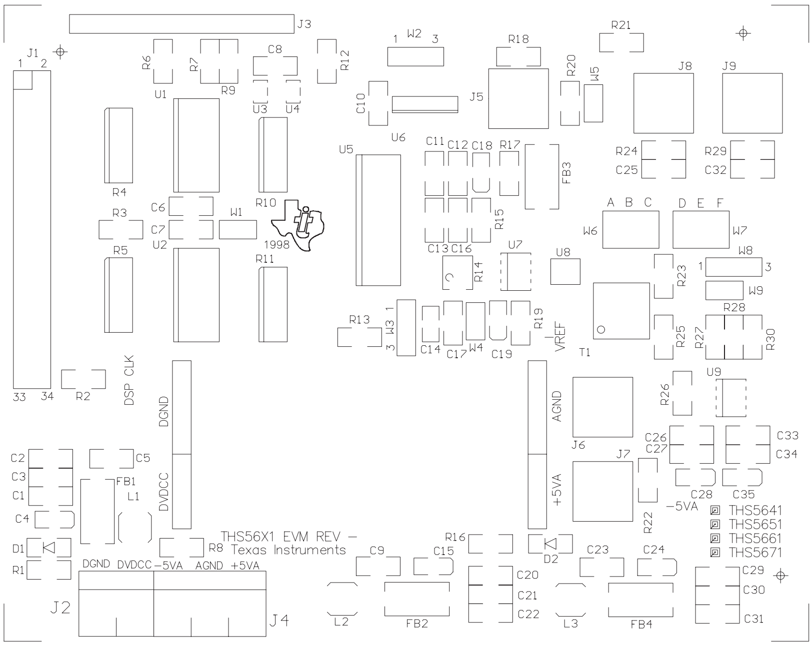


Figure 34. Board Layout, Layer 5

Table 2. Bill of Materials

QTY	REF. DES	PART NUMBER	DESCRIPTION	MFG.
3	C1, C22, C31	1206ZC105KAT2A	Ceranucm 1 μF, 10 V, X7R, 10%	AVX
4	C18, C19, C28, C35	ECSTOJY475	6.3 V, 4.7 μF, tantalum	Panasonic
3	C15, C24, C4	ECSTOJY106	6.3 V, 10 μF, tantalum	Panasonic
0	C25, C32		Ceramic, not installed, 50 V, X7R, 10%	
6	C14, C2, C20, C26, C29, C33	12065C103KAT2A	Ceramic, 0.01 μF, 50 V, X7R, 10%	AVX
17	C10, C11, C12, C13, C16, C17, C21, C23, C27, C3, C30, C34, C5, C6, C7, C8, C9	12065C104KAT2A	Ceramic, 0.1 μF, 50 V, X7R, 10%	AVX
2	D1, D2	AND/AND5GA or equivalent	GREEN LED, 1206 size SM chip LED	
4	FB1, FB2, FB3, FB4	27-43-037447	Fair-Rite SM beads #27-037447	FairRite
1	J1	TSW-117-07-L-D or equivalent	34-Pin header for IDC	Samtec
1	J2	KRMZ2 or equivalent	2 Terminal screw connector, 2TERM_CON	Lumberg
1	J3	TSW-112-07-L-S or equivalent	Single row 12-pin header	Samtec
1	J4	KRMZ3 or equivalent	3 Terminal screw connector	Lumberg
3	J5, J6, J7	142-0701-206 or equivalent	PCB Mount SMA jack, SMA_PCB_MT	Johnson Components
0	J8, J9	142-0701-206 or equivalent	PCB Mount SMA jack, not installed	Johnson Components
3	L1, L2, L3	DO1608C-472	DO1608C-series, DS1608C-472	Coil Craft
1	R1	1206	1206 Chip resistor, 1.5K, 1/4 W, 1%	
4	R10, R11, R4, R5	CTS/CTS766-163-(R)330-G-TR	8 Element isolated resistor pack, 33 Ω	

APPLICATION INFORMATION

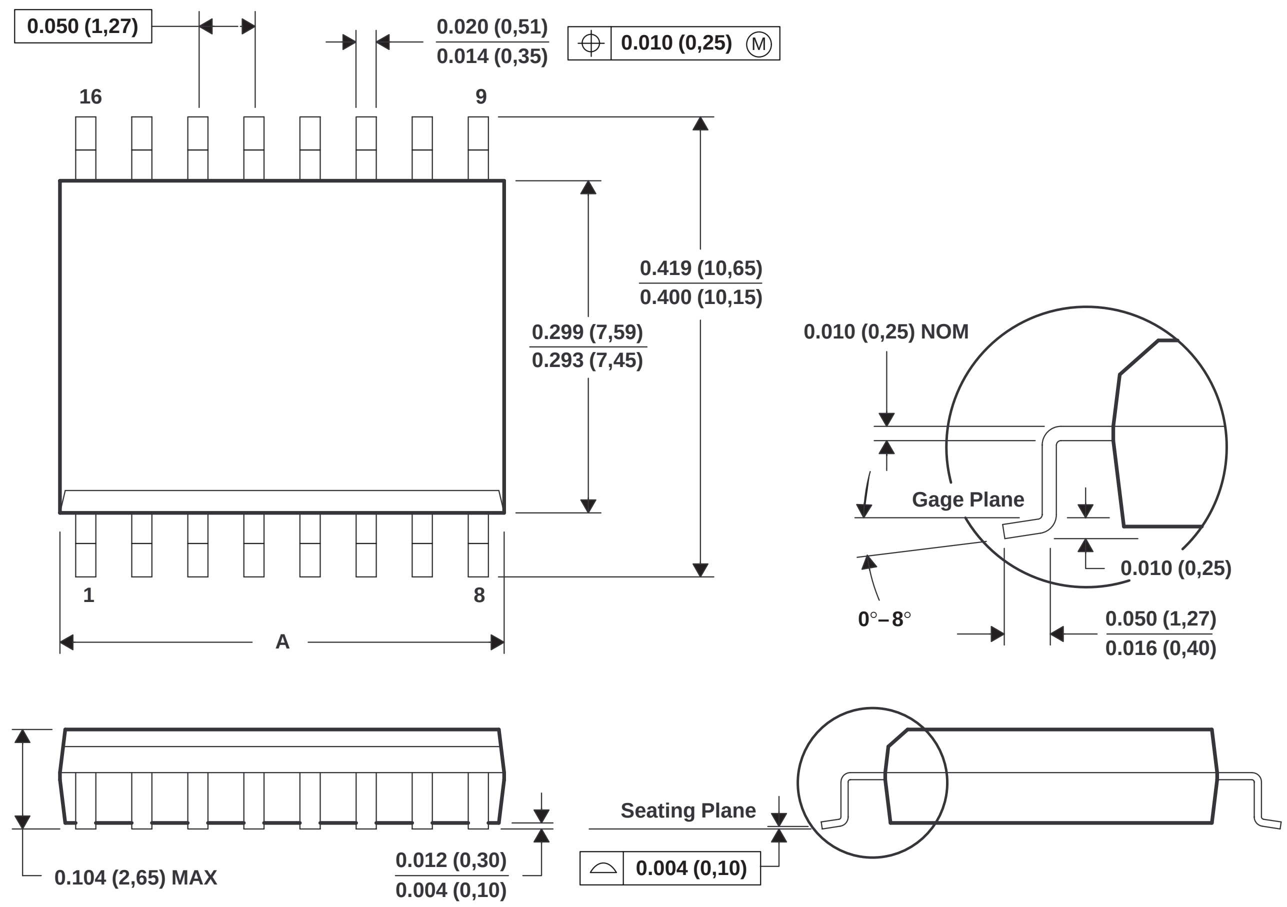
Table 2. Bill of Materials (Continued)

QTY	REF. DES	PART NUMBER	DESCRIPTION	MFG.
4	R12, R19, R7, R9	1206	1206 Chip resistor, 33 Ω, 1/4 W, 1%	
5	R13, R17. R2, R21, R8	1206	1206 Chip resistor, 0 Ω, 1/4 W, 1%	
1	R14	3214W-1-502 E or equivalent	4 mm SM Pot, 5K	Bourns
1	R15	1206	1206 Chip resistor, 2.94K, 1/4 W, 1%	
1	R16	1206	1206 Chip resistor, 3K, 1/4 W, 1%	
3	R18, R24, R29	1206	1206 Chip resistor, 49.94K, 1/4 W, 1%	
3	R20, R3, R6	1206	1206 Chip resistor, 10K, 1/4 W, 1%	
1	R22	1206	1206 Chip resistor, 10K, 1/4 W, 1%	
1	R23	1206	1206 Chip resistor, 100K, 1/4 W, 1%	
1	R25	1206	1206 Chip resistor, TBD, 1/4 W, 1%	
4	R26, R27, R28, R30	1206	1206 Chip resistor, 750K, 1/4 W, 1%	
1	T1	T1-1T-KK81	RF Transformer, T1-1T-KK81	MiniCircuits
2	U1, U2	SN74LVT245BDW	Octal bus transceiver, 3-state, SN74LVT245B	TI
1	U3	SN74AHCT1G00DBVR/ SN74AHC1G00DBVR	Single gate NAND, SN74AHC1G00	TI
1	U4	SN74AHCT1G32DBVR/ SN74AHCC1G32DBVR	Single 2 input positive or gate, SN74AHC1G32	TI
	THS5641	THS5641IDW	DAC, 2.7–5.5 V, 8 Bit, 125 MHz	TI
	THS5651	THS5651IDW	DAC, 2.7–5.5 V, 10 Bit, 125 MHz	TI
	THS5661	THS5661IDW	DAC, 2.7–5.5 V, 12 Bit, 125 MHz	TI
	THS5671	THS5647IDW	DAC, 2.7–5.5 V, 14 Bit, 125 MHz	TI
1	SN74ALVC08	SN74ALVC08D	Quad AND gate	TI
1	LT1004D	LT1004CD-1-2/LT1004ID-1-2	Precision 1.2 V reference	TI
0	NOT INSTALLED	AD1580BRT	Precision voltage reference, not installed	
1	THS3001	THS3001CD/THS2001ID	THS3001 high-speed op amp	TI
4	W2	TSW-102-07-L-S or equivalent	2 position jumper_.1’’ spacing, W2	Samtec
3	W3	TSW-102-07-L-S or equivalent	3 position jumper_.1’’ spacing, W3	Samtec
2	2X3_JUMPER	TSW-102-07-L-S or equivalent	6-Pin header dual row, 0.025×0.1, 2X3_JUMPER	Samtec

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

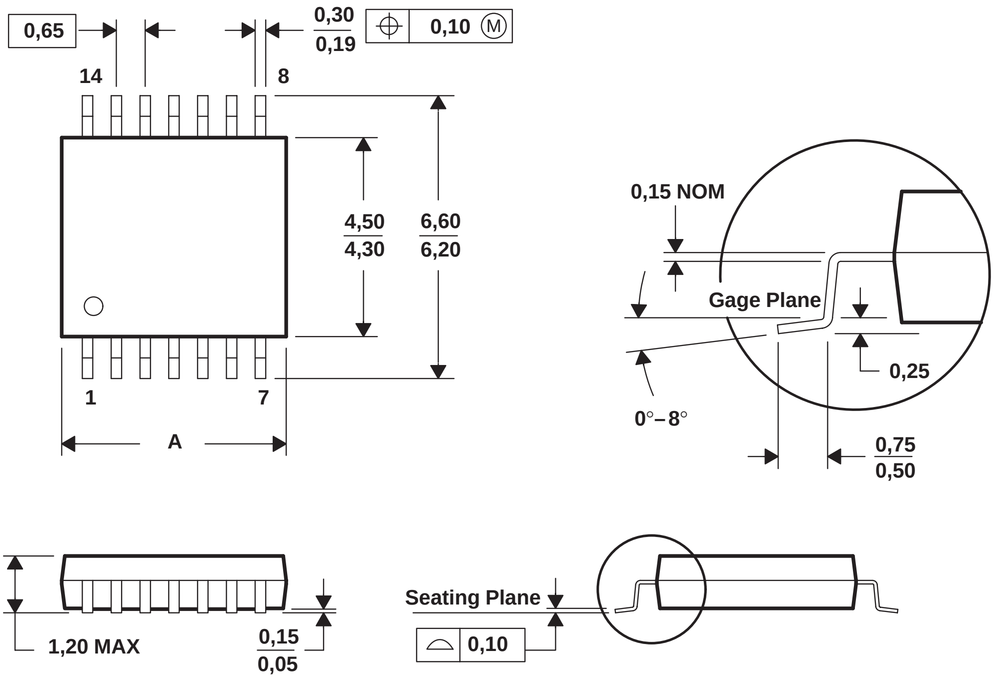
4040000/C 07/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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