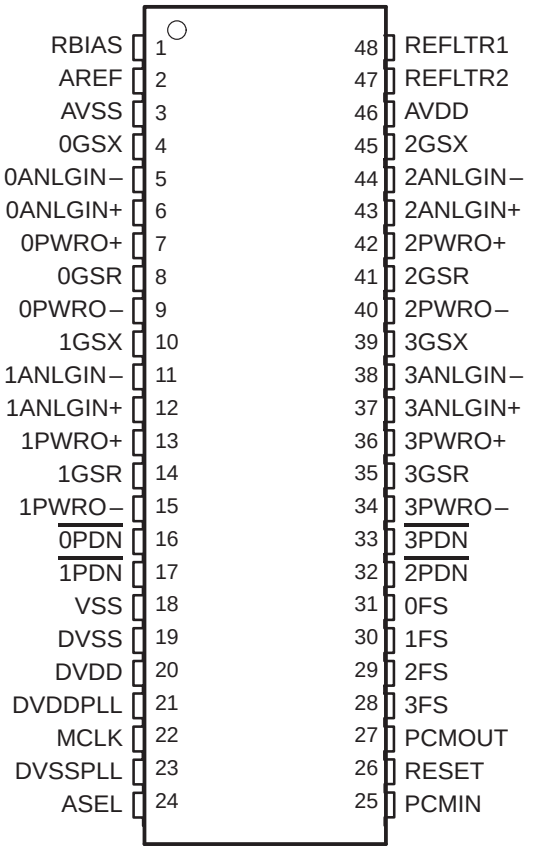
- **Single 5-V Supply**
- **Replaces Four TCM29C13-Type Combos (CODEC and Filters)**
- **Meets CCITT/(D3/D4) G.711 and G.714 Channel Bank Specifications**
- **Advanced Switched-Capacitor Filters and Sigma-Delta A/D and D/A Converter Technology With DSP Filtering**
- **μ-Law or A-Law Companding — Pin-Selectable**
- **2.048 MHz Operation**
- **8 Vpp Full-Signal Differential Receiver Output**
- **Differential Signal Processing Architecture**
- **Low Crosstalk (< –100 dB), Low Idle-Channel Noise, and Good Power Supply Rejection**
- **Single PCM I/O for Simplified PCM Interface**
- **Reliable Submicron Silicon-Gate CMOS Technology**

DL PACKAGE
(TOP VIEW)



description

The TCM38C17IDL QCombo™ is a 4-channel single-chip PCM combo (pulse-code-modulated CODEC with a voice-band filtering) device. It performs the transmit encoding (A/D conversion) and receive decoding (D/A conversion), as well as the transmit and receive filtering functions required to meet CCITT G.711 and G.714 specifications in a PCM system. Each channel provides all the functions required to interface a full-duplex, 4-line voice telephone circuit with a TDM (time-division-multiplexed) system. The TCM38C17IDL is specifically designed for fixed-data-rate applications and is intended to replace four TCM29C13-type devices.

Primary applications include digital transmission and switching of E1 carrier, PABX (private automatic branch exchange), and central office telephone systems and subscriber line concentrators. The device serves as the analog termination of a PCM line or trunk to the POTS (plain old telephone system) local-loop line.

Other applications include any PCM digital-audio interface such as voice-band data storage systems and many digital signal processing applications that can benefit from the reduced footprint of a quad codec configuration and single-rail operation. Dynamic range and excellent idle-channel noise performance are maintained using the TI advanced 4Vt process technologies.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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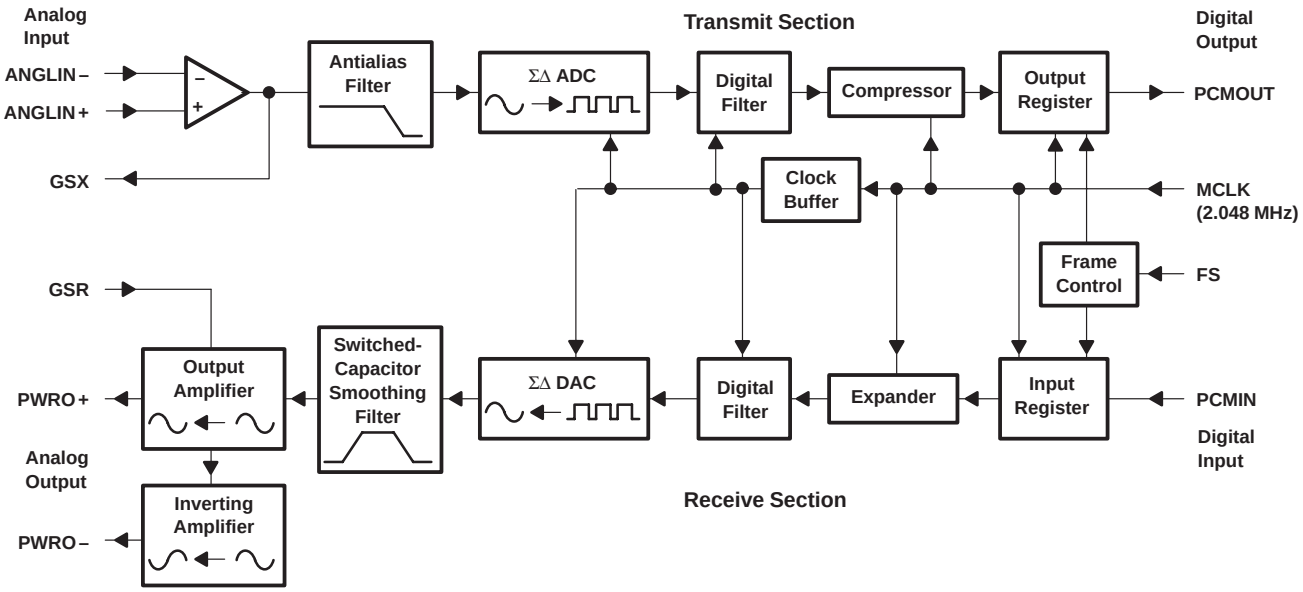
description (continued)

The TCM38C17IDL is available in a 48-pin plastic DL SSOP (shrink small-outline package) and is characterized for operation from –40°C to 85°C.

functional block diagram



NOTE A: One of four identical channels is depicted.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AREF	2		Analog reference point (mid-supply). This voltage is generated internally at a nominal 2.375 V. An external decoupling capacitor (0.1 μF) should be connected from AREF to AVSS for filtering purposes.
0ANLGIN+	6	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 0
0ANLGIN–	5	I	Inverting analog input to uncommitted transmit operational amplifier for channel 0
1ANLGIN+	12	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 1
1ANLGIN–	11	I	Inverting analog input to uncommitted transmit operational amplifier for channel 1
2ANLGIN+	43	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 2
2ANLGIN–	44	I	Inverting analog input to uncommitted transmit operational amplifier for channel 2
3ANLGIN+	37	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 3
3ANLGIN–	38	I	Inverting analog input to uncommitted transmit operational amplifier for channel 3
ASEL	24	I	A-law and μ-law operation select. When ASEL is connected to ground, A-law is selected. When ASEL is connected to VDD, μ-law is selected (digital).
AVDD	46		Analog supply voltage, 5 V, ±5%
AVSS	3		Analog ground return for AVDD supply
DVDD	20		Digital supply voltage, 5 V, ±5%
DVDDPLL	21		Phase-locked loop supply voltage, 5 V, ±5%
DVSSPLL	23		Phase-locked loop ground return for DVDDPLL supply
DVSS	19		Digital ground return for DVDD supply
0FS	31	I	Frame synchronization clock input/time slot enable for channel 0 TX and RX (digital)
1FS	30	I	Frame synchronization clock input/time slot enable for channel 1 TX and RX (digital)
2FS	29	I	Frame synchronization clock input/time slot enable for channel 2 TX and RX (digital)
3FS	28	I	Frame synchronization clock input/time slot enable for channel 3 TX and RX (digital)
0GSR	8	I	Receive amplifier gain-set input (channel 0). The ratio of an external voltage divider network connected to 0PWRO– and 0PWRO+ determines the receive amplifier gain. Maximum gain occurs when 0GSR is connected to 0PWRO–, and minimum gain occurs when it is connected to 0PWRO+ (analog).
1GSR	14	I	Receive amplifier gain-set input (channel 1). The ratio of an external voltage divider network connected to 1PWRO– and 1PWRO+ determines the receive amplifier gain. Maximum gain occurs when 1GSR is connected to 1PWRO–, and minimum gain occurs when it is connected to 1PWRO+ (analog).
2GSR	41	I	Receive amplifier gain-set input (channel 2). The ratio of an external voltage divider network connected to 2PWRO– and 2PWRO+ determines the receive amplifier gain. Maximum gain occurs when 2GSR is connected to 2PWRO–, and minimum gain occurs when it is connected to 2PWRO+ (analog).
3GSR	35	I	Receive amplifier gain-set input (channel 3). The ratio of an external voltage divider network connected to 3PWRO– and 3PWRO+ determines the receive amplifier gain. Maximum gain occurs when 3GSR is connected to 3PWRO–, and minimum gain occurs when it is connected to 3PWRO+ (analog).
0GSX	4	O	Output terminal of internal uncommitted transmit operational amplifier for channel 0 (analog)
1GSX	10	O	Output terminal of internal uncommitted transmit operational amplifier for channel 1 (analog)
2GSX	45	O	Output terminal of internal uncommitted transmit operational amplifier for channel 2 (analog)
3GSX	39	O	Output terminal of internal uncommitted transmit operational amplifier for channel 3 (analog)
MCLK	22	I	Master clock input (2.048 MHz) (digital)
PCMIN	25	I	Transmit PCM input (digital)
PCMOUT	27	O	Transmit PCM output (digital)
$\overline{0PDN}$	16	I	Power-down select for channel 0. This channel of the device is inactive with a CMOS low-level input to $\overline{0PDN}$ and active with a CMOS high-level input to the terminal (digital).
$\overline{1PDN}$	17	I	Power-down select for channel 1. This channel of the device is inactive with a CMOS low-level input to $\overline{1PDN}$ and active with a CMOS high-level input to the terminal (digital).
$\overline{2PDN}$	32	I	Power-down select for channel 2. This channel of the device is inactive with a CMOS low-level input to $\overline{2PDN}$ and active with a CMOS high-level input to the terminal (digital).

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{3PDN}$	33	I	Power-down select for channel 3. This channel of the device is inactive with a CMOS low-level input to $\overline{3PDN}$ and active with a CMOS high-level input to the terminal (digital).
0PWRO+	7	O	Noninverting output of channel 0 power amplifier. 0PWRO+can drive a 600 Ω || 100 pF load differentially (analog).
0PWRO–	9	O	Inverting output of channel 0 power amplifier. 0PWRO– can drive a 600 Ω || 100 pF load differentially (analog).
1PWRO+	13	O	Noninverting output of channel 1 power amplifier. 1PWRO+ can drive a 600 Ω || 100 pF load differentially (analog).
1PWRO–	15	O	Inverting output of channel 1 power amplifier. 1PWRO– can drive a 600 Ω || 100 pF load differentially (analog).
2PWRO+	42	O	Noninverting output of channel 2 power amplifier. 2PWRO+ can drive a 600 Ω || 100 pF load differentially (analog).
2PWRO–	40	O	Inverting output of channel 2 power amplifier. 2PWRO– can drive a 600 Ω || 100 pF load differentially (analog).
3PWRO+	36	O	Noninverting output of channel 3 power amplifier. 3PWRO+ can drive a 600 Ω || 100 pF load differentially (analog).
3PWRO–	34	O	Inverting output of channel 3 power amplifier, 3PWRO– can drive a 600 Ω || 100 pF load differentially (analog).
RBIAS	1		Bias current setting resistor. A 100 kΩ, ±5% resistor should be connected between terminals RBIAS and AVSS to set the bias current of the device.
REFLTR1	48		Voltage reference. A 1-µF external decoupling capacitor should be connected from REFLTR1 to AVSS for filtering purposes.
REFLTR2	47		Voltage reference. A 1-µF external decoupling capacitor should be connected from REFLTR2 to AVSS for filtering purposes.
RESET	26	I	Reset. Reset for all internal registers is initiated when RESET is brought high (digital).
VSS	18		Substrate bias. VSS should be externally connected to AVSS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . . –0.3 V to 7 V
Digital ground voltage range, V_O . . . . . –0.3 V to 7 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to AVSS.

recommended operating conditions (see Notes 2 and 3)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}	$0.8 \times V_{DD}$			V
Low-level input voltage, V_{IL}			$0.2 \times V_{DD}$	V
Load resistance between PWRO+ and PWRO– (differential), R_L	600			Ω
Load capacitance between PWRO+ and PWRO– (differential), C_L			100	pF
Operating free-air temperature, T_A	–40		85	°C

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltages at analog inputs, outputs and the AVDD terminal are with respect to the AREF terminal. All other voltages are referenced to the DVSS terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, total device, MCLK = 2.048 MHz, outputs not loaded, V_{DD} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	Operating	All channels		50†		mA
		Power down	$\overline{PDN}$ (all channels)		11		mA

† With 8 V_{pp} output

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	PCMOUT	I_{OH} = –3.2 mA	4.6	5		V
V_{OL}	Low-level output voltage	PCMOUT	I_{OL} = 3.2 mA		0	0.4	V
I_{IH}	High-level input current, any digital input		$V_I = 0.8 \times V_{DD}$			10	μA
I_{IL}	Low-level input current, any digital input		$V_I = 0.2 \times V_{DD}$			10	μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

transmit amplifier input

PARAMETER	MIN	TYP	MAX	UNIT
Input current at ANLGIN+ and ANLGIN–		±100		nA
Input offset voltage at ANLGIN+ and ANLGIN–		±5		mV
Common-mode rejection at ANLGIN+ and ANLGIN–	55			dB
Open-loop voltage amplification at ANLGIN+ and ANLGIN–	60			dB
Open-loop unity-gain bandwidth at ANLGIN+ and ANLGIN–		900		kHz
Input resistance at ANLGIN+ and ANLGIN–		10		MΩ

receive filter output

PARAMETER	TEST CONDITION	MIN	TYP‡	MAX	UNIT
Output offset voltage at PWRO+/PWRO –	Relative to AREF			±80	mV
Output resistance at PWRO+/PWRO –	DC output		1		Ω

‡ All typical values are at V_{DD} = 5 V, and T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

transmit and receive gain and dynamic range, V_{DD} = 5 V, T_A = 25°C (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 0 dBm0		±0.1	±0.18	dBm0
Encoder milliwatt response variation with temperature and power supplies		T_A = –40°C to 85°C, Supplies = ±5%			±0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission-level point		Signal input per CCITT G.711		±0.1	±0.18	dBm0
Digital milliwatt response variation with temperature and power supplies		T_A = –40°C to 85°C, Supplies = ±5%			±0.08	dB
Zero-transmission–level point (0 dBm0), transmit channel	μ-law	Input buffer configured for unity gain		0.747		Vrms
	A-law			0.75		
Transmit overload signal level, peak-to-peak centered at AREF					3	Vpp
Zero-transmission–level point (0 dBm0), receive channel	μ-law	R_L = 600 Ω at maximum gain (Load is connected between PWRO+ and PWRO–)		1.99		Vrms
	A-law			2		
Receive overload signal level, fully differential			7.8	8		Vpp

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test.
5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single ended in the maximum-gain (unity) configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

transmit and receive gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit gain tracking error, sinusoidal input	3 > input level ≥ –40 dBm0			±0.25	dB
	–40 > input level > –50 dBm0			±0.5	
	–50 ≥ input level ≥ –55 dBm0			±1.2	
Receive gain tracking error, sinusoidal input	3 > input level ≥ –40 dBm0			±0.25	dB
	–40 > input level > –50dBm0			±0.5	
	–50 ≥ input level ≥ –55 dBm0			±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted (μ-law), PCMOUT	ANLGIN+ = 0 V		10	12	dBrnC0
Transmit noise, psophometrically weighted (A-law), PCMOUT	ANLGIN+ = 0 V		–80	–75	dBm0p
Receive noise, C-message-weighted quiet code at PWRO+ (μ-law)	PCMIN = 11111111		5	12	dBrnC0
Receive noise, psophometrically weighted at PWRO+ (A-law)	PCMIN = 11010101		–85	–79	dBm0p

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT
V_{DD} supply voltage rejection, transmit channel	0 < f < 30 kHz	Idle channel, Supply signal = 200 mVpp, f measured at PCMOUT		–40		dB
	30 < f < 50 kHz			–45		
V_{DD} supply voltage rejection, receive channel (single-ended)	0 < f < 30 kHz	Idle channel, Supply signal = 200 mVpp, narrow-band, f measured at PWRO+		–40		dB
	30 < f< 50 kHz			–45		
Crosstalk (same channel) attenuation, transmit-to-receive (single-ended)		ANLGIN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCMIN = lowest decode level, measured at PWRO+		≤100‡	–75	dB
Crosstalk (same channel) attenuation, receive-to-transmit (single-ended)		PCMIN = 0 dBm0, f = 1.02 kHz, measured at PCMOUT		≤100‡	–75	dB
Crosstalk (between channels) attenuation	Transmit to transmit	0 dBm0, 300 Hz – 3400 Hz		≤100‡	–76	dB
	Transmit to receive			≤100‡	–78	
	Receive to transmit			≤100‡	–76	
	Receive to receive			≤100‡	–78	

† All typical values are at V_{DD} = 5 V, and T_A = 25°C
‡ Actual levels were beneath the test equipment measurement floor.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (CCITT G.712 - Method 2)	0 > ANLGIN > –30 dBm0	36		dB
	–30 > ANLGIN > –40 dBm0	30		
	–40 > ANLGIN > –45 dBm0	25		
Receive signal to distortion ratio, sinusoidal input (CCITT G.712 - Method 2)	0 > ANLGIN > –30 dBm0	36		dB
	–30 > ANLGIN > –40 dBm0	30		
	–40 > ANLGIN > –45 dBm0	25		
Transmit single-frequency distortion products	Input signal = 0 dBm0		–46	dBm0
Receive single-frequency distortion products	Input signal = 0 dBm0		–46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)		–35	dBm0
	CCITT G.712 (7.2)		–49	
	CCITT G.712 (6.1)		–25	
	CCITT G.712 (9)		–40	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITION		MIN	MAX	UNIT
Gain (voltage amplification) relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLGIN is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITION		MIN	MAX	UNIT
Gain (voltage amplification) relative to gain at 1.02 kHz	Input signal at PCMIN is 0 dBm0	Below 20 Hz		0.15	dB
		20 Hz		0.15	
		200 Hz	−0.5	0.15	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

		MIN	NOM†	MAX	UNIT
$t_{c(MCLK)}$	Clock period for MCLK 2.048 MHz systems		488.28		ns
t_r	Rise time for MCLK			30	ns
t_f	Fall time for MCLK			30	ns
$t_{w(MCLK)}$	Pulse duration for MCLK (see Note 8)	220			ns
	Clock duty cycle [$t_{w(MCLK)}/t_{c(MCLK)}$] for MCLK	45%	50%	55%	

† All nominal values are at V_{DD} = 5 V, and T_A = 25°C.

NOTE 7: FS clock must be phase-locked with MCLK.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figures 3 and 4)

		MIN	MAX	UNIT
$t_{su(FS)}$	Setup time, frame sync, from FS↑ to MCLK↓	100	t_c (MCLK) –100	ns
$t_{su(PCMIN)}$	Setup time, receive data, from data valid to MCLK↓	10		ns
$t_{h(PCMIN)}$	Hold time, receive data, from MCLK↓ to data invalid	60		ns
$t_{h(RESET)}$	Hold time, RESET terminal ↑ to reset activation	100		ns
$t_{h(FS)}$	Hold time, frame sync, from MCLK↑ to FS↓	10	t_c(MCLK)×7	ns
$t_{d(FS-FS)}$	Delay time, between MCLK↓ while any channel FS high and MCLK↓ while next channel FS high (see Figure 6)		t_c(MCLK)×64	µs

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see Figure 3)

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{pd1}	Transmit clock↑ to bit 1 data valid at PCMOUT (data enable time on time slot entry) (see Note 8)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	Transmit clock↑ bit n to bit n data valid at PCMOUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	Transmit clock↓ bit 8 to bit 8 hi-Z at PCMOUT (data float time on time slot exit) (see Note 9)	C_L = 0 pF	60	215	ns

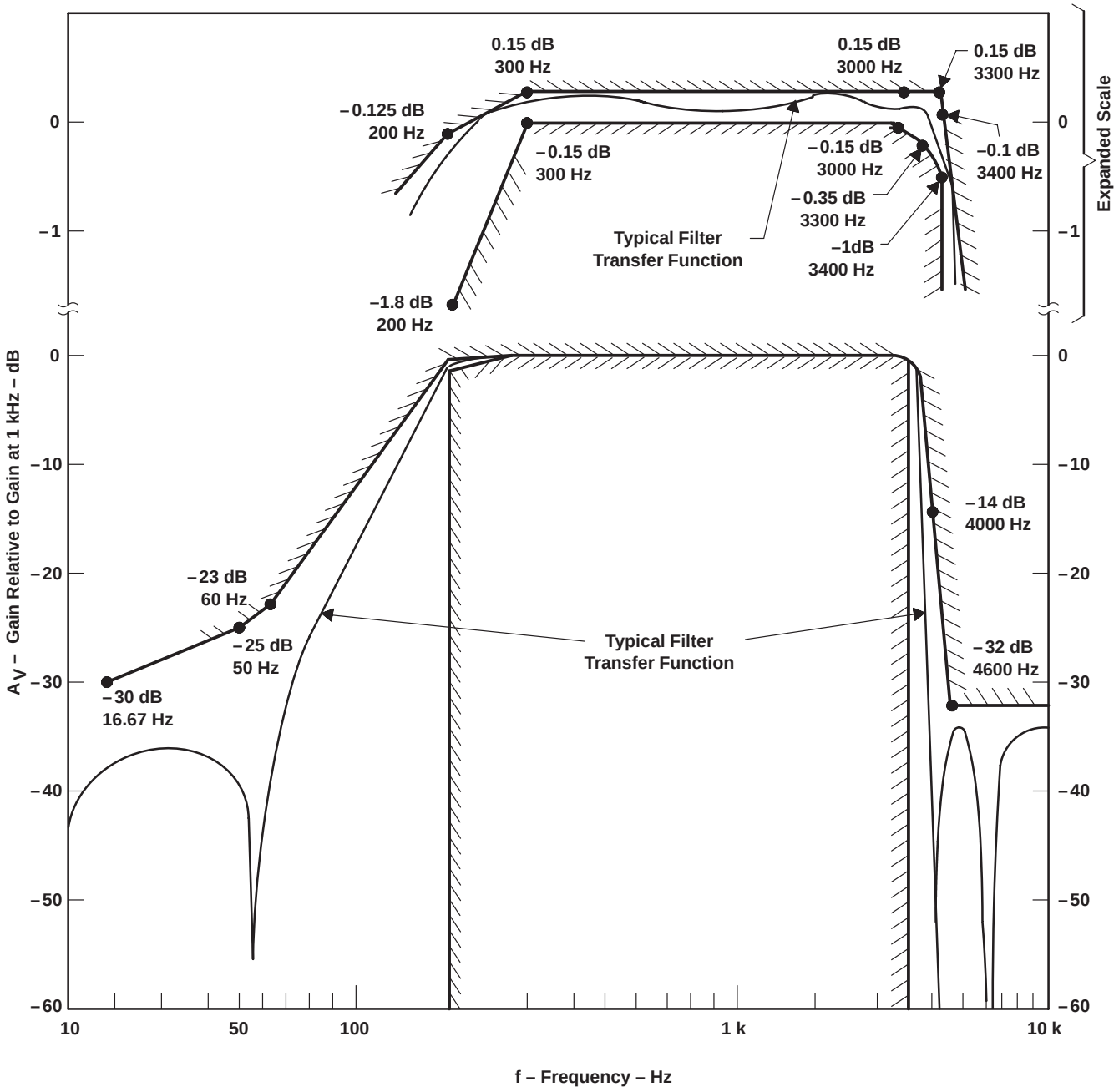
NOTE 8: Timing parameters t_{pd1} and t_{pd3} are referenced to the high-impedance state.

absolute and relative delay times over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Transmit absolute delay time to PCMOUT	Fixed data rate, MCLK = 2.048 MHz, Input to ANLGIN 1.02 kHz at 0 dBm0		500		µs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz – 600 Hz		170		µs
	f = 600 Hz – 1000 Hz		95		
	f = 1000 Hz – 2600 Hz		45		
	f = 2600 Hz – 2800 Hz		105		
Receive absolute delay time to PWRO	Fixed data rate, MCLK = 2.048 MHz, Digital input is digital milliwatt codes		190		µs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz – 600 Hz		45		µs
	f = 600 Hz – 1000 Hz		35		
	f = 1000 Hz – 2600 Hz		85		
	f = 2600 Hz – 2800 Hz		110		

† All typical values are at V_{DD} = 5 V, and T_A = 25°C.

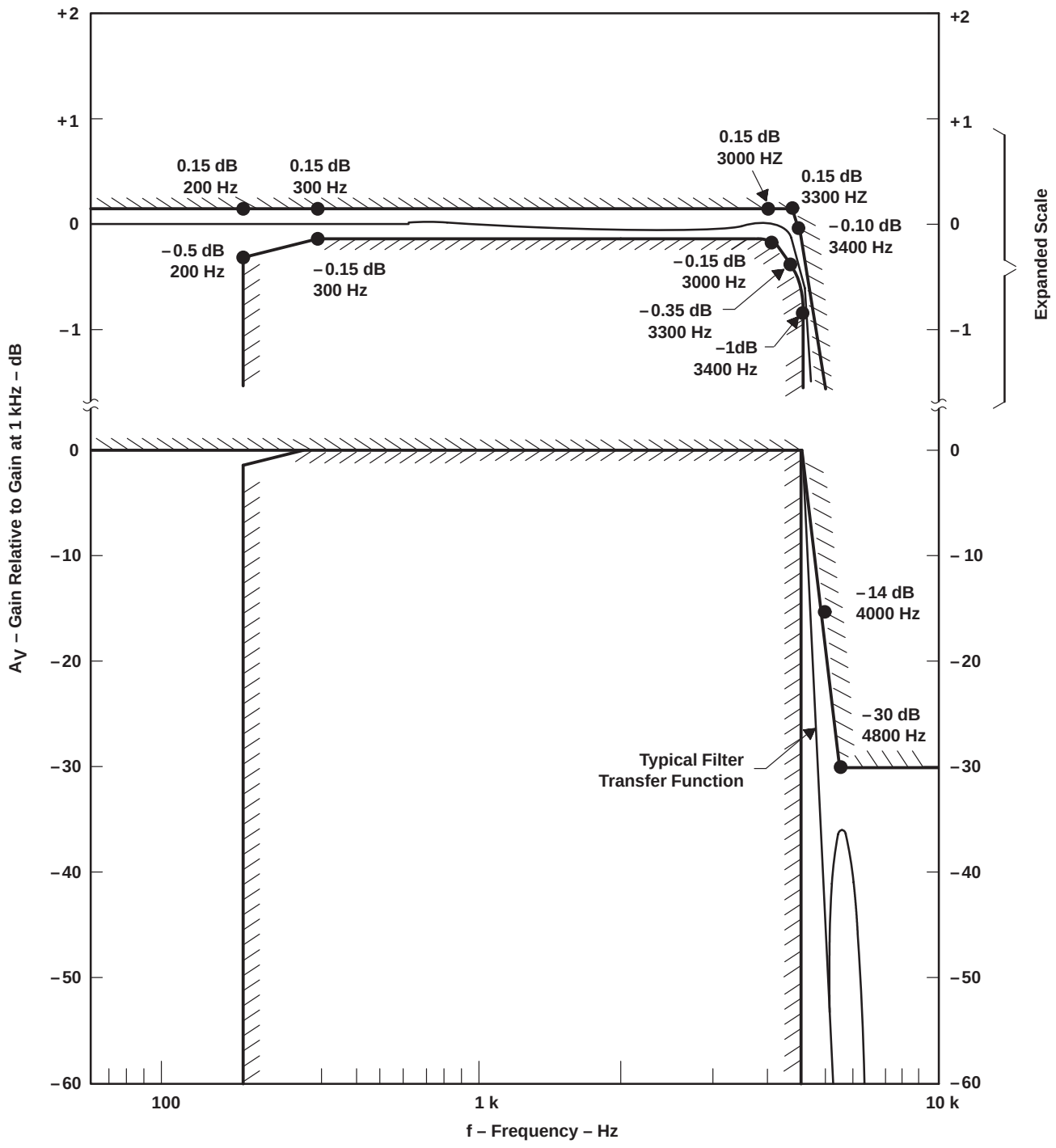
PARAMETER MEASUREMENT INFORMATION



NOTE A: Gain (voltage amplification) is defined as gain relative to gain at 1 kHz –dB.

Figure 1. Transmit-Filter Transfer Characteristics

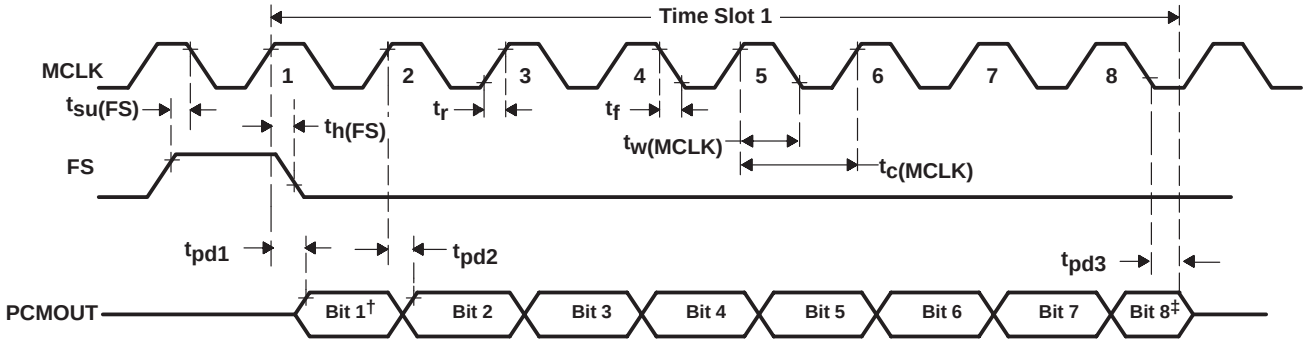
PARAMETER MEASUREMENT INFORMATION



NOTE A: Gain (voltage amplification) is defined as gain relative to gain at 1 kHz –dB.

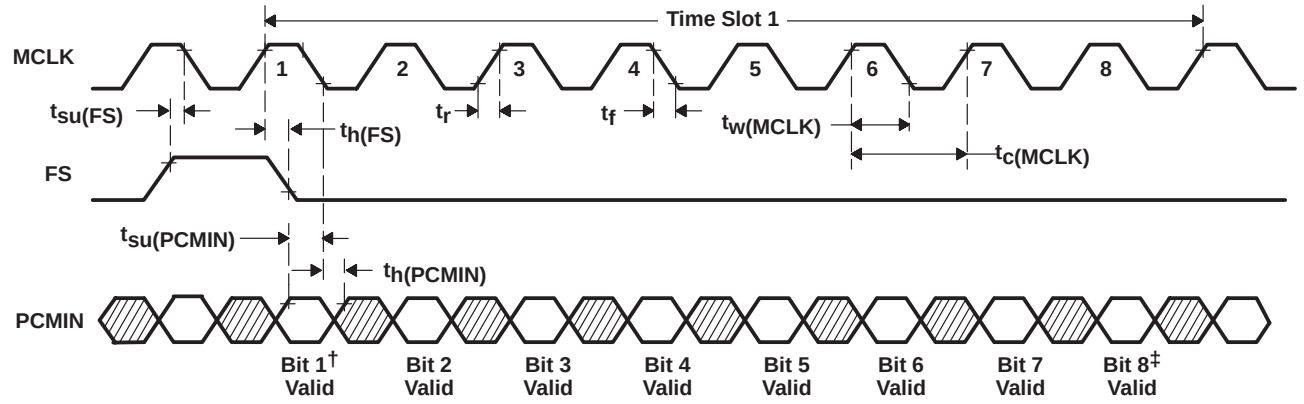
Figure 2. Receive-Filter Transfer Characteristics

PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = most significant bit and is clocked in first on the PCMIN terminal or is clocked out first on the PCMOUT terminal.
‡ Bit 8 = LSB = least significant bit and is clocked in last on the PCMIN terminal or is clocked out last on the PCMOUT terminal.

Figure 3. PCM Transmit Timing



† Bit 1 = MSB = most significant bit and is clocked in first on the PCMIN terminal or is clocked out first on the PCMOUT terminal.
‡ Bit 8 = LSB = least significant bit and is clocked in last on the PCMIN terminal or is clocked out last on the PCMOUT terminal.

Figure 4. PCM Receive Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

The TCM38C17IDL system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the QCombo is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the supply voltage drops momentarily below ground or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode with a forward voltage drop of less than or equal to 0.4 V (1N5711 or equivalent) between the power supply and GND (see Figure 5). It is possible that a QCombo-equipped card with an edge connector can not be hot inserted into a powered-up system. In this case, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

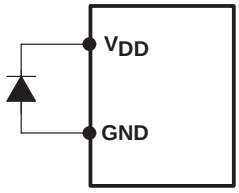


Figure 5. Latch-Up Protection Diode Connection

device power-up sequence

Latch-up also can occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply power.
4. Force a power down-condition in the device.
5. Connect the master clock.
6. Release the power-down condition.
7. Apply FS synchronization pulses.
8. Apply the analog signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

system reliability and design considerations (continued)

internal sequencing

On the transmit channel, digital output PCMOUT is held in the high-impedance state for approximately four frames (500 μs) after power up. Frame sync must be applied to all four channels during this time. After this delay, PCMOUT is functional and occurs in the proper timeslot. Valid digital information, such as for on/off hook detection, is available almost immediately.

To further enhance system reliability, PCMOUT is placed in a high-impedance state approximately 20 μs after an interruption of MCLK. This interruption could possibly occur with some kind of fault condition elsewhere in the system.

power-down operation

To minimize power consumption, a power-down mode is provided for each channel. To power down a channel, an external logic low signal is applied to the corresponding PDN terminal. In the power-down mode, the average power consumption is reduced to an average of 1 mW/channel.

miscellaneous

TCM38C17IDL timing and voltage references are described in the following paragraphs.

data timing

The TCM38C17IDL uses the 2.048 MHz master clock input to step data into and out of the device. An 8-kHz clock signal applied to the FS terminal sets the sampling frequency and indicates the beginning of data transfer. When MCLK goes low while FS is high, the frame sync is recognized. The next eight rising edges of MCLK step data out of PCMOUT, while data is received into PCMIN on the next eight falling edges of MCLK. It is recommended that frame sync pulses be one MCLK period in duration, but it is permissible for them to last up to seven MCLK periods from the recognition of the frame sync.

Frame syncs for channels 0 through 3 must occur sequentially. When all four channels are in use, the frame syncs (downward edge of MCLK during frame sync high) must occur at nominal 64 MCLK pulse intervals, making the frame syncs evenly distributed. When one or more channels are not in use, the active frame syncs have greater timing flexibility, but still must be separated by a minimum of 64 MCLK periods (nominal 31.25 μs with 2.048 MHz MCLK). See Figure 6.

PRINCIPLES OF OPERATION

system reliability and design considerations (continued)

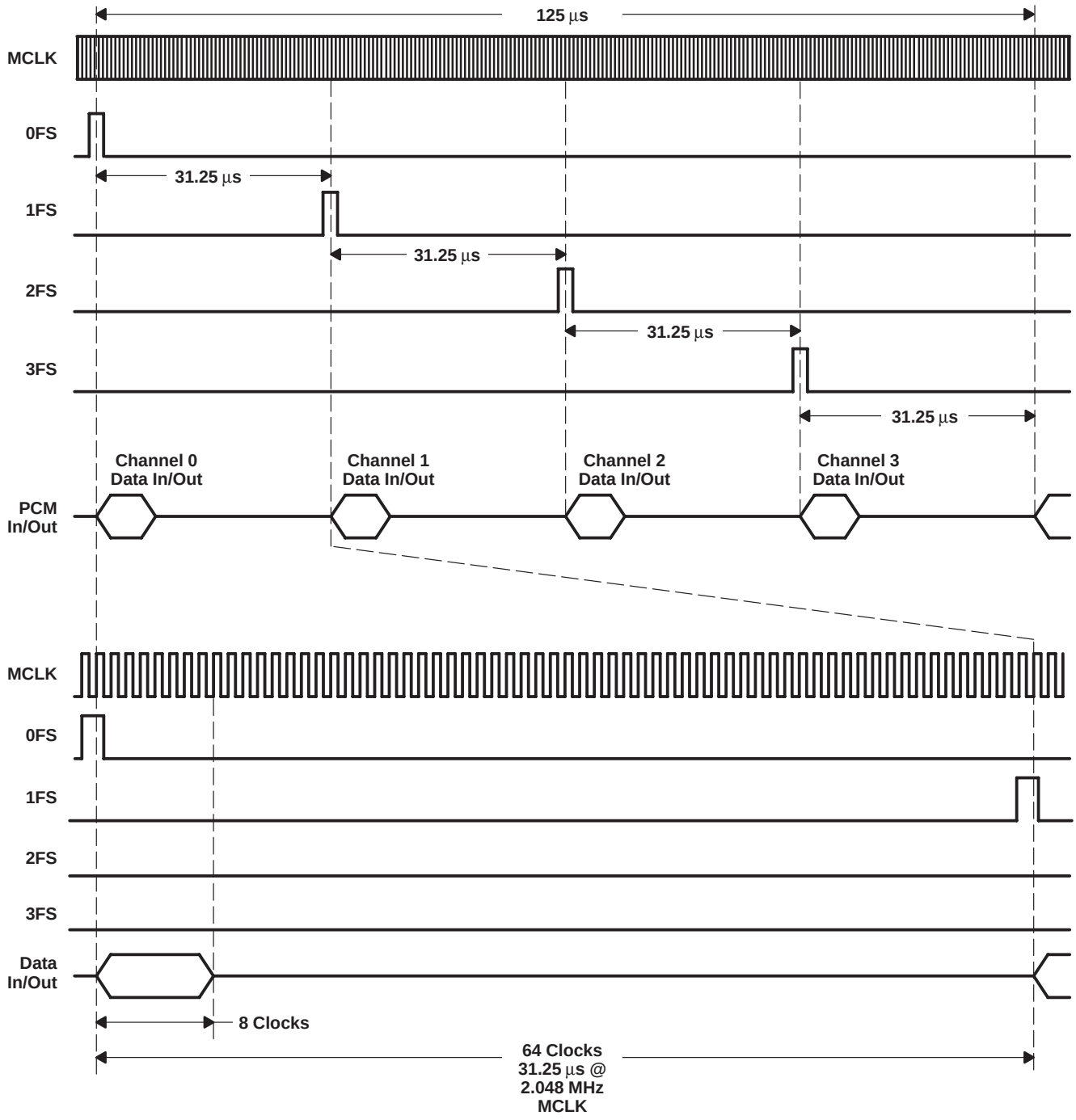


Figure 6. Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations (continued)

precision voltage references

It is recommended that an external 1-µF capacitor be connected between REFLTR1 and AVSS and between REFLTR2 and AVSS to ensure clean voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A band-gap mechanism is used to derive a temperature-independent and bias-stable reference voltage. These references are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.1 dB in absolute gain (voltage amplification) can be achieved for each half channel, providing the user a significant margin to compensate for error in other board components.

transmit operation

The TCM38C17IDL transmit operation is described in the following paragraphs.

transmit input amplifier

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. Gain for the amplifier is set using external input and feedback resistors as shown in Figure 7. This allows maximum flexibility in presetting volume levels. Unity gain can be achieved by assigning R_I and R_F equal values. The feedback impedance between GSX and ANLGIN should be greater than 10 kΩ in parallel with less than 50 pF. GSX also provides a means of sampling the amplified signal.

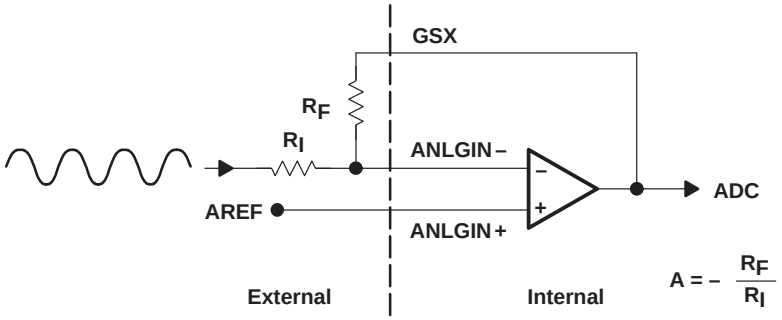


Figure 7. Transmit Path Gain Setting Circuitry

transmit filter

The transmit filters provide passband flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

PRINCIPLES OF OPERATION

receive operation

The TCM38C17IDL receive operation is described in the following paragraphs.

receive filter

The receive filters provide pass-band flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

output amplifier

The QCombo incorporates a versatile analog output power amplifier than can drive transformer hybrids or low-impedance loads directly in either a single-ended or differential configuration. The QCombo output stage allows for volume control (in the differential mode) by connection of a resistor divider chain to the output terminals of the device. The inverting operational amplifier can drive a 600 Ω load in parallel with 100 pF. Figure 8 is a representation of the internal structure of the output amplifier.

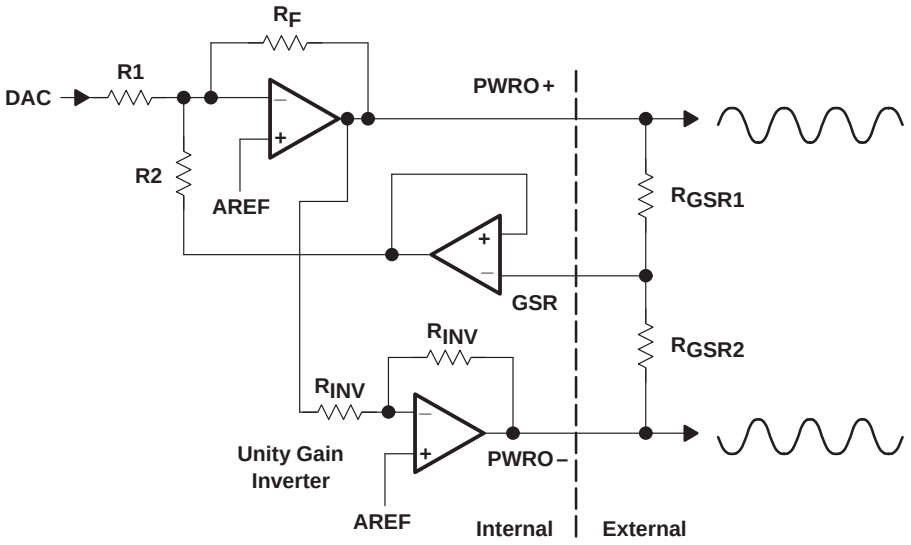


Figure 8. Output Amplifier Architecture

APPLICATION INFORMATION

Various TCM38C17IDL output configurations are detailed in the following paragraphs.

differential configuration

For connection to a transformer, the fully differential configuration is recommended to provide maximum possible output, or voltage swing, to the primary of an attached transformer. Figure 9 shows the QCombo in a fully-differential mode.

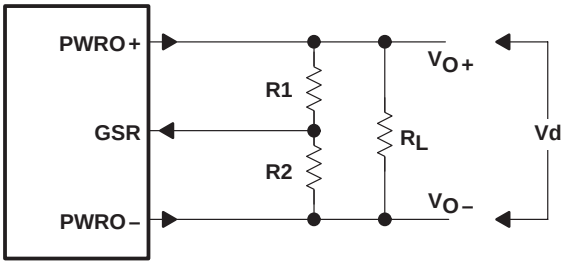


Figure 9. Fully Differential Gain-Setting Configuration

PWRO+ and PWRO– are low-impedance complementary outputs. The total output available for the output load (R_L) is then $V_D = V_{O+} – V_{O–}$. R1 and R2 form a gain-setting resistor network with a center tap connected to the GSR input.

R1 + R2 should be greater than 10 kΩ and less than 100 kΩ because the parallel combination R1 + R2 and R_L sets the total loading. The total parasitic capacitance of the GSR input, along with the parallel combination of R1 and R2, define a time constant that must be minimized to avoid inaccuracies in the gain calculations.

The resistor gain control actually consists of attenuating the full differential output voltage. The equation to determine the value of the attenuation constant is given in equation 1.

$$A = \frac{1 + (R1 \div R2)}{4 + (R1 \div R2)} \quad (1)$$

which can also be expressed as shown in equation 2.

$$A = \frac{R1 + R2}{4(R2 + R1 \div 4)} \quad (2)$$

where A = attenuation constant

Depending on the values of gain setting resistors R1 and R2, the attenuation constant (A) can have a value of 0.25 to unity (1), or approximately 12 dB of voltage adjustment.

APPLICATION INFORMATION

differential configuration (continued)

Maximum output (A = 1) can be obtained by maximizing R1 and minimizing R2. This can be done by letting R1 = infinity and R2 = 0 Ω (connect GSR to PWRO–), as shown in Figure 10. Referring to the transmit and receive gain and dynamic range specifications, a maximum output of approximately 8 Vpp can be expected in this configuration with a load ≥ 600 Ω. See the maximum analog output section for more detail on the digital input required for maximum analog output.

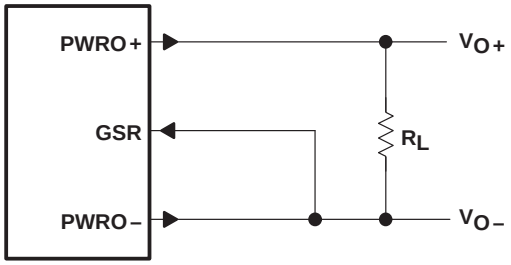


Figure 10. Fully Differential Maximum Gain-Setting Configuration (A = 1)

Figure 11 illustrates the QCombo with the resistor gain-control setting for an attenuation of A = 0.625.

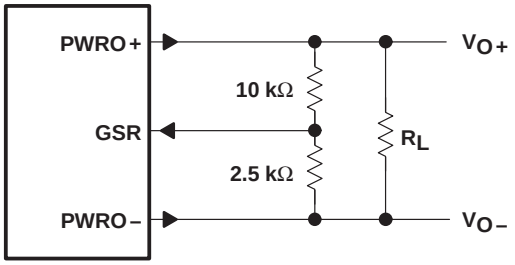


Figure 11. Fully Differential Mid-Gain-Setting Configuration (A = 0.625)

Shown in Figure 12, a minimum output (A = 0.25 dB) can be obtained by letting R1 = 0 Ω (connect GSR to PWRO+), and R2 = infinity.

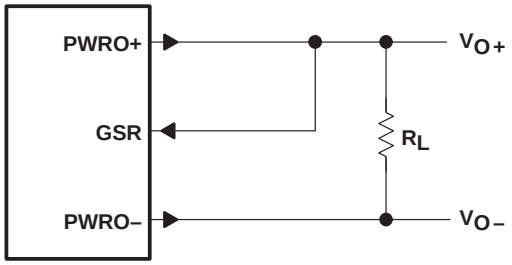


Figure 12. Fully Differential Minimum-Gain-Setting Configuration (A = 0.25)

APPLICATION INFORMATION

single-ended configuration

Figure 13 illustrates the QCombo in a typical single-ended configuration. Gain is set by manipulating the resistor network in the same way as detailed for the differential mode. A SLIC should be ac-coupled to the TCM38C17.

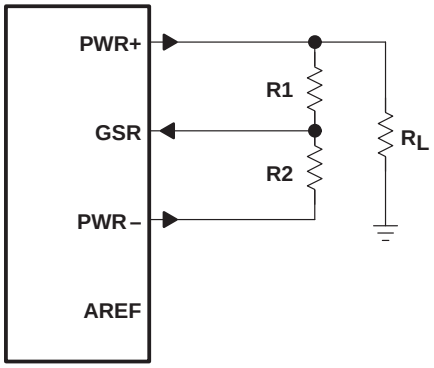
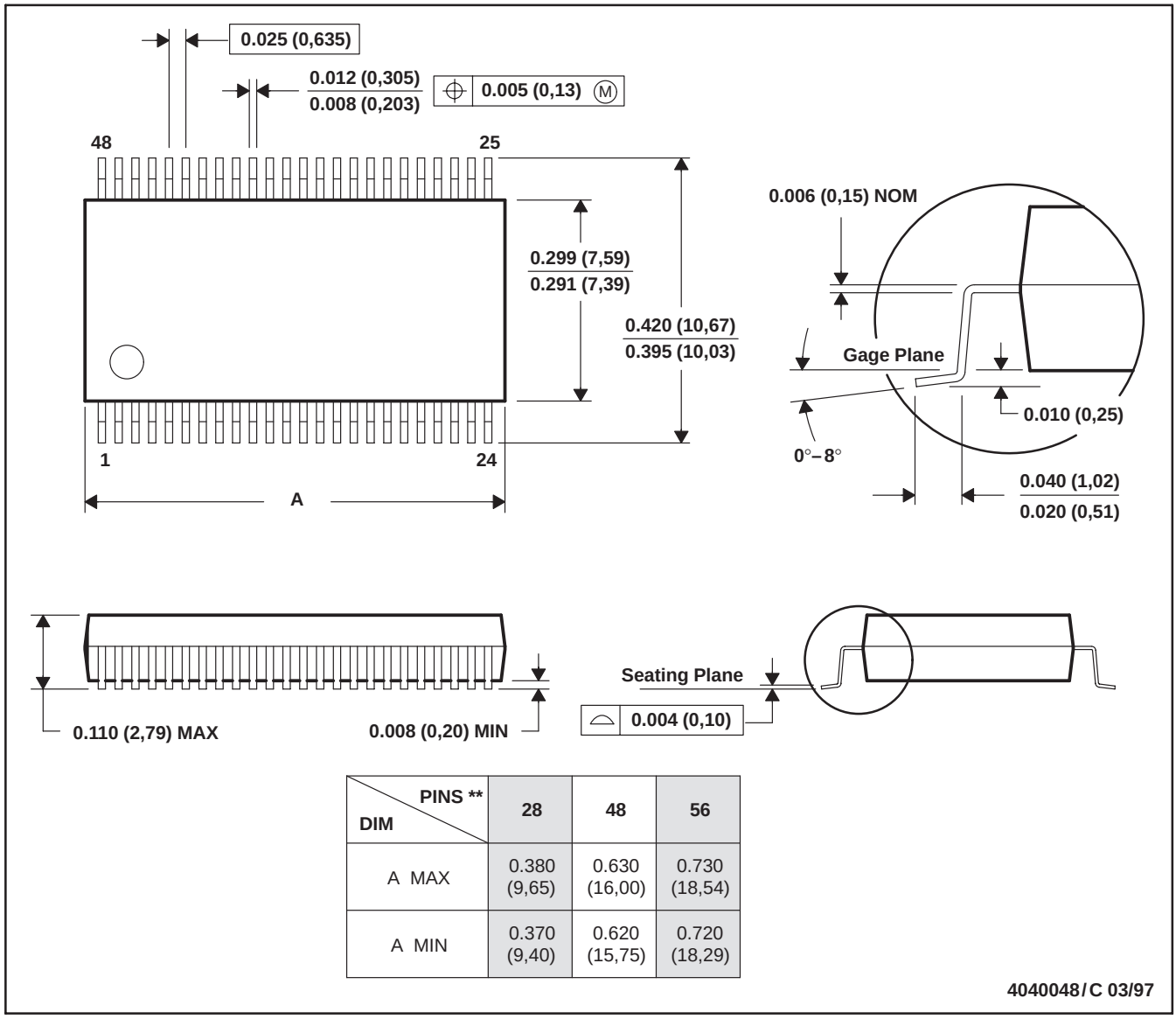


Figure 13. Single-Ended Configuration

MECHANICAL DATA

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/C 03/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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