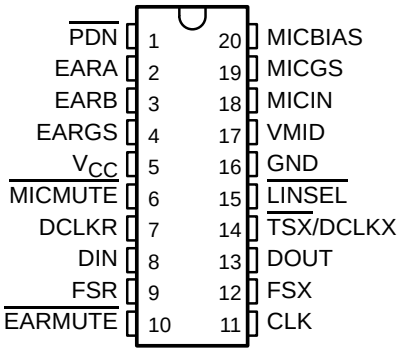
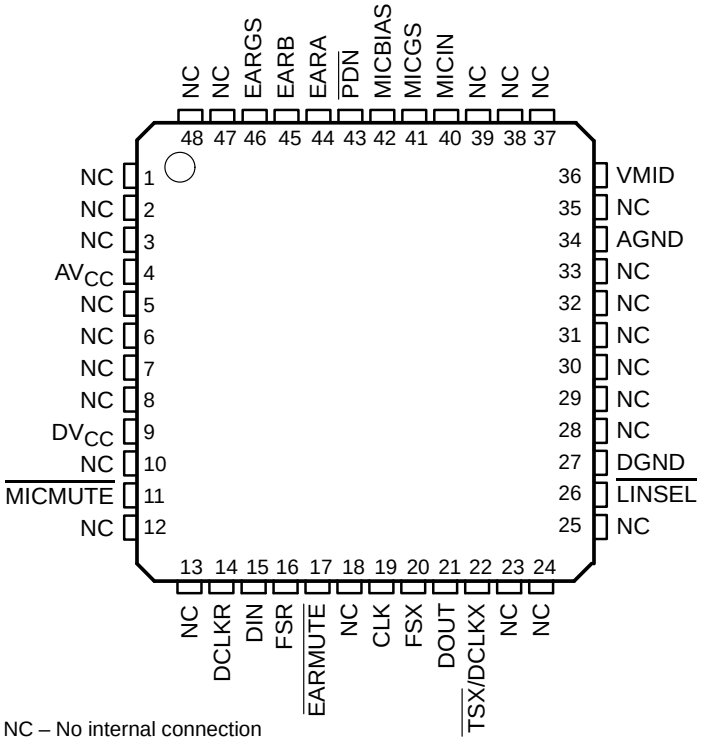
- **Single 3-V Operation**
- **Low Power Consumption:**
  - **Operating Mode . . . 20 mW Typ**
  - **Standby Mode . . . 5 mW Typ**
  - **Power-Down Mode . . . 2 mW Typ**
- **Combined A/D, D/A, and Filters**
- **Extended Variable-Frequency Operation**
  - **Sample Rates up to 16 kHz**
  - **Pass-Band up to 7.2 kHz**
- **Electret Microphone Bias Reference Voltage Available**
- **Drive a Piezo Speaker Directly**
- **Compatible With All Digital Signal Processors (DSPs)**
- **Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:**
  - **TLV320AC36 . . . μ-Law and Linear Modes**
  - **TLV320AC37 . . . A-Law and Linear Modes**
- **Programmable Volume Control in Linear Mode**
- **300 Hz – 3.6 kHz Passband with Specified Master Clock**
- **Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCS Standards for Hand-Held Battery-Powered Telephones**

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description

The TLV320AC36 and TLV320AC37 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data, and either three bits of gain-setting control data, or three zero bits of padding to create a16-bit word, are sent and received.

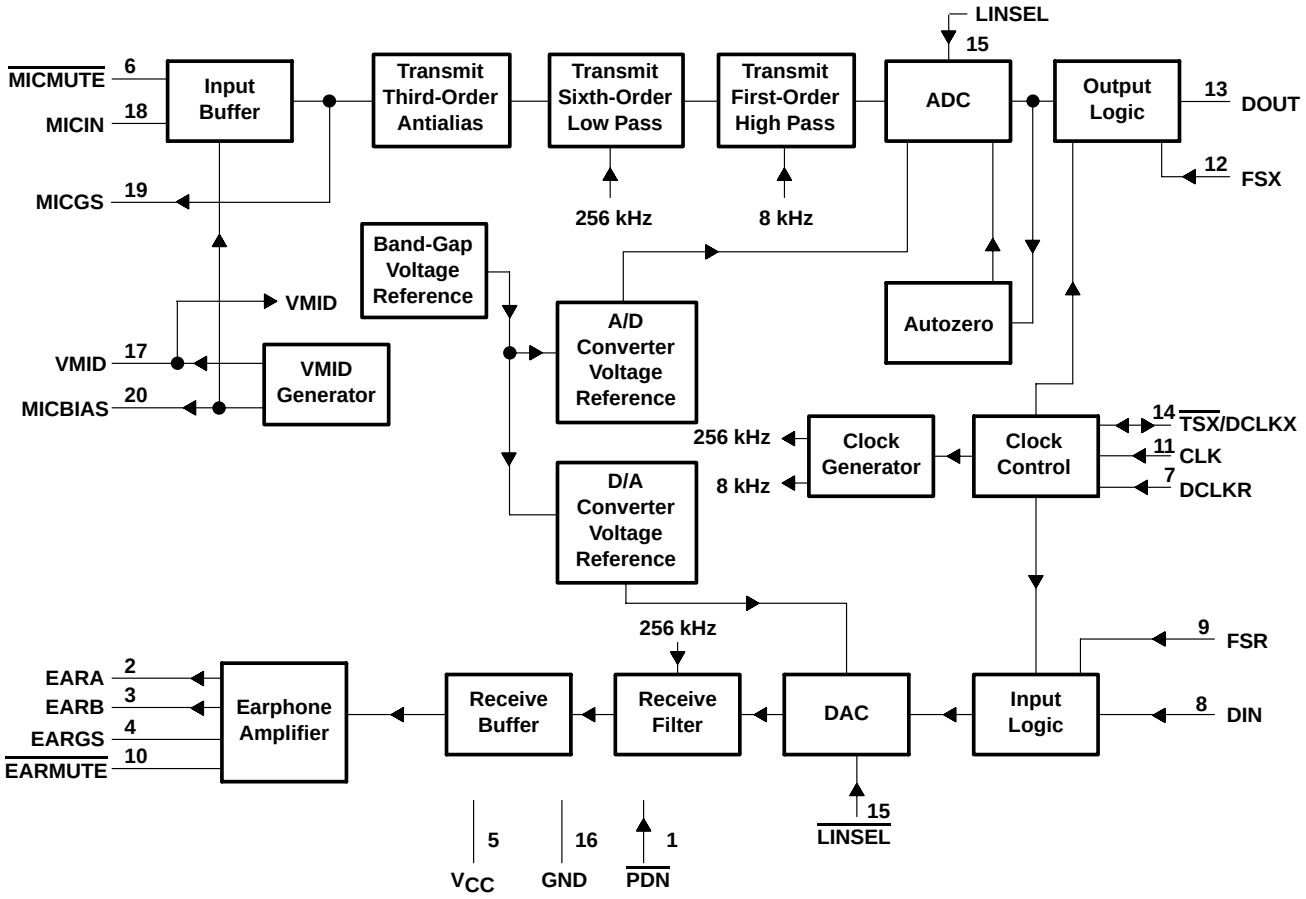
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TLV320AC3xC devices are characterized for operation from 0°C to 70°C. The TLV320AC3xI devices are characterized for operation from –40°C to 85°C.

functional block diagram



NOTE A: Terminal numbers shown are for the DW and N packages.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DW, N	PT		
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is μ-law, and companding code on the 'AC37 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe ($\overline{\text{TSX}}$ active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 5.5 V
Output voltage range at DOUT, V_O . . . . . –0.3 V to 5.5 V
Input voltage range at DIN, V_I . . . . . –0.3 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	3.3	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC36C, TLV320AC37C	0	70	°C
	TLV320AC36I, TLV320AC37I	–40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded, V_{CC} = 3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		7.5	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.75	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		4.5	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 3 V	2.4	2.8		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN‡				1.5		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
$I_O$max	Maximum output current	VMID		3			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
‡ The frequency of the first pole is 100 Hz.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3§	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
$I_O$max	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
§ 2.5 V_{pp} when V_{CC} is 2.7 V.

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC36)		0.614	Vrms
	Companded mode selected, A-law ('AC37)		0.616	
	Linear mode selected ('AC36 and 'AC37)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC36)		2.5	Vpp
	Companded mode selected, A-law ('AC37)		2.5	
	Linear mode selected ('AC36 and 'AC37)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at –10 dBm0	MICIN to DOUT at 0 dBm0 to –40 dBm0		±0.5	dB
	MICIN to DOUT at –41 dBm0 to –50 dBm0		±1.5	dB
	MICIN to DOUT at –51 dBm0 to –55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	–10	0	dB
		f_{MICIN} = 200 Hz	–2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	–0.55	0.2	
		f_{MICIN} = 3.4 kHz	–1	–0.1	
		f_{MICIN} = 4 kHz		–14	
		f_{MICIN} ≥4.6 kHz		–32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		–72	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –24 dBm0	36		dB
	MICIN to DOUT at –25 dBm0 to –30 dBm0	34		
	MICIN to DOUT at –31 dBm0 to –38 dBm0	30		
	MICIN to DOUT at –39 dBm0 to –40 dBm0	24		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –10 dBm0	46		dB
	MICIN to DOUT at –11 dBm0 to –12 dBm0	44		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC36)		3	Vpp
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 0 dBm0 to –38 dBm0		±0.5	dB
	DIN to EARA and EARB at –39 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	–0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	–0.55	0.2	
		f_{DIN} = 3.4 kHz	–1	–0.1	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		– 72	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to – 18 dBm0	36		dB
	DIN to EARA and EARB at – 19 dBm0 to – 24 dBm0	34		
	DIN to EARA and EARB at – 25 dBm0 to – 30 dBm0	30		
	DIN to EARA and EARB at – 31 dBm0 to – 38 dBm0	23		
	DIN to EARA and EARB at – 39 dBm0 to – 45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to – 12 dBm0	46		dB
	DIN to EARA and EARB at – 13 dBm0 to – 18 dBm0	38		
	DIN to EARA and EARB at – 19 dBm0 to – 24 dBm0	32		
	DIN to EARA and EARB at – 25 dBm0 to – 40 dBm0	18		
	DIN to EARA and EARB at – 41 dBm0 to – 45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level – 13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		– 30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		– 30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	50			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	50			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}$–40	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}$–35	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}$–35	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

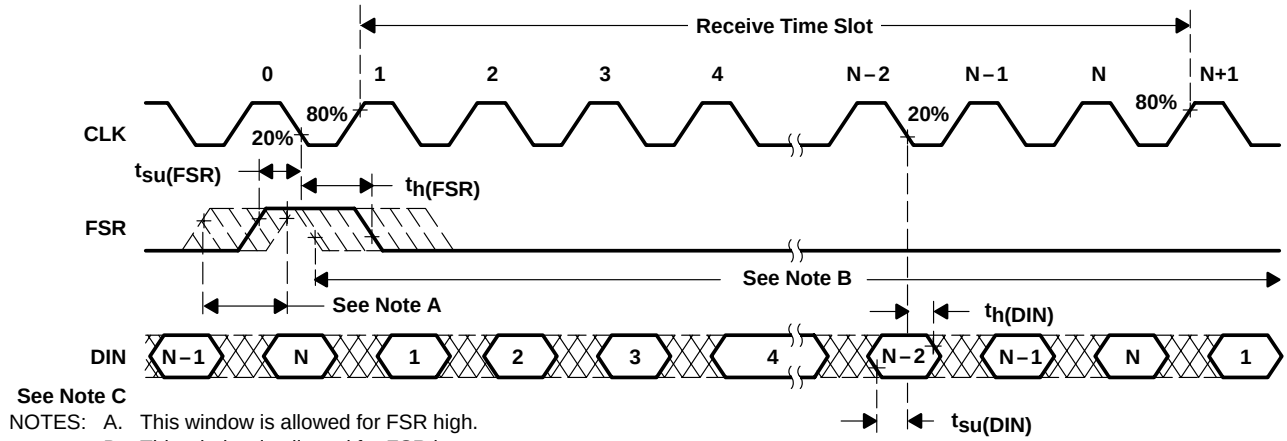
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

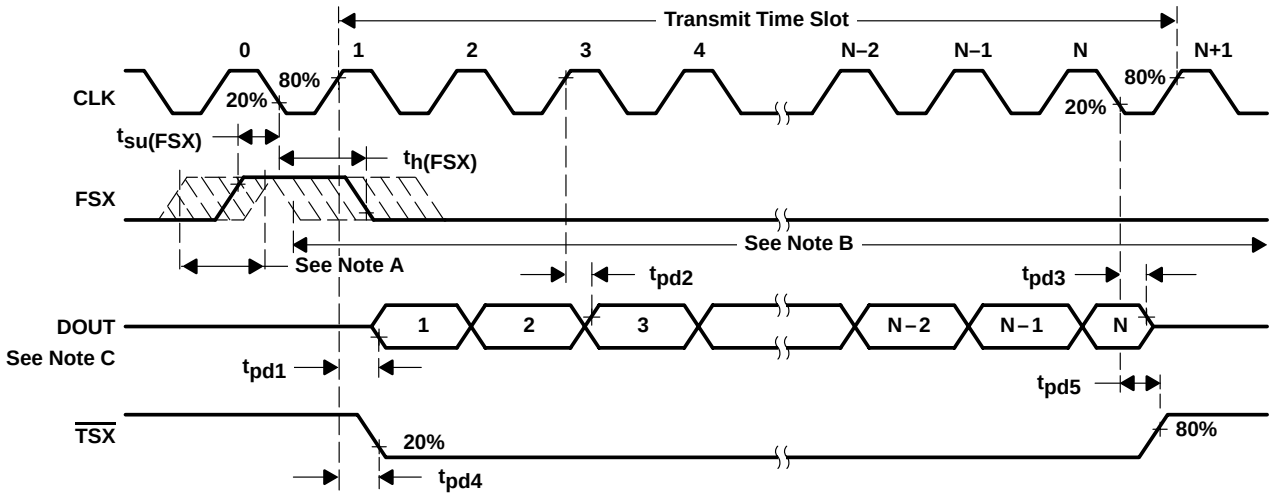
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

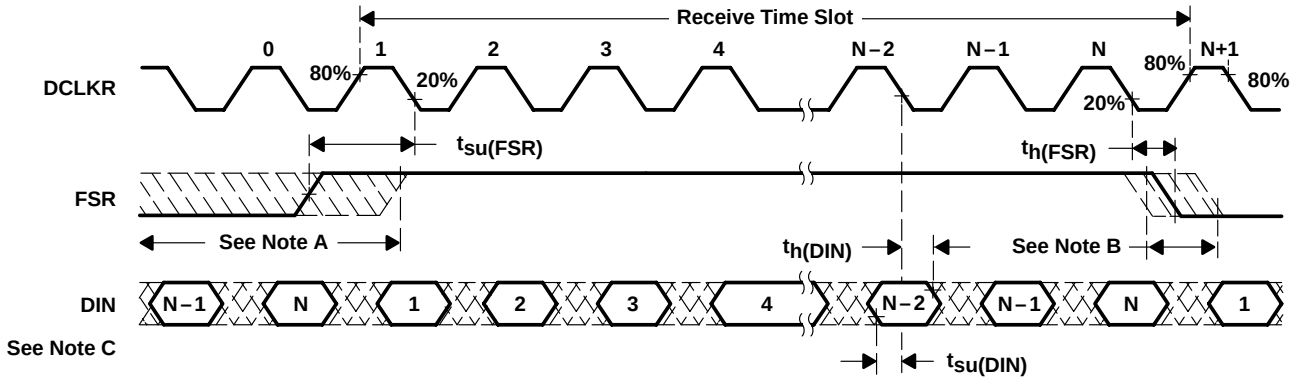
Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

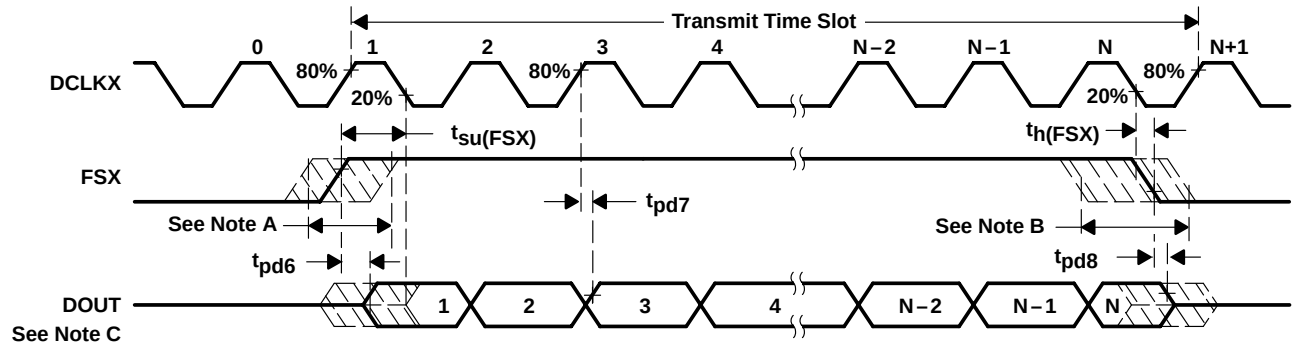
Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	2 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

† X = don't care

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

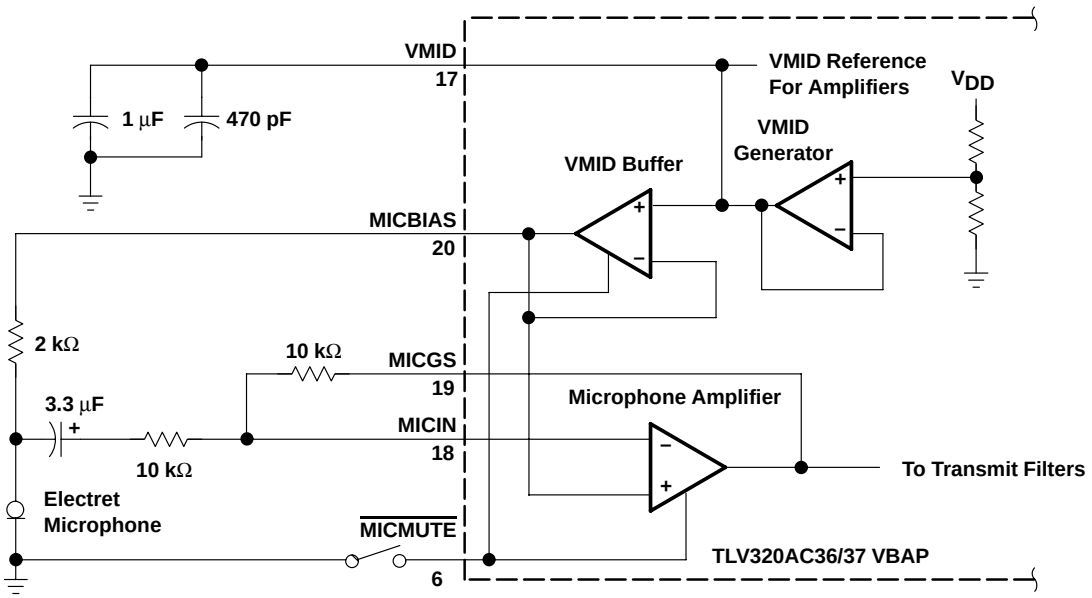
conversion laws

The TLV320AC36 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TLV320AC37 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TLV320AC36 and the TLV320AC37.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. In the companded mode, when the MICIN signal level decreases to a level near the noise floor, the VBAP mutes the signal and outputs zero bits while continuing to monitor the signal level. When the input level once again exceeds the noise threshold, the mute is released and normal operation resumes. Input hysteresis is provided to ensure noiseless transitions in to and out of the muted condition. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

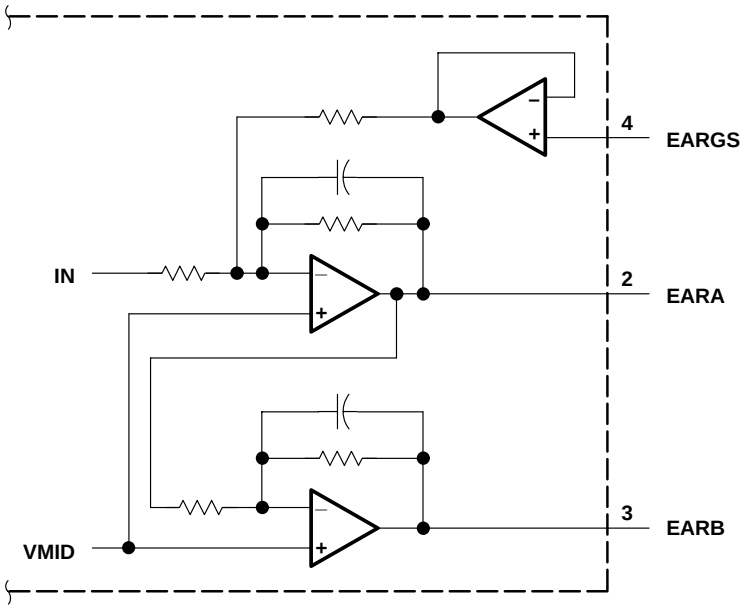
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

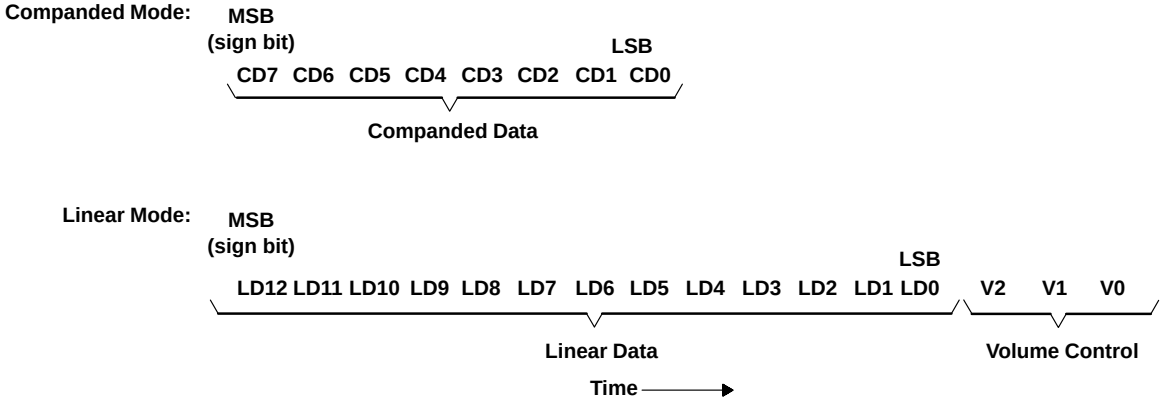
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0 = Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

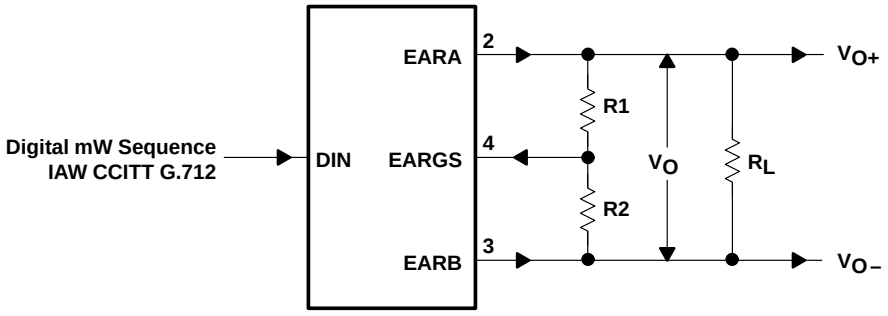
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 7. Gain-Setting Configuration

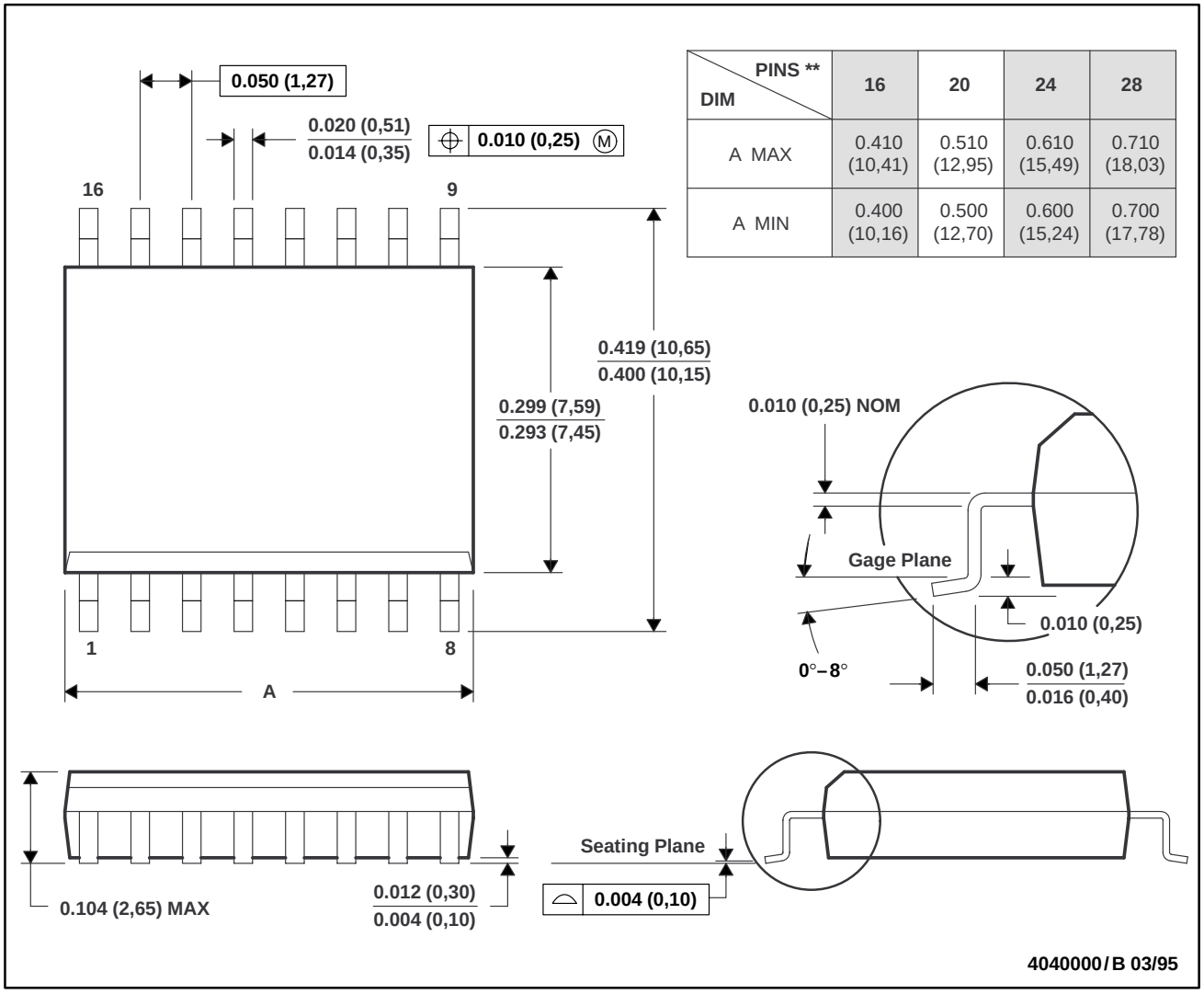
higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

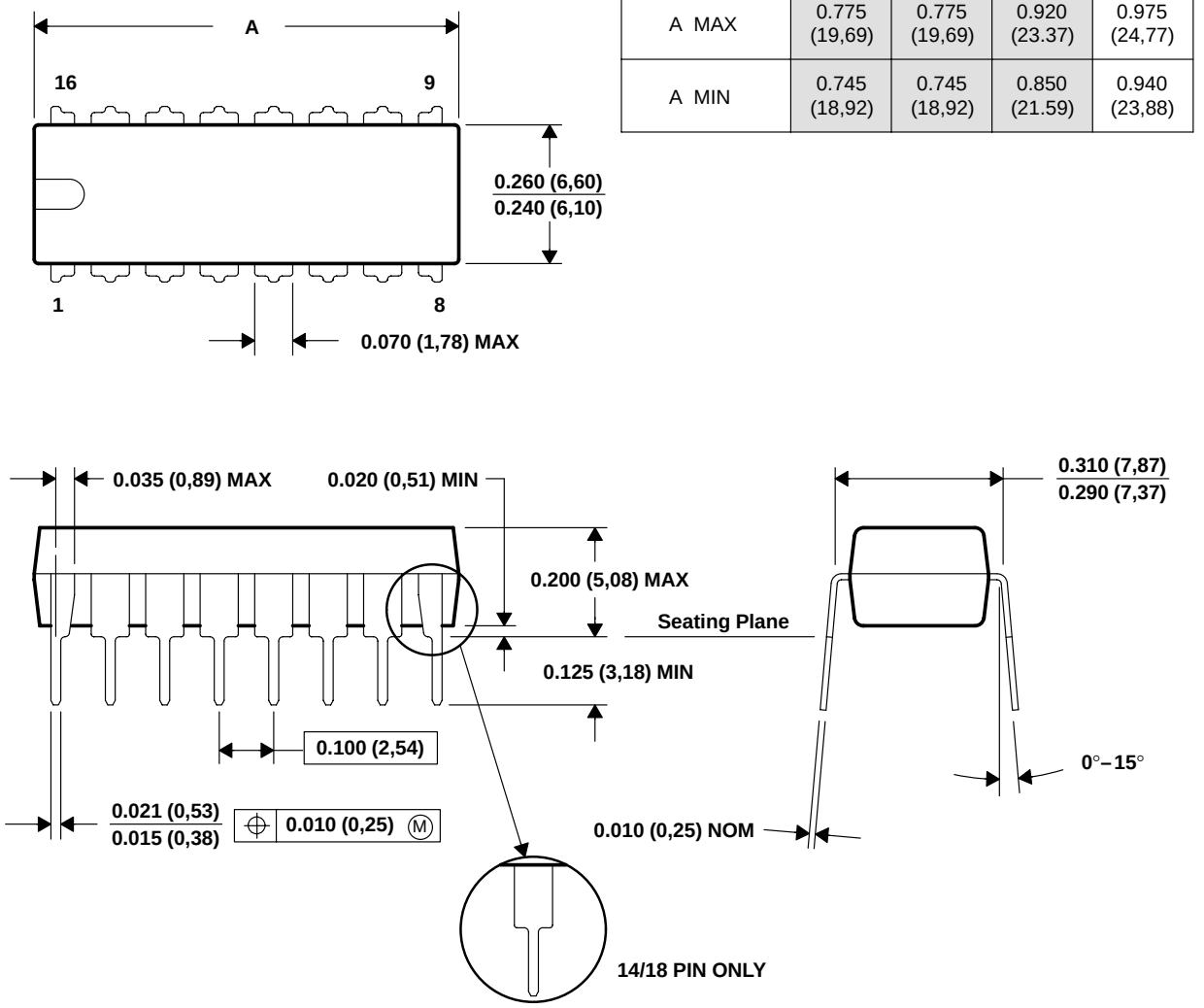
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

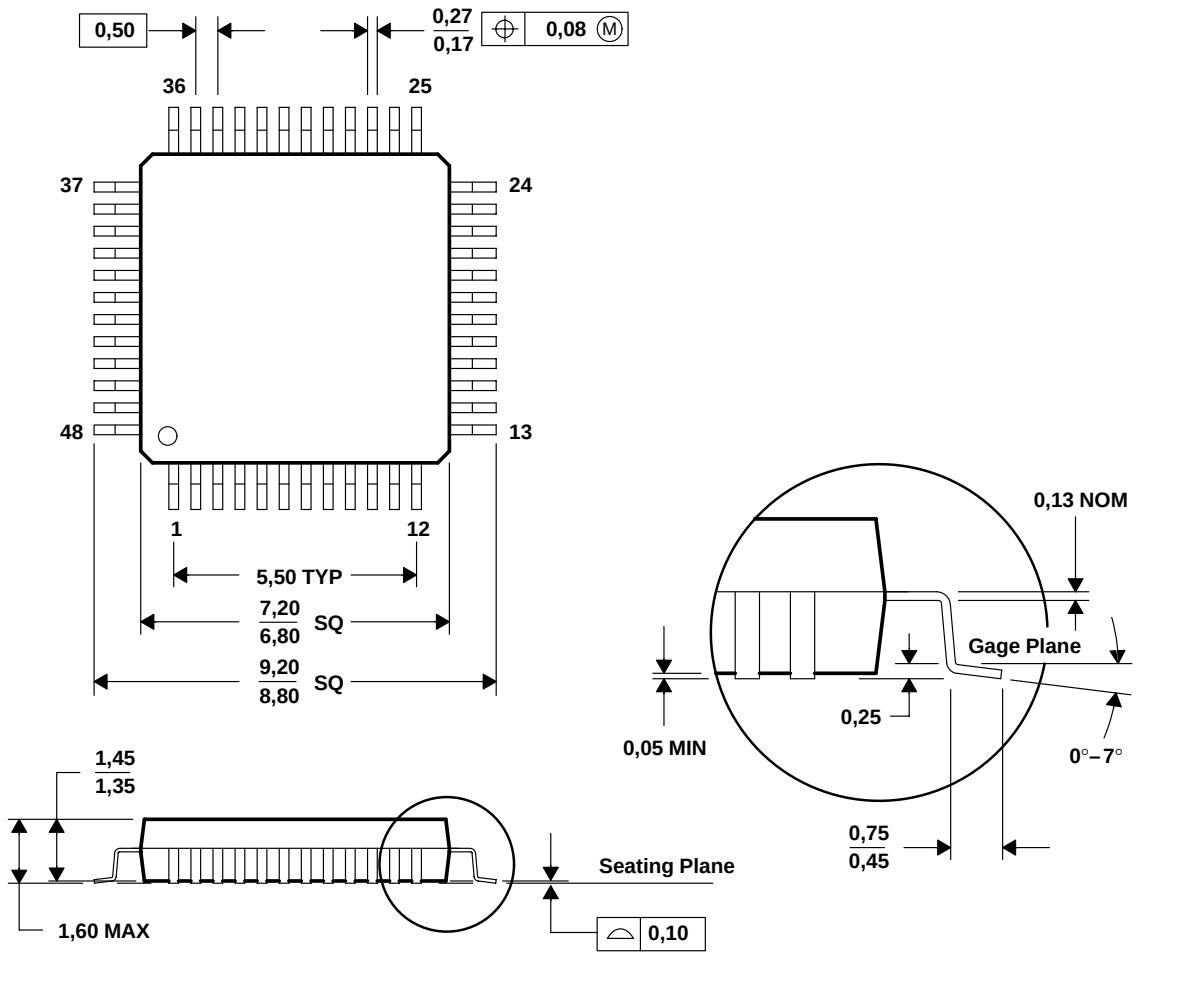
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally-enhanced plastic package with leads connected to the die pads.

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