TSB12LV21B
(PCILynx-2) IEEE 1394 LINK LAYER CONTROLLER

SLLS306– JULY 1998

- **IEEE Standard for a 1394-1995 Compliant**
- **IEEE Standard for a 1212-1991 Compliant**
- **Supports IEEE 1394-1995 Link Layer Control**
- **PCI Local Bus Specification Rev. 2.1 Compliant**
- **Supports IEEE 1394 Transfer Rates of 100, 200, and 400 Mb per second**
- **3.3-V Core Logic while Maintaining 5-V Tolerant Inputs**
- **Performs the Function of 1394 Cycle Master**
- **Provides 4K Bytes of Configurable FIFO RAM**
- **Provides 5 Scatter-Gather DMA Channels**
- **Provides Software Control of Interrupt Events**
- **Provides 4 General-Purpose Input/Outputs**
- **Supports Plug-and-Play (PnP) Specification**
- **Generates 32-bit CRC for Transmission of 1394 Packets**
- **Performs 32-bit CRC Checking on Reception of 1394 Packets**
- **Provides PCI Bus Master Function for Supporting DMA Operations**
- **Provides PCI Slave Function for Read/Write Access of Internal Registers**
- **Supports Distributed DMA Transfers Between 1394 and Local Bus RAM, ROM, AUX, or Zoomed Video**
- **Advanced Submicron, Low-Power CMOS Technology**
- **Packaged in a 176-Pin PQFP (PGF)**

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description

The TSB12LV21B (PCILynx-2) provides a high-performance IEEE 1394-1995 interface with the capability to transfer data between the 1394 PHY-link interface, the PCI bus interface, and external devices connected to the local bus interface. The 1394 PHY-link interface provides the connection to the 1394 physical layer device; it is supported by the on-board link layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and PHY-link interface at rates of 100 Mbit/s, 200 Mbit/s, and 400 Mbit/s. The link layer also provides the capability to receive status from the physical layer device and to access the physical layer control and status registers by the application software. The PCILynx–2 complies with

- PCI Local Bus Specification, Revision 2.1
- IEEE Standard for a 1394-1995 High Performance Serial Bus
- IEEE Standard 1212-1991
- IEEE Standard Control and Status Register (CSR) Architecture for Microcomputer Buses

An internal 4Kbyte-memory can be configured as multiple variable-size FIFOs, eliminating the need for external FIFOs. Separate FIFOs are user configurable to support 1394 receive, asynchronous transmit, and isynchronous transmit transfer operations.

The PCI interface supports 32-bit burst transfers up to 33 MHz and is capable of operating both as a master and as a target device. Configuration registers can be loaded from an external serial EEPROM, allowing board and system designers to assign their own unique identification codes. An autoboot mode allows data-moving systems (such as docking stations) to be designed to operate on the PCI bus without the need for a host CPU.

The DMA controller uses packet control list (PCL) data structures to control the transfer of data and allow the DMA to operate without host CPU intervention. These PCLs can reside in PCI memory or in memory that is connected to a local bus port. The PCLs implement an instruction set that allows linking, conditional branching, 1394 data transfer control, auxiliary support commands, and status reporting. Five DMA channels accommodate programmable data types. PCLs can be chained together to form a channel control program that can be developed to support each DMA channel. Data can be stored in either big endian or little endian format, eliminating the need for the host CPU to perform byte swapping. Data can be transferred either to 4-byte aligned locations, to provide the highest performance, or to nonaligned locations, to provide the best memory use.

The RAM, ROM, AUX, ZV, and general purpose I/O (GPIO) ports collectively make up the local bus interface. These ports mapped into the PCI address, can be accessed either through the PCI bus or through internal DMA transactions. Internal transactions do not appear on the external PCI bus, thereby conserving PCI bandwidth. DMA packet control lists or other data may be stored in external RAM or ROM attached to the local bus interface. This further reduces PCI bus use and generally improves performance. The ZV local bus port is designed to transfer data from 1394 video devices to an external device connected to the PCILynx-2 ZV port. This interface provides a method for receiving 1394 digital camera packets directly from a ZV-compliant device attached to the local bus interface.

Built-in test registers, a dedicated test output terminal, and four GPIO terminals allow observation of internal states and provide a convenient software debug capability. Programmable interrupts are available to inform driver software of important events, such as 1394 bus resets and DMA-to-PCL transfer completion.

The 3.3-V internal operation provides reduced power consumption, while maintaining compatibility with 5-V signaling environments. The PCI interface is compatible with both 3-V and 5-V PCI systems.

terminal assignment

PGF QUAD FLATPACK PACKAGE

TOP VIEW

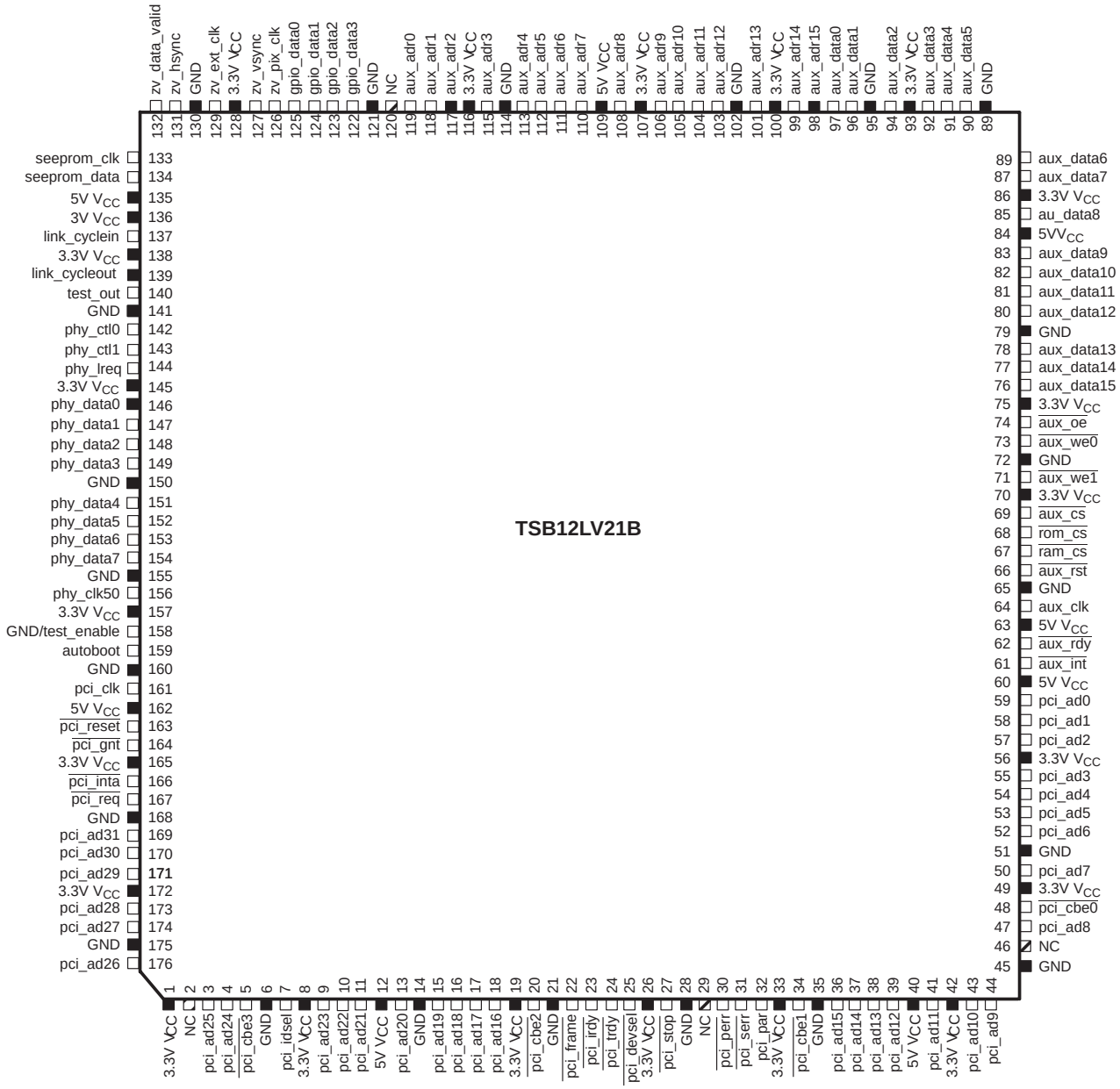

Figure 1. PCILynx-2 Terminal Assignment/Pinout

pin description table

This sections identifies and classifies the functionality of each pin on the PCILynx–2.

Table 1. Signals Sorted by Pin Number

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	3.3V V_{CC}	42	3.3V V_{CC}	83	aux_data9	124	gpio_data1
2	NC	43	pci_ad10	84	5.0VV_{CC}	125	gpio_data0
3	pci_ad25	44	pci_ad9	85	aux_data8	126	zp_pix_clk
4	pci_ad24	45	GND	86	3.3V V_{CC}	127	zv_vsync
5	pci_$\overline{cbe3}$	46	NC	87	aux_data7	128	3.3V V_{CC}
6	GND	47	pci_ad8	88	aux_data6	129	zv_ext_clk
7	pci_idsel	48	pci_$\overline{cbe0}$	89	GND	130	GND
8	3.3V V_{CC}	49	3.3V V_{CC}	90	aux_data5	131	zv_hsync
9	pci_ad23	50	pci_ad7	91	aux_data4	132	zv_data_valid
10	pci_ad22	51	GND	92	aux_data3	133	seeprom_clk
11	pci_ad21	52	pci_ad6	93	3.3V V_{CC}	134	seeprom_data
12	5.0V V_{CC}	53	pci_ad5	94	aux_data2	135	5V V_{CC}
13	pci_ad20	54	pci_ad4	95	GND	136	3V V_{CC}
14	GND	55	pci_ad3	96	aux_data1	137	link_cyclein
15	pci_ad19	56	3.3V V_{CC}	97	aux_data0	138	3.3VV_{CC}
16	pci_ad18	57	pci_ad2	98	aux_adr15	139	link_cylceout
17	pci_ad17	58	pci_ad1	99	aux_adr14	140	test_out
18	pci_ad16	59	pci_ad0	100	3.3V V_{CC}	141	GND
19	3.3V V_{CC}	60	5.0V V_{CC}	101	aux_adr13	142	phy_ctl0
20	pci_$\overline{cbe2}$	61	$\overline{aux\_int}$	102	GND	143	phy_ctl1
21	GND	62	$\overline{aux\_rdy}$	103	aux_adr12	144	phy_lreq
22	$\overline{pci\_frame}$	63	5.0V V_{CC}	104	aux_adr11	145	3.3V V_{CC}
23	$\overline{pci\_irdy}$	64	aux_clk	105	aux_adr10	146	phy_data0
24	$\overline{pci\_trdy}$	65	GND	106	aux_adr9	147	phy_data1
25	$\overline{pci\_devsel}$	66	$\overline{aux\_rst}$	107	3.3V V_{CC}	148	phy_data2
26	3.3V V_{CC}	67	$\overline{ram\_cs}$	108	aux_adr8	149	phy_data3
27	$\overline{pci\_stop}$	68	$\overline{rom\_cs}$	109	5.0V V_{CC}	150	GND
28	GND	69	$\overline{aux\_cs}$	110	aux_adr7	151	phy_data4
29	NC	70	3.3V V_{CC}	111	aux_adr6	152	phy_data5
30	$\overline{pci\_perr}$	71	$\overline{aux\_we1}$	112	aux_adr5	153	phy_data6
31	$\overline{pci\_serr}$	72	GND	113	aux_adr4	154	phy_data7
32	pci_par	73	$\overline{aux\_we0}$	114	GND	155	GND
33	3.3V V_{CC}	74	$\overline{aux\_oe}$	115	aux_adr3	156	phy_clk50
34	pci_$\overline{cbe1}$	75	3.3V V_{CC}	116	3.3V V_{CC}	157	3.3V V_{CC}
35	GND	76	aux_data15	117	aux_adr2	158	test_out/GND
36	pci_ad15	77	aux_data14	118	aux_adr1	159	auto_boot
37	pci_ad14	78	aux_data13	119	aux_adr0	160	GND
38	pci_ad13	79	GND	120	NC	161	pci_clk
39	pci_ad12	80	aux_data12	121	GND	162	5.0V V_{CC}
40	5.0V V_{CC}	81	aux_data11	122	gpio_data3	163	$\overline{pci\_reset}$
41	pci_ad11	82	aux_data10	123	gpio_data2	164	$\overline{pci\_gnt}$

Table 1. Signals Sorted by Pin Number (Continued)

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
165	3.3V V_{CC}	168	GND	171	pci_ad29	174	pci_ad27
166	pci_inta	169	pci_ad31	172	3.3V V_{CC}	175	GND
167	pci_req	170	pci_ad30	173	pci_ad28	176	pci_ad26

Terminal Functions

power supply terminals

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
GND	6, 14, 21, 28, 35, 45, 51, 65, 72, 79, 89, 95, 102, 114, 121, 130, 141, 150, 155, 160, 168, 175	I	Device ground terminals
3.3V VCC	1, 8, 19, 26, 33, 42, 49, 56, 70, 75, 86, 93, 100, 107, 116, 128, 136, 138, 145, 157, 165, 172	I	3.3-V power supply terminal for core logic
5.0V VCC	12, 40, 60, 63, 84, 109, 162	I	5-V power rail for 5-V tolerant Input buffers

PCI system terminals

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
pci_clk	161	I	System PCI bus clock. This signal ranges from 0MHz–-33MHz MHz and provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
pci_reset	163	I	pci_reset. When the PCI bus reset is asserted the pci_reset signal causes the PCILynx-2 to 3-state all output buffers and reset all internal registers. When pci_reset is asserted, the device is completely nonfunctional. After pci_reset is deasserted, the PCILynx-2 is in its default state.
pci_inta	166	OD	PCI system interrupt A. This is an open drain signal.

Terminal Functions (Continued)

PCI address and data terminals

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
pci_ad31 – pci_ad29 pci_ad28 pci_ad27 pci_ad26 pci_ad25 pci_ad24 pci_ad23 – pci_ad21 pci_ad20 pci_ad19 – pci_ad16 pci_ad15 – pci_ad12 pci_ad11 pci_ad10 pci_ad9 pci_ad8 pci_ad7 pci_ad6 – pci_ad3 pci_ad2 – pci_ad0	169 – 171 173 174 176 3 4 9 – 11 13 15 – 18 36 – 39 41 43 44 47 50 52 – 55 57 – 59	I/O	Multiplexed PCI address and data signals. During the address phase of a primary bus PCI cycle, pci_ad31:0 contain a 32-bit address or other destination information. During the data phase pci_ad31:0 contain data
pci_$\overline{cbe3}$ pci_$\overline{cbe2}$ pci_$\overline{cbe1}$ pci_cbe0	5 20 34 48	I/O	PCI Command/Byte enables
pci_par	32	I/O	PCI bus parity. In all PCI bus read and write cycles the PCILynx–2 calculates even parity across the pci_ad31:0 and pci_cbe3:0 signals. As an initiator during PCI cycles, the PCILynx-2 outputs this parity indicator with a one pci_clk delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator. A miscompare can result in the assertion of a parity error ($\overline{pci\_perr}$).

Terminal Functions (Continued)

PCI interface control

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
pci_devsel	24	I/O	PCI device select. The PCILynx-2 asserts this signal to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCILynx-2 monitors this signal until a target responds. If no target responds before time-out occurs, then the PCILynx-2 will terminate the cycle with an initiator abort.
pci_frame	22	I/O	PCI cycle frame. This signal is driven by the initiator of a bus cycle. pci_frame is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When pci_frame is deasserted the PCI bus transaction is in the final data phase.
pci_gnt	164	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the PCILynx-2 access to the PCI bus after the current data transaction has completed. This signal may or may not follow a PCI bus request depending upon the PCI bus parking algorithm.
pci_idsel	7	I	Initialization device select. pci_idsel selects the PCILynx-2 during configuration space accesses. pci_idsel can be connected to one of the upper 24 PCI address lines on the PCI bus.
pci_irdy	23	I/O	PCI initiator ready. pci_irdy indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of pci_clk where both pci_irdy and pci_trdy are asserted. Until pci_irdy and pci_trdy are both sampled asserted, wait states are inserted.
pci_perr	30	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match pci_par, when pci_perr is enabled through bit 6 of the command register.
pci_req	167	O	PCI bus request. Asserted by the PCILynx-2 to request access to the PCI bus as an initiator.
pci_serr	31	OD	PCI system error. Output that is pulsed from the PCILynx-2 when enabled through the command register, indicating a system error has occurred. The PCILynx-2 needs not be the target of the PCI cycle in order to assert this signal.
pci_stop	27	I/O	PCI cycle stop signal. This signal is driven by a PCI target to request the initiator to stop the current PCI bus transaction. This signal is used for target disconnects and is commonly asserted by target devices which do not support burst data transfers.
pci_trdy	24	I/O	PCI target ready. pci_trdy indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of pci_clk where both pci_irdy and pci_trdy are asserted. Until both pci_irdy and pci_trdy are asserted, wait states are inserted.

IEEE 1394 PHY/LINK interface terminals

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
phy_ctl1 phy_ctl0	143 142	I/O	PHY-link bidirectional control lines
phy_data7 – phy_data4 phy_data3 – phy_data0	154 – 151 149 – 146	I/O	PHY-link bidirectional data lines
phy_clk50	156	I	50MHz-System clock from PHY chip
phy_lreq	144	O	PHY-link request signal generated by the PCILynx-2 controller

Terminal Functions (Continued)

auxiliary/zoom video port terminals

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
aux_clk	64	O	Auxiliary port clock out. This signal is output at the frequency of the PCI clock.
$\overline{\text{aux\_rst}}$	66	O	Auxiliary port reset out
$\overline{\text{aux\_int}}$	61	I	Auxiliary port interrupt input
aux_adr15 – aux_adr14 aux_adr13 aux_adr12 –aux_adr9 aux_adr8 aux_adr7 –aux_adr4 aux_adr3 aux_adr2 – aux_adr0	98 – 99 101 103 – 106 108 110 – 113 115 117 – 119	O	Auxiliary port address lines output to external logic
aux_data15 – aux_data13 aux_data12 – aux_data9 aux_data8 aux_data7 – aux_data6 aux_data5 – aux_data3 aux_data2 aux_data1 – aux_data0	76 – 78 80 – 83 85 87 – 88 90 – 92 94 96 – 97	I/O	Auxiliary port bidirectional data bus to external logic
$\overline{\text{aux\_cs}}$	69	O	Auxiliary port chip select to external logic
$\overline{\text{aux\_oe}}$	74	O	Auxiliary port output enable to enable external logic data onto the auxiliary data bus
$\overline{\text{aux\_rdy}}$	62	I	Auxiliary port ready indication from external logic
$\overline{\text{aux\_we1}}$ $\overline{\text{aux\_we0}}$	71 73	O	Auxiliary port write strobes to external logic
$\overline{\text{ram\_cs}}$	67	O	External RAM chip select
$\overline{\text{rom\_cs}}$	68	O	External ROM chip select
zv_data_valid	132	O	Zoom video port data valid signal
zv_ext_clk	129	I	Zoom video port external clock input
zv_hsync	131	O	Zoom video port horizontal sync signal
zv_pix_clk	126	I/O	Zoom video port pixel clock for zoomed video data
zv_vsync	127	O	Zoom video port vertical sync signal

miscellaneous

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
autoboot	159	I	Autoboot. Selects autoboot mode. When this terminal is tied high, autoboot mode is selected.
gpio_data3 – gpio_data2	122 – 125	I/O	Auxiliary port general-purpose programmable I/O signals
link_cyclein	137	I	Optional 8kHz clock for use as the cycle clock
link_cycleout	140	O	Cycle timer 8kHz clock output
seeprom_clk	133	I/O	External serial EEPROM data clock
seeprom_data	134	I/O	External serial EEPROM read/write data line
test_enable/GND	158	I	Enables TEST_OUT for AND tree testing. This pin should be tied to GND if AND tree testing is not used.
test_out	140	O	Output for AND tree testing

system block diagram

The following figure illustrates a typical system implementation of the PCILynx-2.

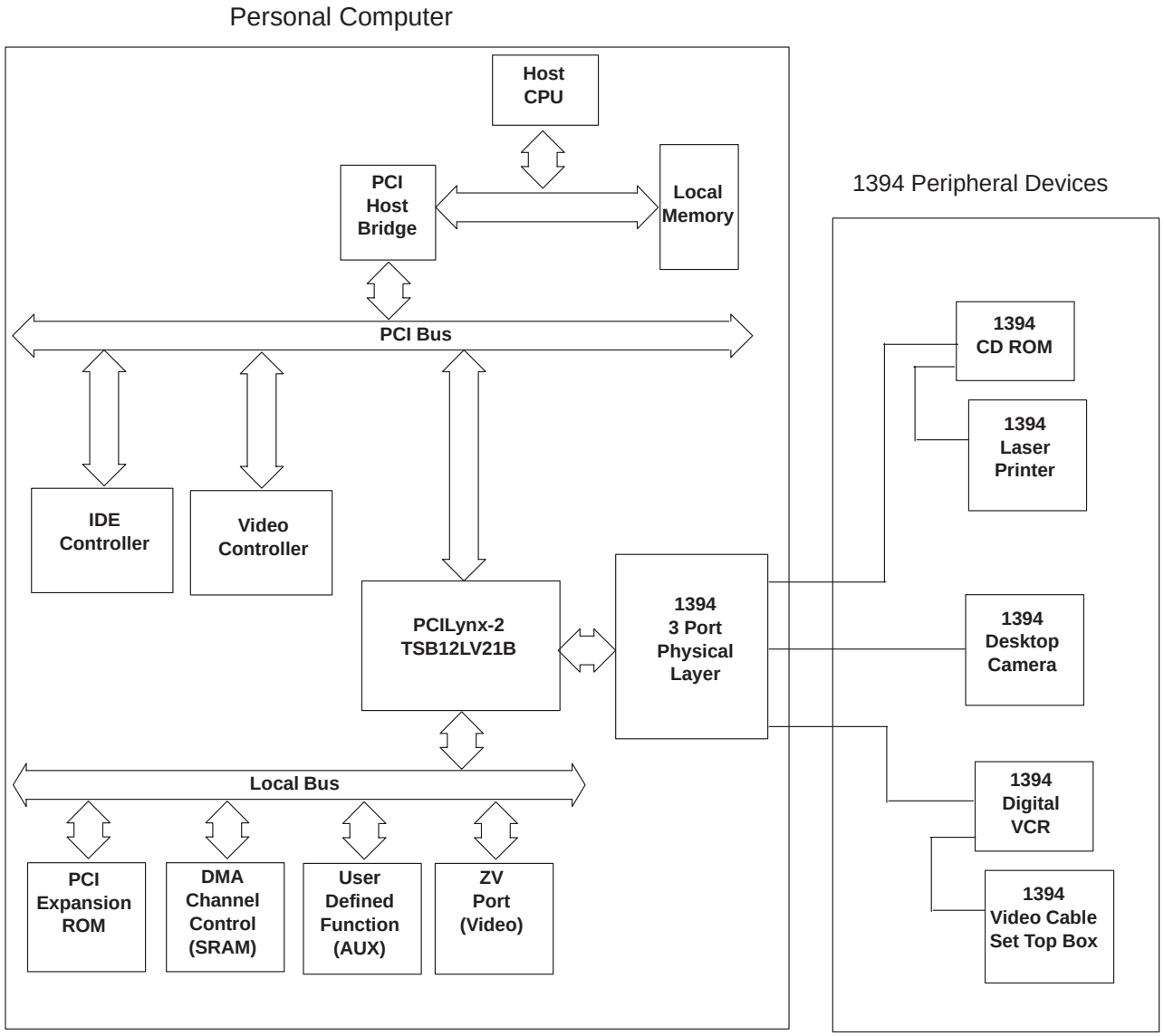

Figure 2. System Block Diagram

functional block diagram

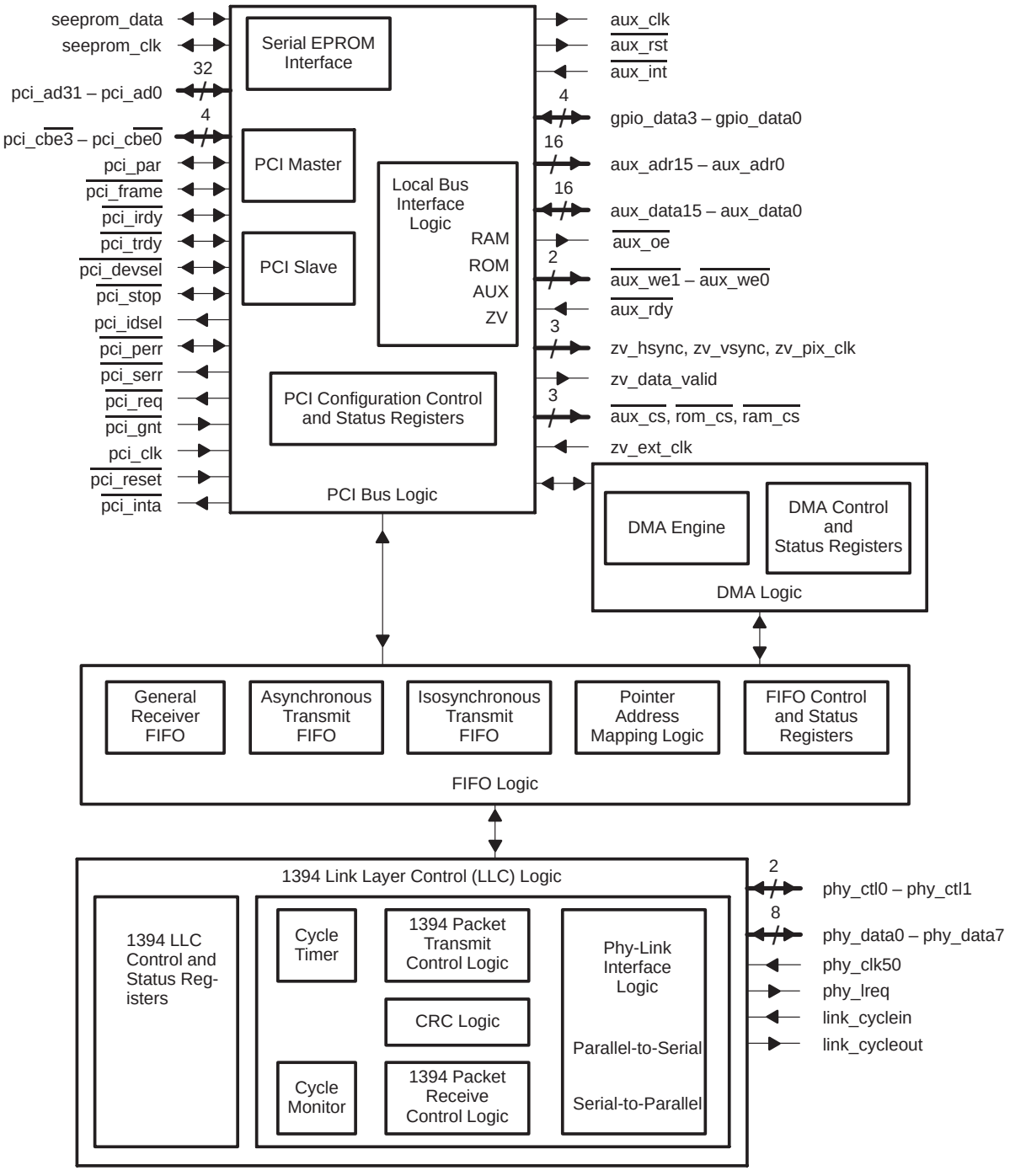

Figure 3. Functional Block Diagram

TEXAS INSTRUMENTS
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absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
V_{CCP} . . . . . –0.5 V to 6 V
V_{CC5V} . . . . . –0.5 V to 6 V
Input voltage range for Universal PCI, V_I: PCI . . . . . –0.5 V to V_{CCP} + 0.5 V
Input voltage range for 5-V tolerant TTL/LVCMOS, V_I: . . . . . –0.5 V to V_{CC5V} + 0.5 V
Output voltage range for Universal PCI, V_O . . . . . –0.5 V to V_{CCP} + 0.5 V
Output voltage range for 5-V tolerant TTL/LVCMOS, V_O . . . . . –0.5 V to V_{CC5V} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) . . . . . ± 20 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers. For 5-V tolerant buffers, use V_I > V_{CC5V}. For Universal PCI, use V_I > V_{CCP}.
2. Applies to external output and bidirectional buffers. For 5-V tolerant buffers, use V_O > V_{CC5V}. For Universal PCI, use V_O > V_{CCP}.

recommended operating conditions (see Note 3)

		OPERATION	MIN	NOM	MAX	UNIT
Core voltage, V_{CC}	Commercial	3.3	3	3.3	3.6	V
I/O voltage, V_{CCP}	Commercial	5	3	5	5.5	V
I/O voltage, V_{CC5V}	Commercial	5	3	5	5.5	V
High-level Input voltage, V_{IH}†			2			V
Low-level Input voltage, V_{IL}†					0.8	V
Input voltage, V_I	Universal PCI		0		V_{CCP}	V
	5-V tolerant		0		V_{CC5V}	
Output voltage, V_O‡			0		V_{CC}	V
Input transition times (t_r and t_f), t_t			0		6	ns
Operating ambient temperature range, T_A			0	25	70	°C
Virtual junction temperature, T_J§			0	25	115	°C

† Applies for external input and bidirectional buffers without hysteresis.
‡ Applies for external output buffers.
§ These junction temperatures reflect simulation conditions. Customer is responsible for verifying junction temperature.
NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (see Note 4)	PCI		3.3 V	I_{OH} = –0.5 mA	0.9 V_{CC}		V
				5 V	I_{OH} = –2 mA	2.4		
		TTL/LVCMOS†			I_{OH} = –18 mA	2.4		
		TTL/LVCMOS‡			I_{OH} = –14 mA	2.4		
V_{OL}	Low-level output voltage	PCI		3.3 V	I_{OL} = 1.5 mA		0.1 V_{CC}	V
				5 V	I_{OL} = 6 mA		0.5	
		TTL/LVCMOS†			I_{OL} = 18 mA		0.5	
		TTL/LVCMOS‡			I_{OL} = 14 mA		0.5	
I_{IL}	Low-level input current	Input pins	Bushold		V_I = 0.8 V		20	µA
			Others		V_I = GND		–1	
		I/O pins	Bushold		V_I = 0.8 V		400	
			Others		V_I = GND		–20	
I_{IH}	High-level input current	Input pins	Bushold		V_I = 2 V		–20	µA
			Others		V_I = 5.5 V		20	
		I/O pins	Bushold		V_I = 2 V		–20	
			Others		V_I = 5.5 V		20	

† All PHY-link pins, aux_clk(64), $\overline{\text{aux\_we1}}$(71), and $\overline{\text{aux\_we0}}$(73).
‡ All other TTL/LVCMOS pins
NOTE 4: V_{OH} is not tested on $\overline{\text{pci\_serr}}$(31) or $\overline{\text{pci\_inta}}$(166) due to open-drain output.

PCI interface switching characteristics, see Figure 4

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su1}	Setup time, pci_xx low or high to pci_clk high†	40% to 40%		7			ns
t_{h1}	Hold time, pci_clk high to pci_xx low or high†, $\overline{\text{pci\_gnt}}$ low or high	40% to 40%		0			ns
t_{d1}	Delay time, pci_clk high to pci_xx low or high†	40% to 40%		2		11	ns
t_{su2}	Setup time, $\overline{\text{pci\_gnt}}$ low or high to pci_clk high	40% to 40%		10			ns
t_{d2}	Delay time, pci_clk high to $\overline{\text{pci\_inta}}$ low or high	40% to 40%		2		13	ns

† In this case, pci_xx refers to the following signals; pci_ad31–0, pci_cbe3–0, pci_par, pci_frame, pci_irdy, pci_trdy, pci_devsel, pci_stop, pci_idsel, pci_perr, pci_serr, pci_req.

phy-link interface switching characteristics, see Figure 5

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su3}	Setup time, phy_xx low or high to phy_clk high†	1.3 V to 1.3 V		4			ns
t_{h2}	Hold time, phy_clk high to phy_xx, link_cyclein low or high	1.3 V to 1.3 V		1			ns
t_{d3}	Delay time, phy_clk high to phy_xx, phy_lreq low or high†	1.3 V to 1.3 V		3		11	ns
t_{su4}	Setup time, phy_clk high to link_cyclein low or high	1.3 V to 1.3 V		5			ns
t_{d4}	Delay time, phy_clk high to link_cycleout low or high	1.3 V to 1.3 V		3		13	ns

† In this case, phy_xx refers to the following bidirectional signals; phy_ctl1–0, phy_data7–0.

local bus switching characteristics, see Figure 6

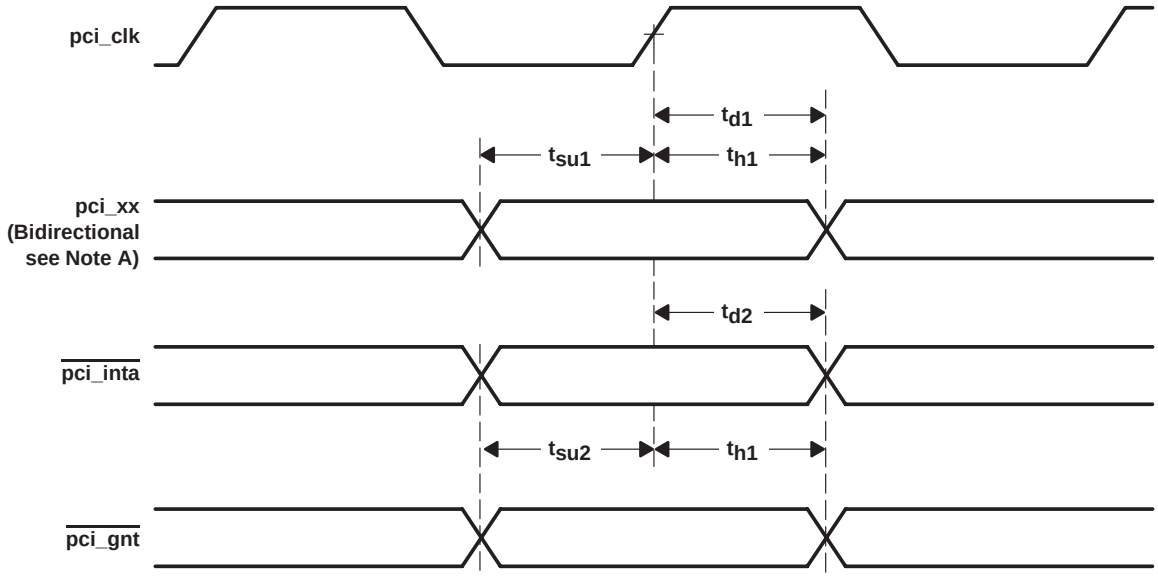
PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{d5}	Delay time, aux_clk high to aux_adr, aux_data15–0 (write), aux_oe valid†	1.3 V to 1.3 V		0		15	ns
t_{d6}	Delay time, aux_clk high to $\overline{\text{rom\_cs}}$, $\overline{\text{ram\_cs}}$, $\overline{\text{aux\_cs}}$ valid	1.3 V to 1.3 V		0		20	ns
t_{d7}	Delay time, $\overline{\text{aux\_we0}}$, $\overline{\text{aux\_we1}}$ high (deasserted) to aux_adr, aux_data15–0 (write), aux_oe, $\overline{\text{rom\_cs}}$, $\overline{\text{ram\_cs}}$, $\overline{\text{aux\_cs}}$ valid	1.3 V to 1.3 V		0.5			ns
t_{d8}	Delay time, aux_clk low to $\overline{\text{aux\_we0}}$, $\overline{\text{aux\_we1}}$ low (asserted)	1.3 V to 1.3 V		0		10	ns
t_{d9}	Delay time, aux_clk high to $\overline{\text{aux\_we0}}$, $\overline{\text{aux\_we1}}$ high (deasserted)	1.3 V to 1.3 V		0		10	ns
t_{d10}	Delay time, aux_clk high to gpio_data3–0 valid	1.3 V to 1.3 V		2		15	ns
t_{su5}	Setup time, aux_adr, adr_data15–0 (write), $\overline{\text{aux\_oe}}$, $\overline{\text{rom\_cs}}$, $\overline{\text{ram\_cs}}$, $\overline{\text{aux\_cs}}$ valid before $\overline{\text{aux\_we0}}$, $\overline{\text{aux\_we1}}$ low (asserted)	1.3 V to 1.3 V		5			ns
t_{su6}	Setup time, aux_data15–0 (read), $\overline{\text{aux\_rdy}}$, gpio_data3–0 valid before aux_clk high	1.3 V to 1.3 V		10			ns
t_{h3}	Hold time, aux_data15–0 (read), $\overline{\text{aux\_rdy}}$, gpio_data3–1 invalid after aux_clk high	1.3 V to 1.3 V		0			ns

† These signals are asserted asynchronously when a ZOOM port transfer imediately preceeds the local bus transfer. In all cases, the setup time to aux_we1 and aux_we0 and the number of waitstates remain the same.

zoom video port switching characteristics, source clock = 30 ns with a 50% duty cycle

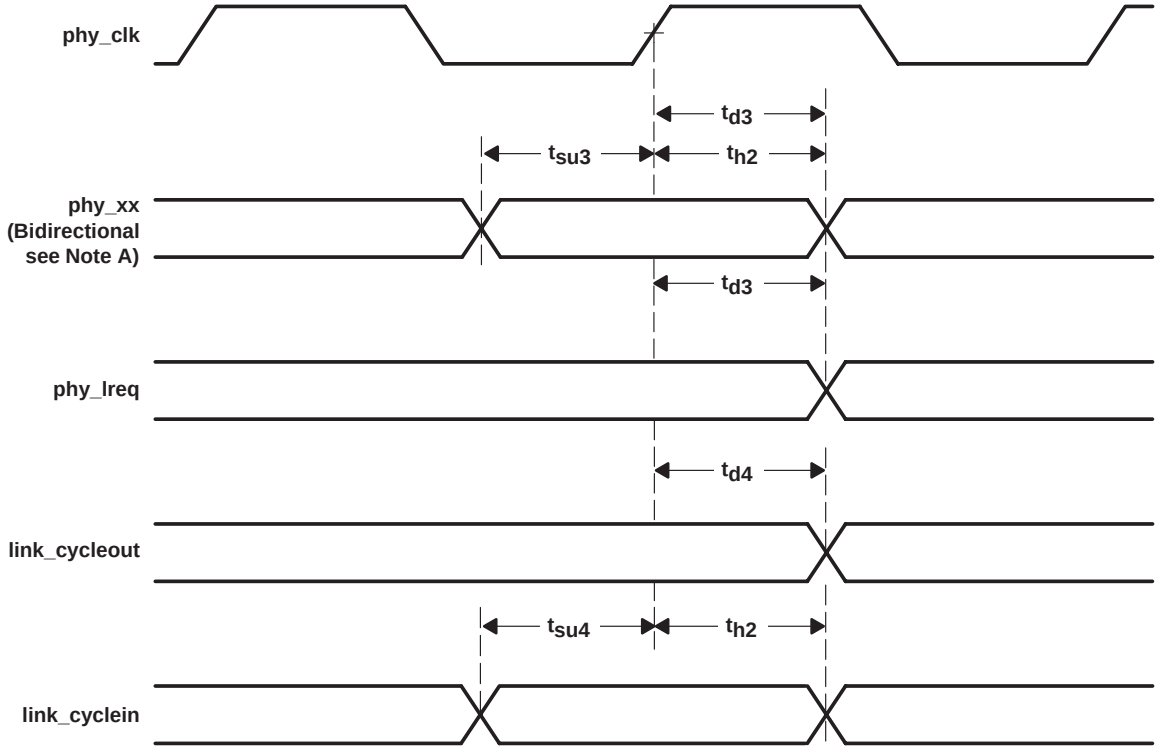
PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su7}	Setup time, zv_hsync low, zv_vsync, zv_data_valid high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 4	12			ns
t_{h4}	Hold time, zv_hsync high, zv_vsync, zv_data_valid low after zv_pix_clk low	1.3 V to 1.3 V	See Figure 4	14			ns
t_{su8}	Setup time, aux_data7–0 valid before zv_pix_clk high or low	1.3 V to 1.3 V	See Figure 4	10			ns
t_{h5}	Hold time, aux_data7–0 valid after zv_pix_clk high or low	1.3 V to 1.3 V	See Figure 4	14			ns
t_{d11}	Delay time, zv_hsync low, zv_vsync, zv_data_valid high after zv_pix_clk low	1.3 V to 1.3 V	See Figure 5	–1		3	ns
t_{d12}	Delay time, aux_data7–0 invalid after zv_pix_clk low	1.3 V to 1.3 V	See Figure 5	–1		5	ns
t_{su9}	Setup time, zv_hsync low before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	25			ns
t_{h6}	Hold time, zv_hsync high after zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	14			ns
t_{su10}	Setup time, zv_vsync high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	10			ns
t_{su11}	Setup time, aux_data7–0 valid, zv_data_valid high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	25			ns
t_{h7}	Hold time, aux_data7–0 valid, zv_data-valid low after zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	14			ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: In this case, pci_xx refers to the following bidirectional signals; pci_ad31–0, pci_cbe3–0, pci_par, pci_frame, pci_irdy, pci_trdy, pci_devsel, pci_stop, pci_idsel, pci_perr, pci_serr, pci_req.

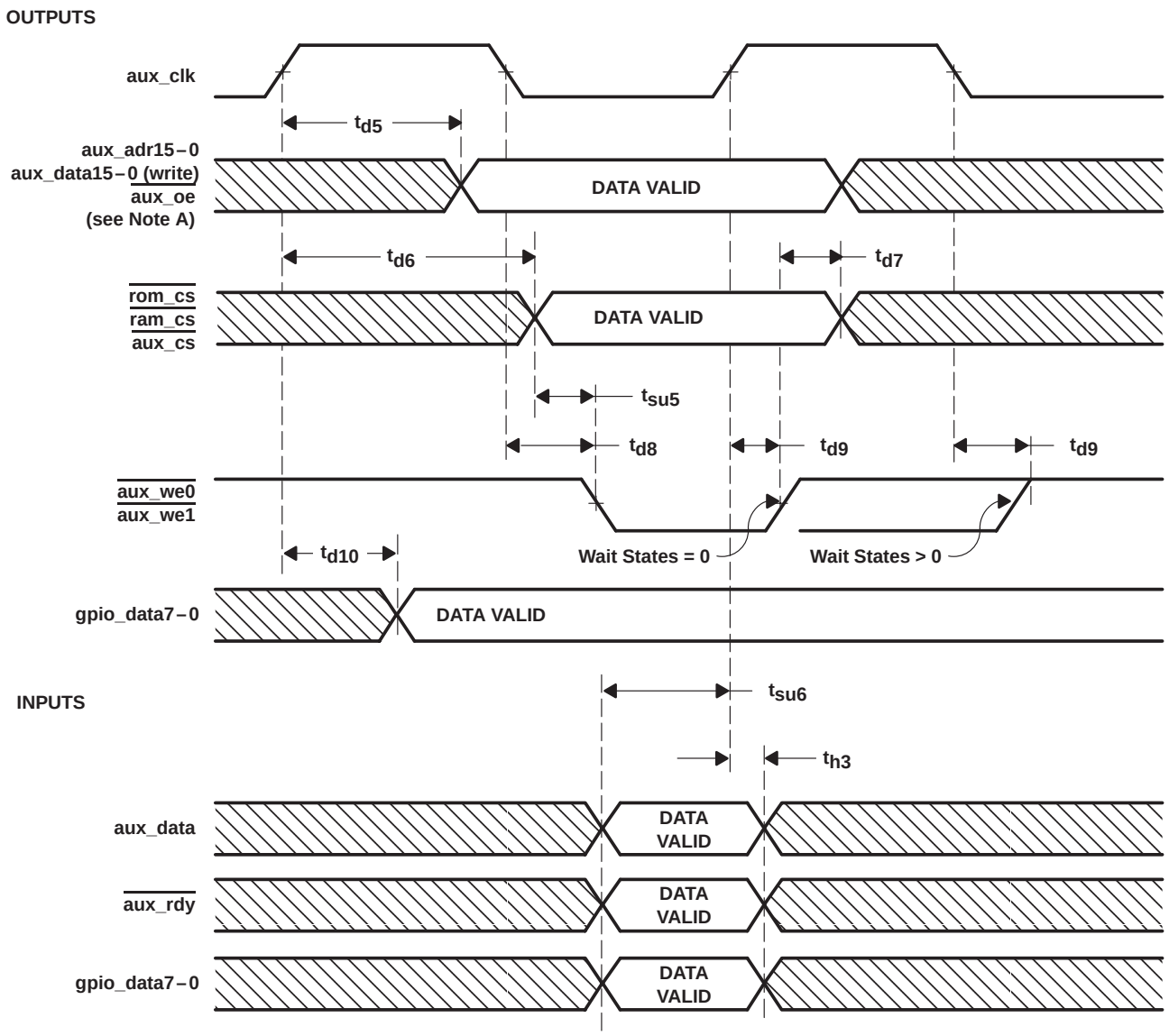
Figure 4. PCI Interface Timing Waveforms



NOTE A: In this case, phy_xx refers to the following bidirectional signals; phy_ctl1–0, phy_data7–0.

Figure 5. Phy-Link Interface Timing Waveforms

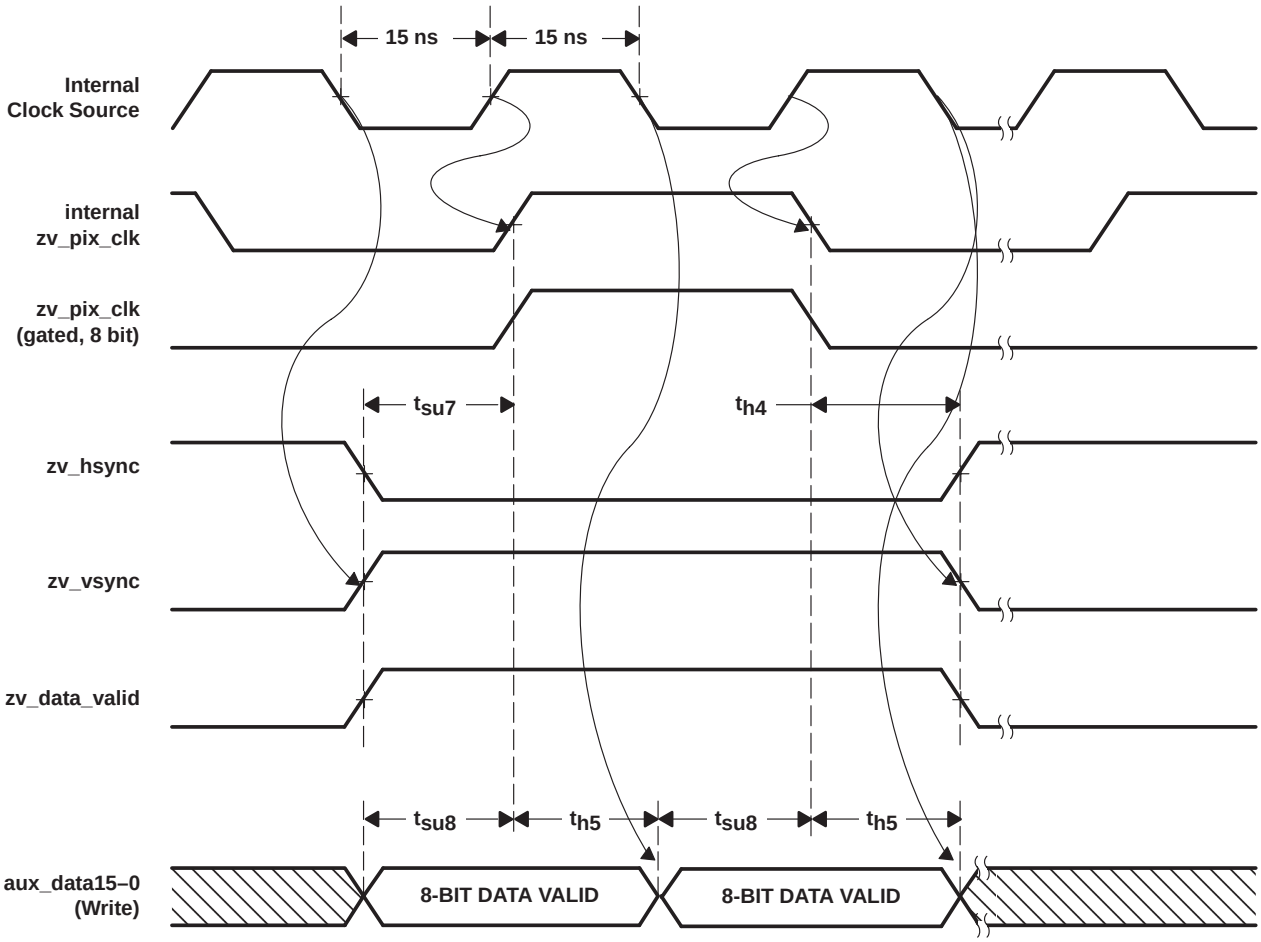
PARAMETER MEASUREMENT INFORMATION



NOTE A: These signals are asserted asynchronously when a ZOOM port transfer immediately preceeds the local bus transfer. In all cases, the setup time to aux_we and the number of wait states remains valid.

Figure 6. Local Bus Timing Waveforms

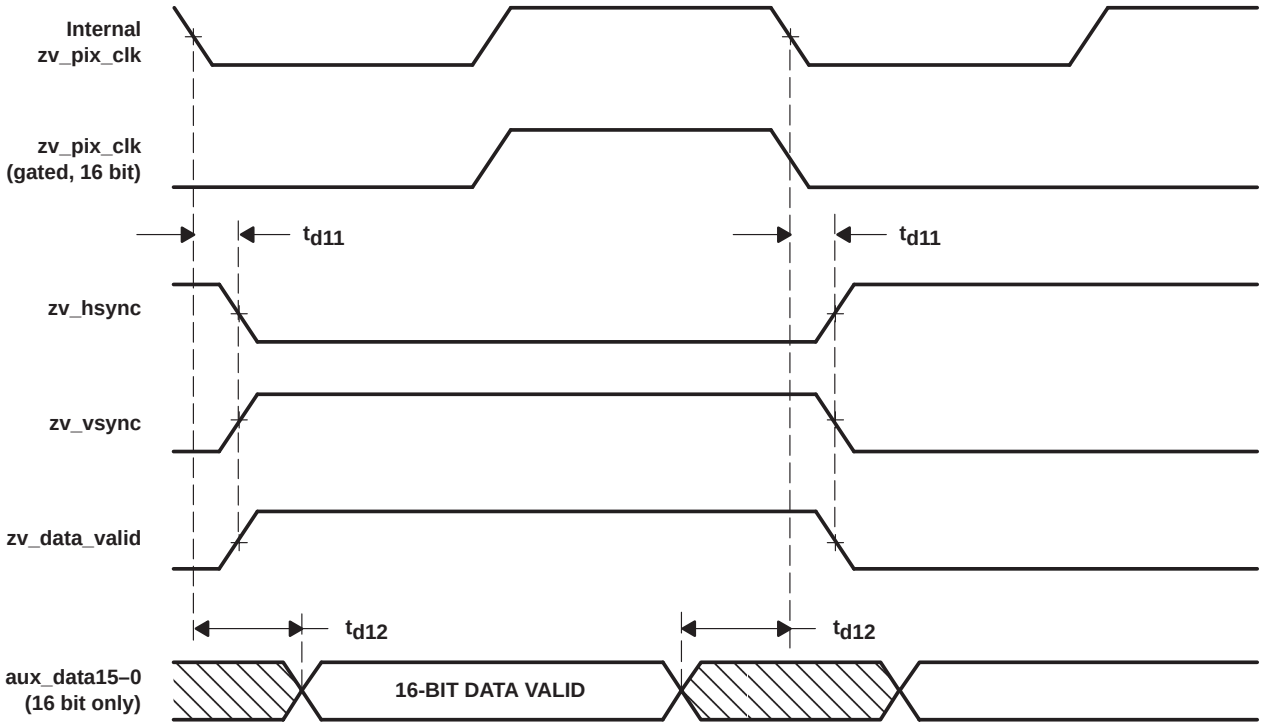
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 8-bit mode and zv_pix_clk is in divide-by-2 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk = 0.
E. The timing of these waveforms is with a 30-ns source clock and a 50/50 duty cycle.

Figure 7. Zoom Video IF Timing Waveforms (8 Bit, Divide-By-2 Mode)

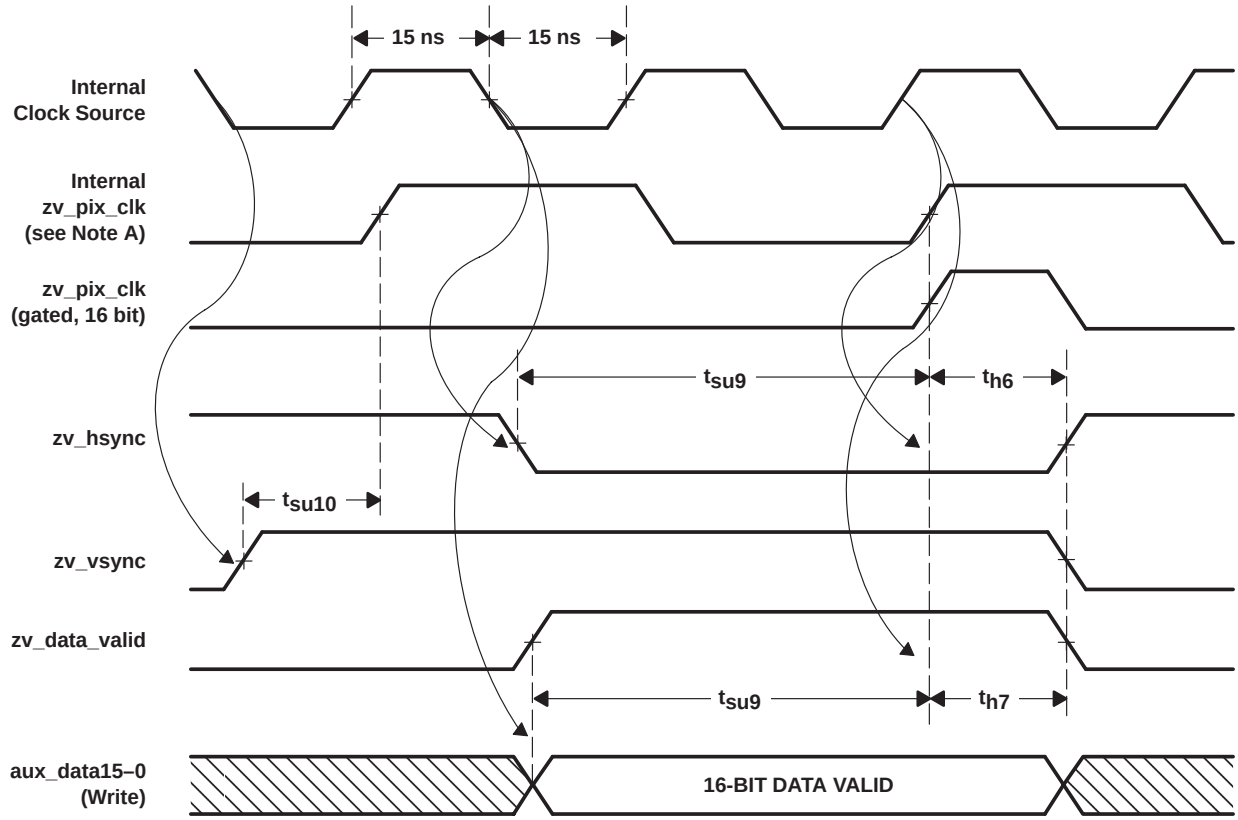
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 16-bit mode and zv_pix_clk is in divide-by-1 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk = 0.

Figure 8. Zoom Video IF Timing Waveforms (16 Bit, Divide-By-1 Mode)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 16-bit mode and zv_pix_clk is in divide-by-2 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk terminal. The polarity shown in this figure is with invert_zv_clk = 0.
E. The timing of these waveforms is with a 30-ns source clock and a 50/50 duty cycle.

Figure 9. Zoom Video IF Timing Waveforms (16 Bit, Divide-By-2 Mode)

APPLICATION INFORMATION

power supply sequencing

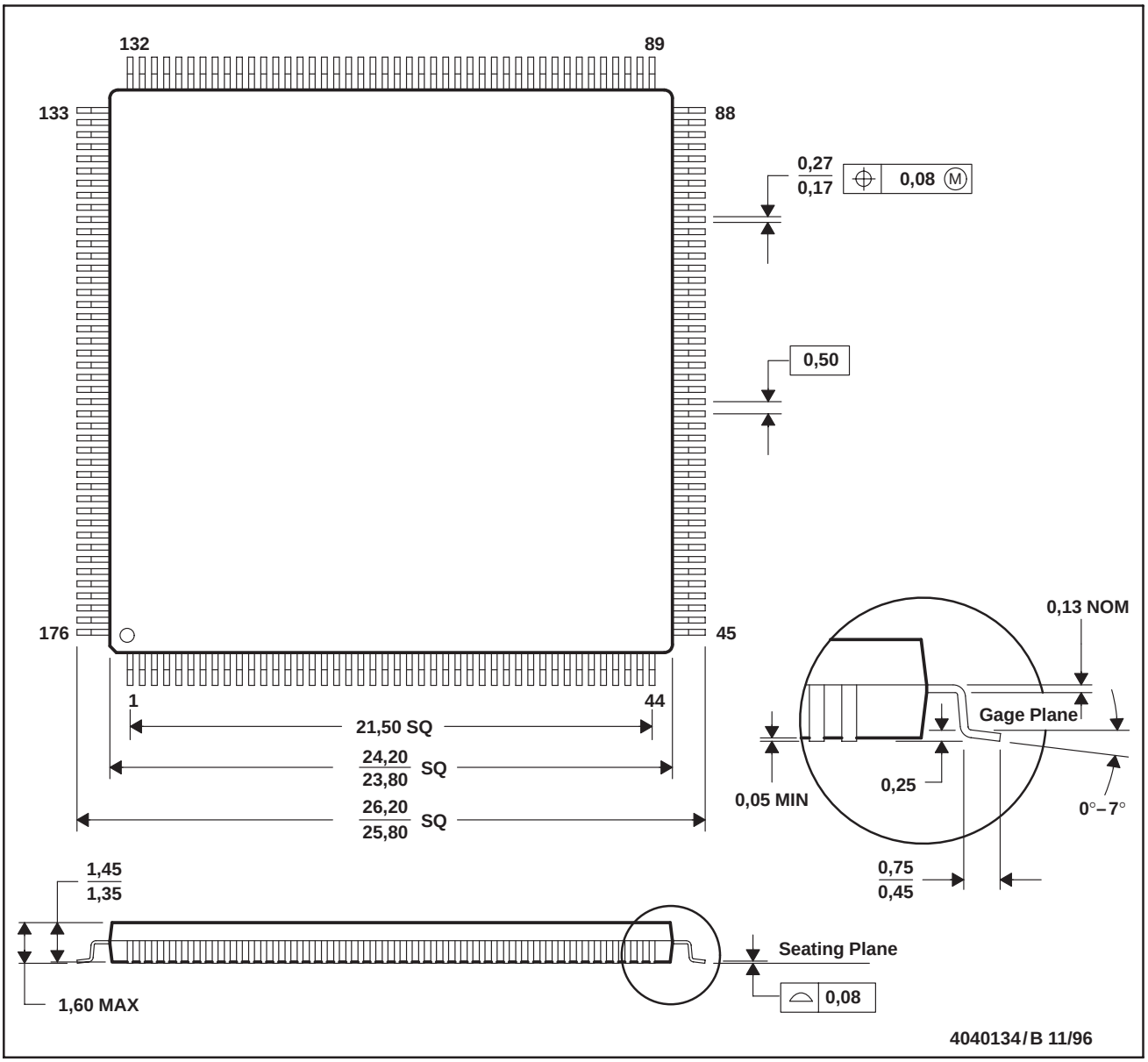
Turning power supplies on and off within a mixed 5-V/3.3-V system is an important consideration. A few basic rules need to be observed to avoid damaging PCILynx-2 devices. Check with the manufacturers of all components used in the 3.3-V to 5-V interface to ensure that no unique device characteristics exist that would lead to more restrictive rules.

- When the 3.3-V supply is turned on before turning on the 5-V supply, PCILynx-2 output buffers in a logic 1 state can supply large amounts of current through their clamp diodes to the 5-V supply terminals (5V V_{CC}). This can lead to excessive power dissipation and violation of current density limits. However, if the 5-V supply is turned on before the 3.3-V supply, the maximum drain-to-gate voltage of the n-channel transistors in the 5-V tolerant buffers exceeds the recommended value and the effects of channel-hot carries can be accelerated.
- When turning on the power supply, all 3.3-V and 5-V supplies should start ramping up from 0 V and reach 95% of their end-point values within a 25-ms time window. All bus contention between the PCILynx-2 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp the 3.3-V supply followed by the 5-V supply. This order is not mandatory, but it allows a larger cumulative number of power supply events than the reverse order.
- When turning off the power supply, all 3.3-V and 5-V supplies should start ramping down from steady state values and reach 5% of these values within a 25-ms window. All bus contention between the PCILynx–2 and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp down the 5-V supply followed by the 3.3-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply off events than the reverse order.
- A cumulative total of 250 seconds of power supply turnon and turnoff events is allowed during the operating lifetime of the PCILynx-2 under worst-case conditions. Worst-case conditions are where the 5-V supply is ramped up before the 3.3-V supply and the 3.3-V supply is ramped down before the 5-V supply. If the maximum time window of the 25 ms is used, a total of 10,000 power supply on or off events can occur as long as the 25-ms time window is observed.
- An additional precaution must be observed when the PCILynx–2 is connected to a 5-V IEEE 1394 physical-layer device that is powered from the 1394 cable. In this case, it is possible for the physical-layer device to have power while the PCILynx–2 does not. It is essential that the physical-layer device must not supply a high signal on any terminal that connects to the PCILynx–2 while the PCILynx-2 power is off. This is normally achieved through the use of the link-power status terminal on the physical-layer device.

If any of these precautions and guidelines are not followed, the PCILynx-2 device can experience possible failures related to overheating, accumulation of channel-hot carriers, and/or metal migration due to excessive current density.

MECHANICAL INFORMATION

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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