

- 28:4 Data Channel Compression at up to 227.5 Million Bytes per Second Throughput
- Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI
- 28 Data Channels and Clock In Low-Voltage TTL
- 4 Data Channels and Clock-Out Low-Voltage Differential
- Operates From a Single 3.3-V Supply With 250 mW (Typ)
- 5-V Tolerant Data Inputs
- Falling Clock-Edge-Triggered Inputs
- Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch
- Consumes Less Than 1 mW When Disabled
- Wide Phase-Lock Input Frequency Range . . . 31 MHz to 68 MHz
- No External Components Required for PLL
- Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Improved Replacement for the National DS90C581

description

The SN75LVDS81 FlatLink transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential-signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82. The SN75LVDS81 can also be used in 21-bit links with the SN75LVDS86 receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the falling edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times (7×) and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN75LVDS81 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on $\overline{\text{SHTDN}}$ clears all internal registers to a low level.

The SN75LVDS81 is characterized for operation over free-air temperature ranges of 0°C to 70°C.

DGG PACKAGE (TOP VIEW)

V _{CC}	1	56	D4
D5	2	55	D3
D6	3	54	D2
D7	4	53	GND
GND	5	52	D1
D8	6	51	D0
D9	7	50	D27
D10	8	49	LVDSGND
V _{CC}	9	48	Y0M
D11	10	47	Y0P
D12	11	46	Y1M
D13	12	45	Y1P
GND	13	44	LVDSV _{CC}
D14	14	43	LVDSGND
D15	15	42	Y2M
D16	16	41	Y2P
NC	17	40	CLKOUTM
D17	18	39	CLKOUTP
D18	19	38	Y3M
D19	20	37	Y3P
GND	21	36	LVDSGND
D20	22	35	PLL _{GND}
D21	23	34	PLL _{V_{CC}}
D22	24	33	PLL _{GND}
D23	25	32	$\overline{\text{SHTDN}}$
V _{CC}	26	31	CLKIN
D24	27	30	D26
D25	28	29	GND

NC – Not Connected



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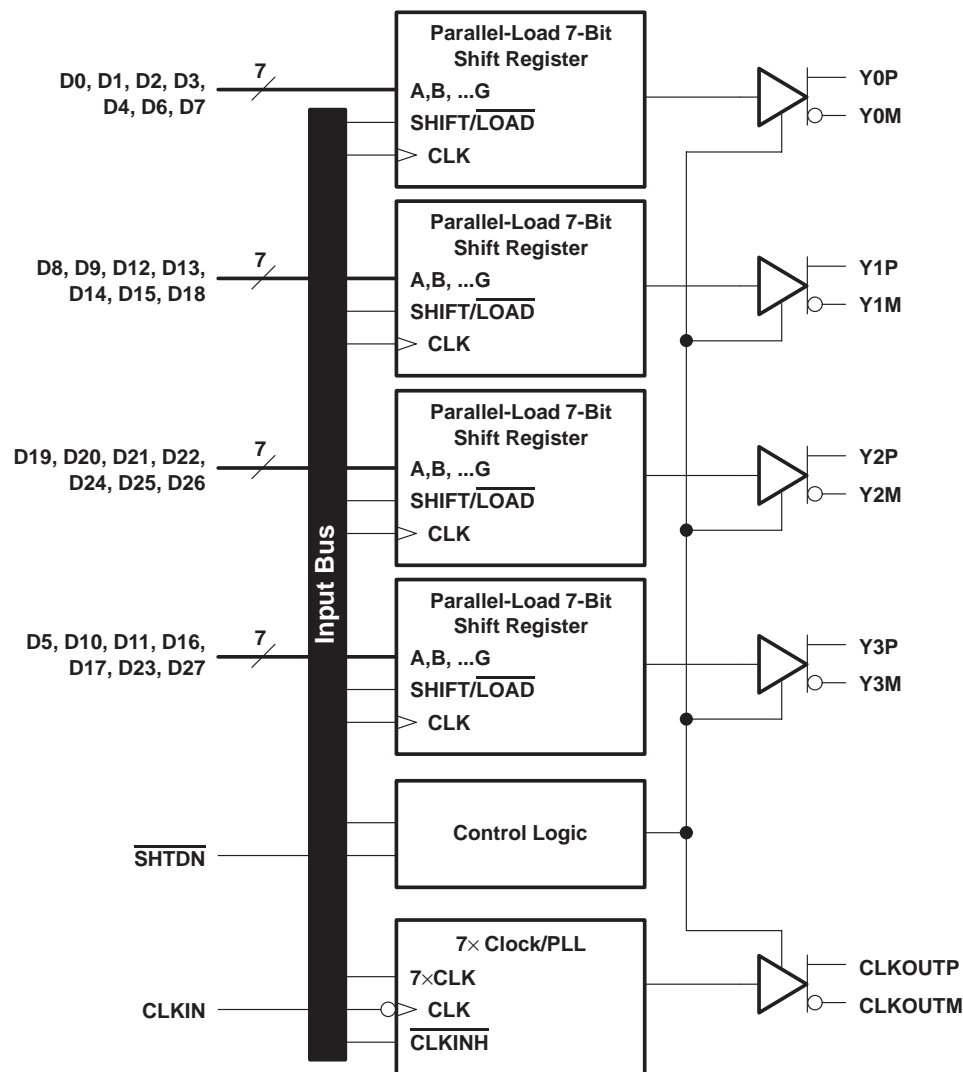
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functional block diagram



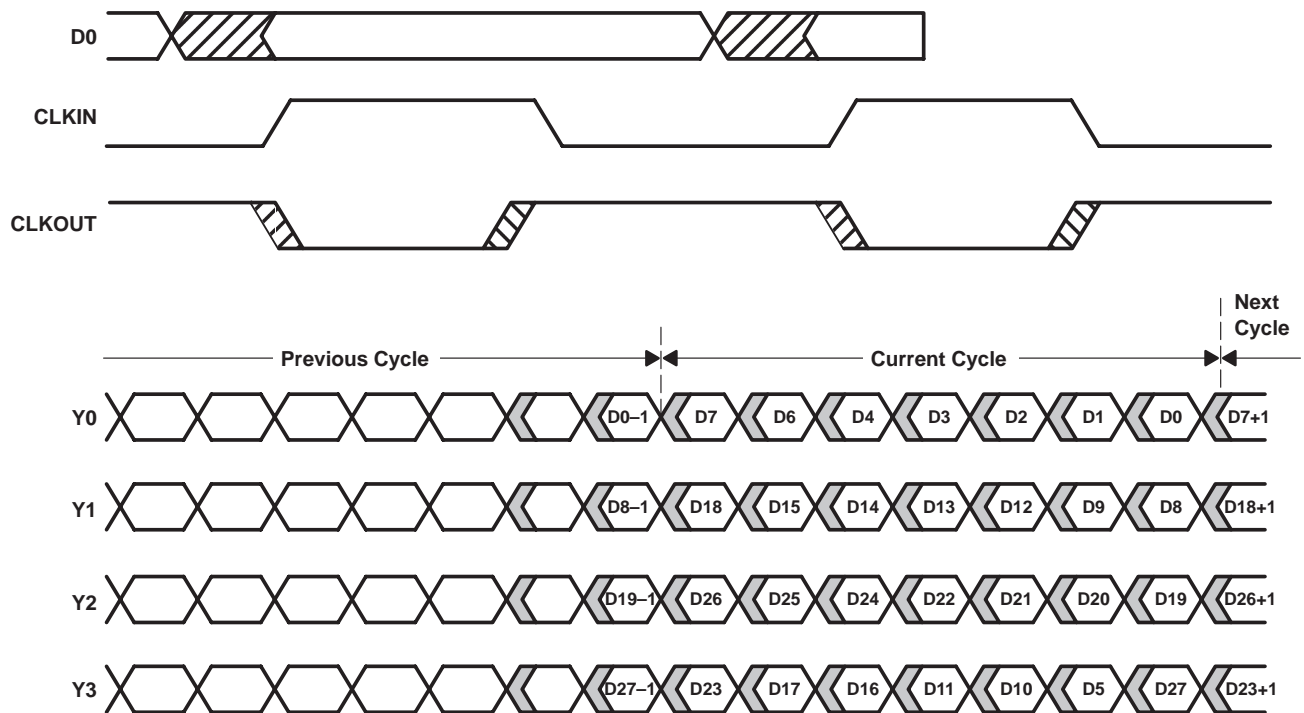
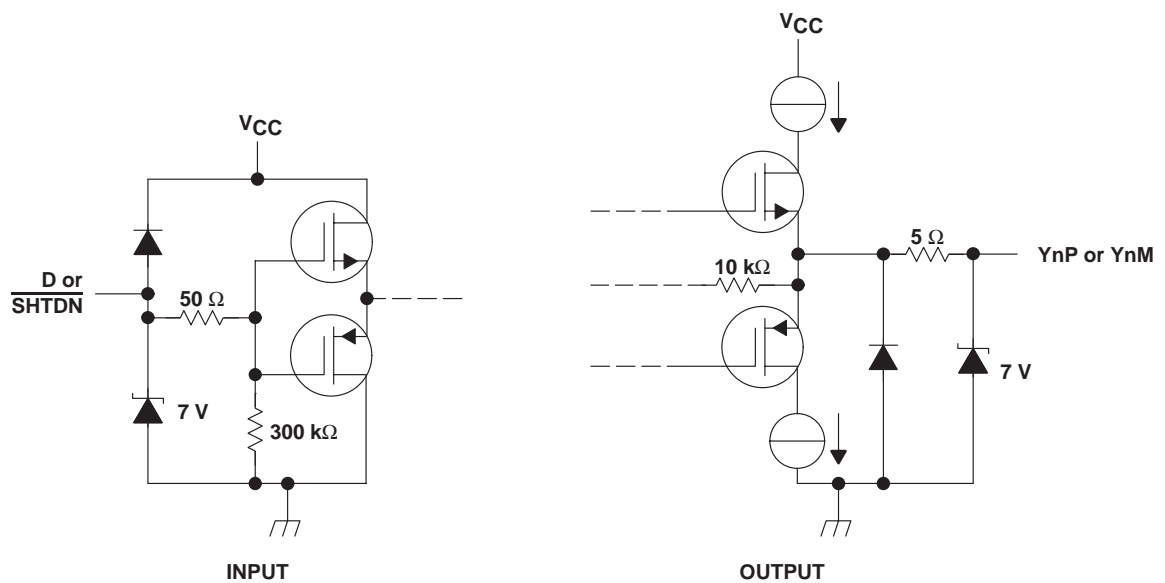


Figure 1. SN75LVDS81 Load and Shift Timing Sequences

equivalent input and output schematic diagrams



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 4 V
Output voltage range, V_O (all terminals)	–0.3 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (all terminals)	–0.5 V to 5.5 V
Continuous total power dissipation	see Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DGG	1377 mW	11.0 mW/°C	882 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Differential load impedance, Z_L	90		132	Ω
Operating free-air temperature, T_A	0		70	°C

timing requirements

		MIN	NOM	MAX	UNIT
t_C	Input clock cycle time	14.7		32.4	ns
t_W	High-level input clock pulse width duration	$0.4t_C$		$0.6t_C$	ns
t_t	Input signal transition time			5	ns
t_{su}	Data setup time, D0 – D27 before CLKIN↓	See Figure 2	3		ns
t_h	Data hold time, D0 – D27 valid after CLKIN↓	See Figure 2	1.5		ns



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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT}	Input threshold voltage			1.4		V
$ V_{OD} $	Differential steady-state output voltage magnitude	$R_L = 100\ \Omega$, See Figure 3	247		454	mV
$\Delta V_{OD} $	Change in the steady-state differential output voltage magnitude between opposite binary states				50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			20	μA
I_{IL}	Low-level input current	$V_{IL} = 0$			± 10	μA
I_{OS}	Short-circuit output current	$V_{O(Yn)} = 0$			± 24	mA
		$V_{OD} = 0$			± 12	mA
I_{OZ}	High-impedance state output current	$V_O = 0$ to V_{CC}			± 10	μA
I_{CC}	Quiescent supply current	Disabled, All inputs at GND			280	μA
		Enabled, $R_L = 100\ \Omega$, Gray-scale pattern (see Figure 4), $V_{CC} = 3.3\ V$, $t_C = 15.28\ ns$		72	80	mA
		Enabled, $R_L = 100\ \Omega$, Worst-case pattern (see Figure 5), $t_C = 15.28\ ns$		85	110	mA
C_I	Input capacitance			3		pF

† All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25^\circ C$.

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switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_0 Delay time, CLKOUT↑ after Yn valid (serial bit position 0)	$t_C = 15.38 \text{ ns } (\pm 0.2\%),$ Input clock jitter < 50 ps‡, See Figure 6	-0.2	0	0.2	ns
t_1 Delay time, CLKOUT↑ after Yn valid (serial bit position 1)		$\frac{1}{7}t_C - 0.2$	$\frac{1}{7}t_C$	$\frac{1}{7}t_C + 0.2$	ns
t_2 Delay time, CLKOUT↑ after Yn valid (serial bit position 2)		$\frac{2}{7}t_C - 0.2$	$\frac{2}{7}t_C$	$\frac{2}{7}t_C + 0.2$	ns
t_3 Delay time, CLKOUT↑ after Yn valid (serial bit position 3)		$\frac{3}{7}t_C - 0.2$	$\frac{3}{7}t_C$	$\frac{3}{7}t_C + 0.2$	ns
t_4 Delay time, CLKOUT↑ after Yn valid (serial bit position 4)		$\frac{4}{7}t_C - 0.2$	$\frac{4}{7}t_C$	$\frac{4}{7}t_C + 0.2$	ns
t_5 Delay time, CLKOUT↑ after Yn valid (serial bit position 5)		$\frac{5}{7}t_C - 0.2$	$\frac{5}{7}t_C$	$\frac{5}{7}t_C + 0.2$	ns
t_6 Delay time, CLKOUT↑ after Yn valid (serial bit position 6)		$\frac{6}{7}t_C - 0.2$	$\frac{6}{7}t_C$	$\frac{6}{7}t_C + 0.2$	ns
$t_{sk(o)}$ Output skew, $t_n - \frac{n}{7}t_C$		-0.2		0.2	ns
t_7 Delay time, CLKIN↓ to CLKOUT↓	$t_C = 15.38 \text{ ns } (\pm 0.2\%),$ Input clock jitter < 50 ps‡, See Figure 6		4.2		ns
$\Delta t_{C(o)}$ Output clock jitter§	$t_C = 15.38 \pm 0.75 \sin(2\pi 500E3t) + 0.05 \text{ ns},$ See Figure 7		±80		ps
	$t_C = 15.38 \pm 0.75 \sin(2\pi 3E6t) + 0.05 \text{ ns},$ See Figure 7		±300		ps
t_W High-level output clock pulse duration			$0.57 t_C$		ns
t_t Differential output transition time (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en} Enable time, $\overline{\text{SHTDN}}$ ↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis} Disable time, $\overline{\text{SHTDN}}$ ↓ to off state (CLKOUT low)	See Figure 9		250		ns

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

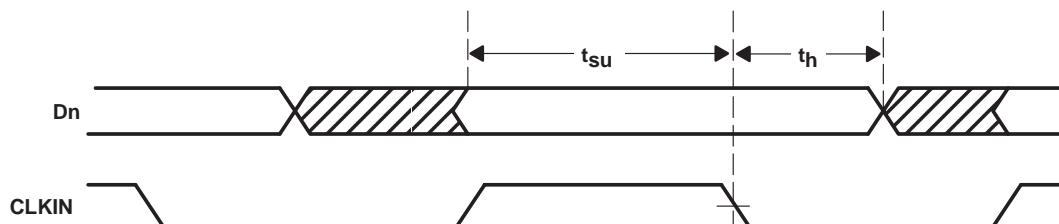
‡ |Input clock jitter| is the magnitude of the change in the input clock period.

§ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15 000 cycles.



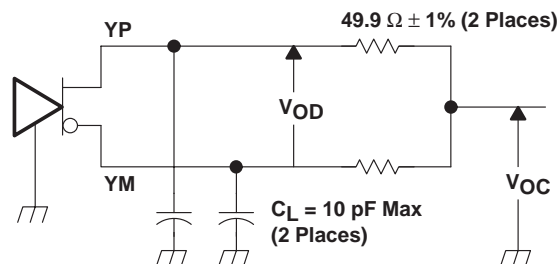
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PARAMETER MEASUREMENT INFORMATION



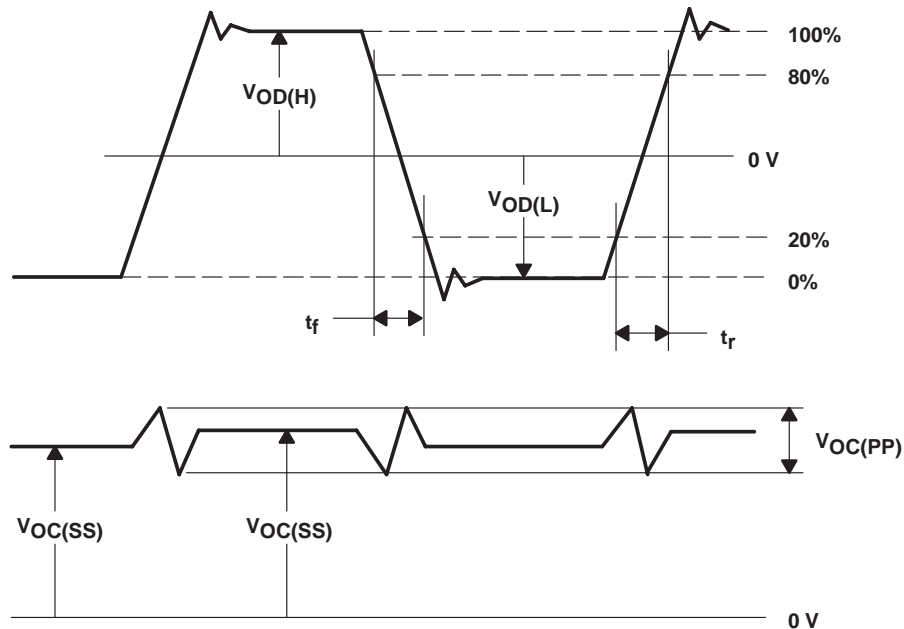
NOTE A: All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Waveforms



NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output will be similarly loaded.

a. SCHEMATIC



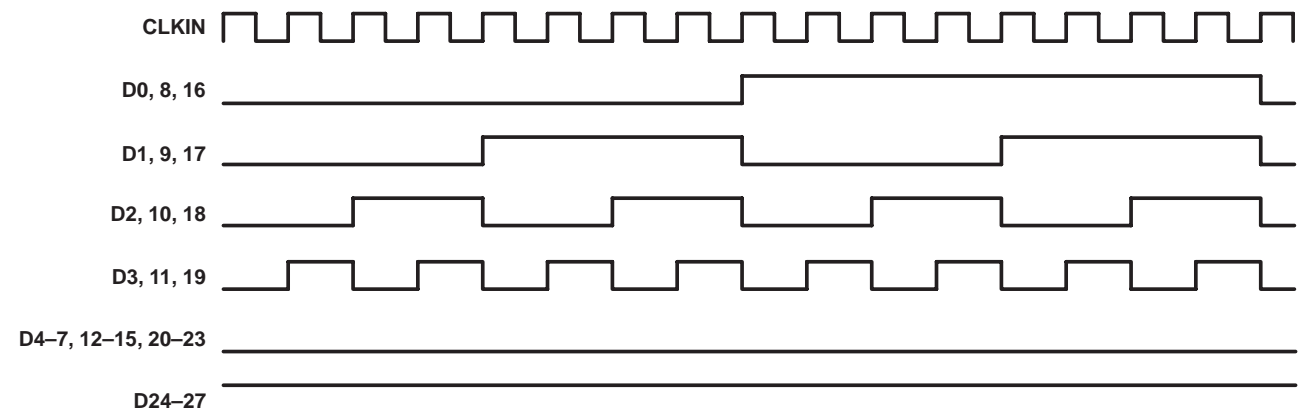
b. WAVEFORMS

Figure 3. Test Load and Voltage Waveforms for LVDS Outputs

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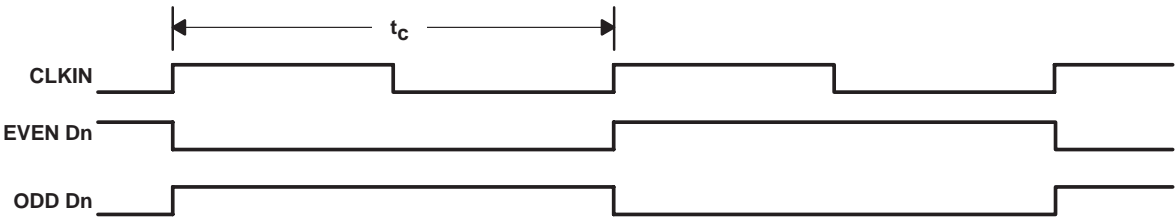
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PARAMETER MEASUREMENT INFORMATION



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 4. 16-Grayscale Test-Pattern Waveforms



NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

Figure 5. Worst-Case Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION

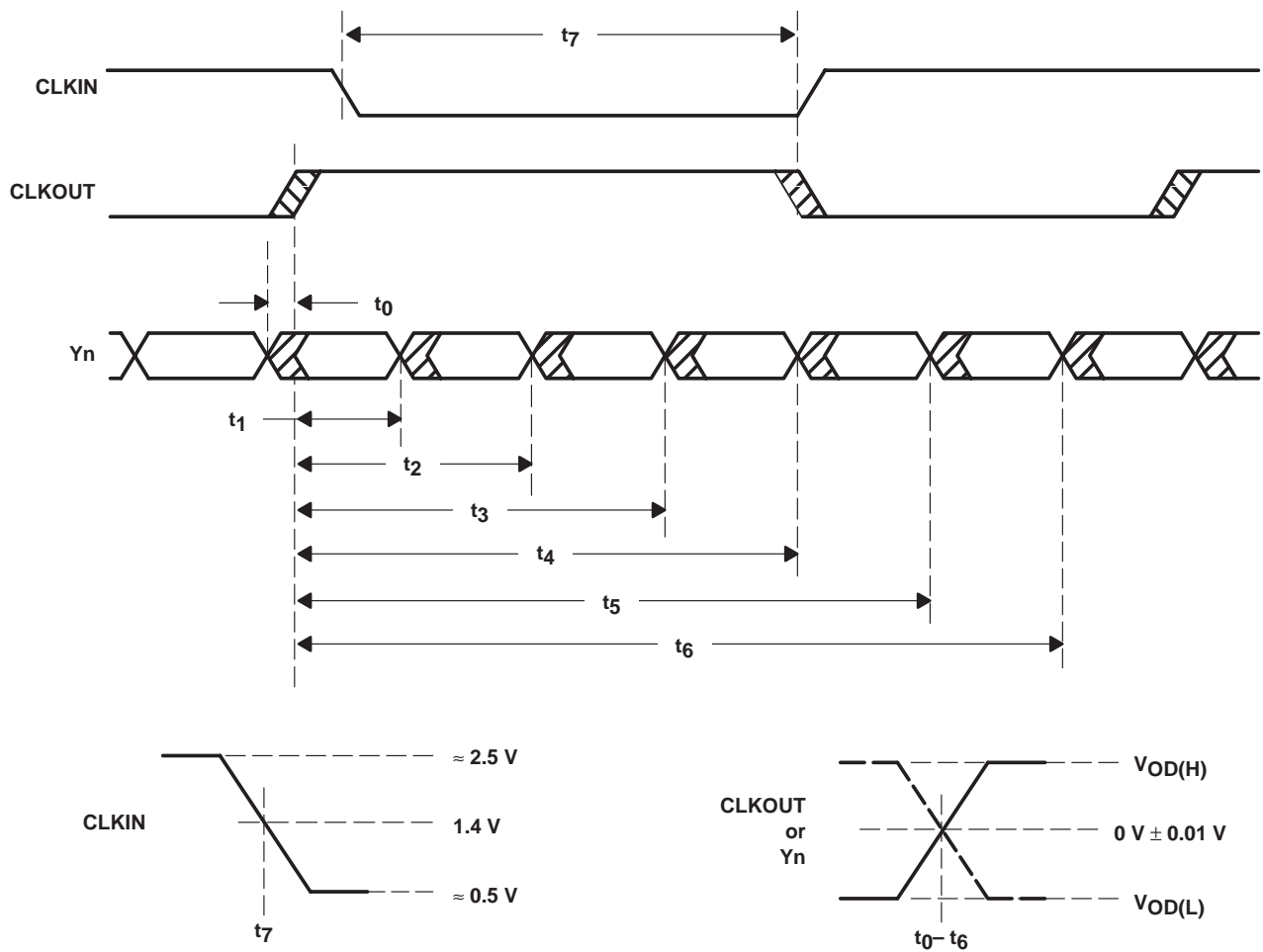


Figure 6. SN75LVDS81 Timing Waveforms

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PARAMETER MEASUREMENT INFORMATION

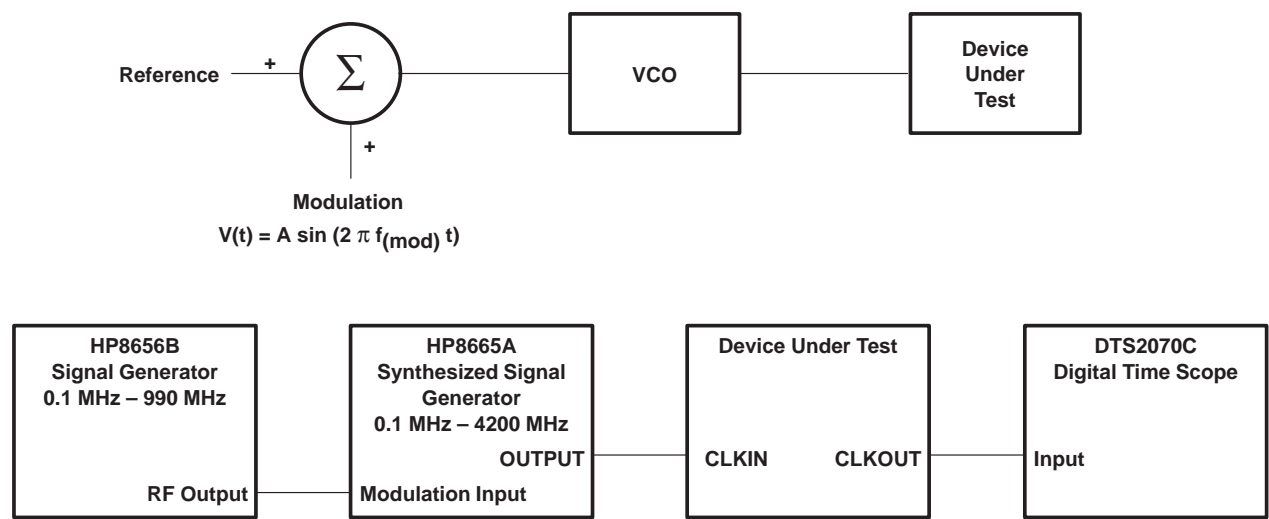


Figure 7. Output Clock Jitter Testing

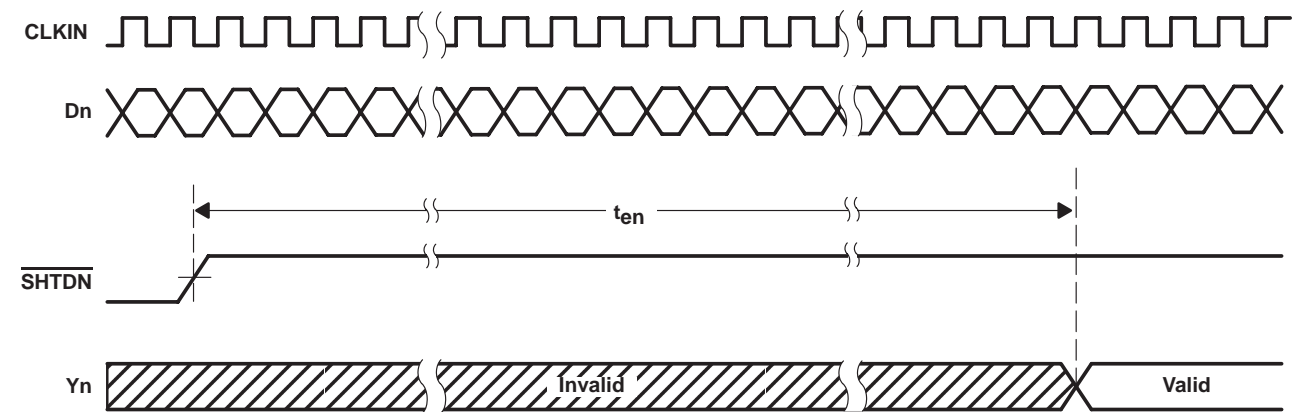


Figure 8. Enable Time Waveforms

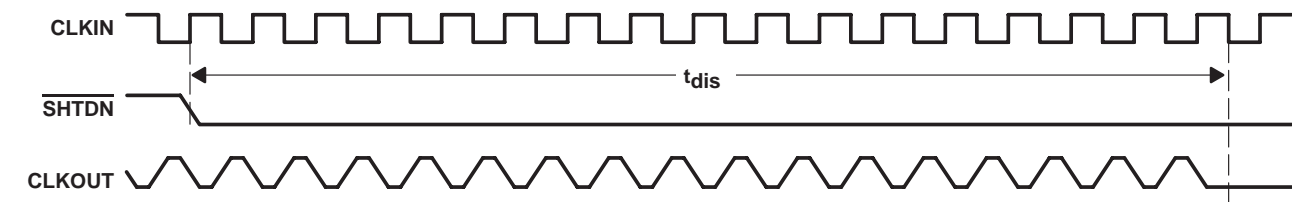


Figure 9. Disable Time Waveforms

TYPICAL CHARACTERISTICS

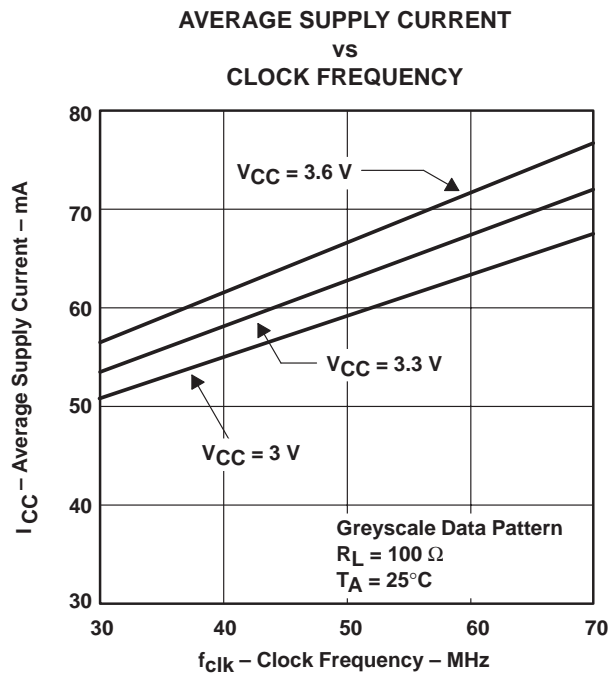


Figure 10

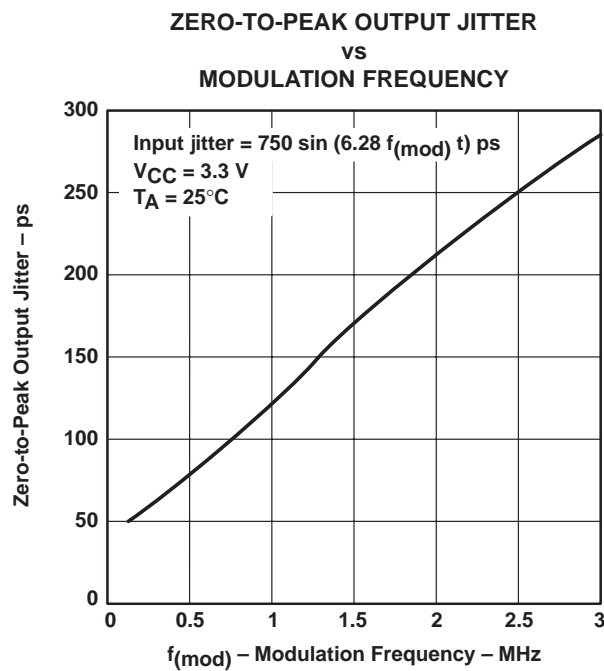


Figure 11

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APPLICATION INFORMATION

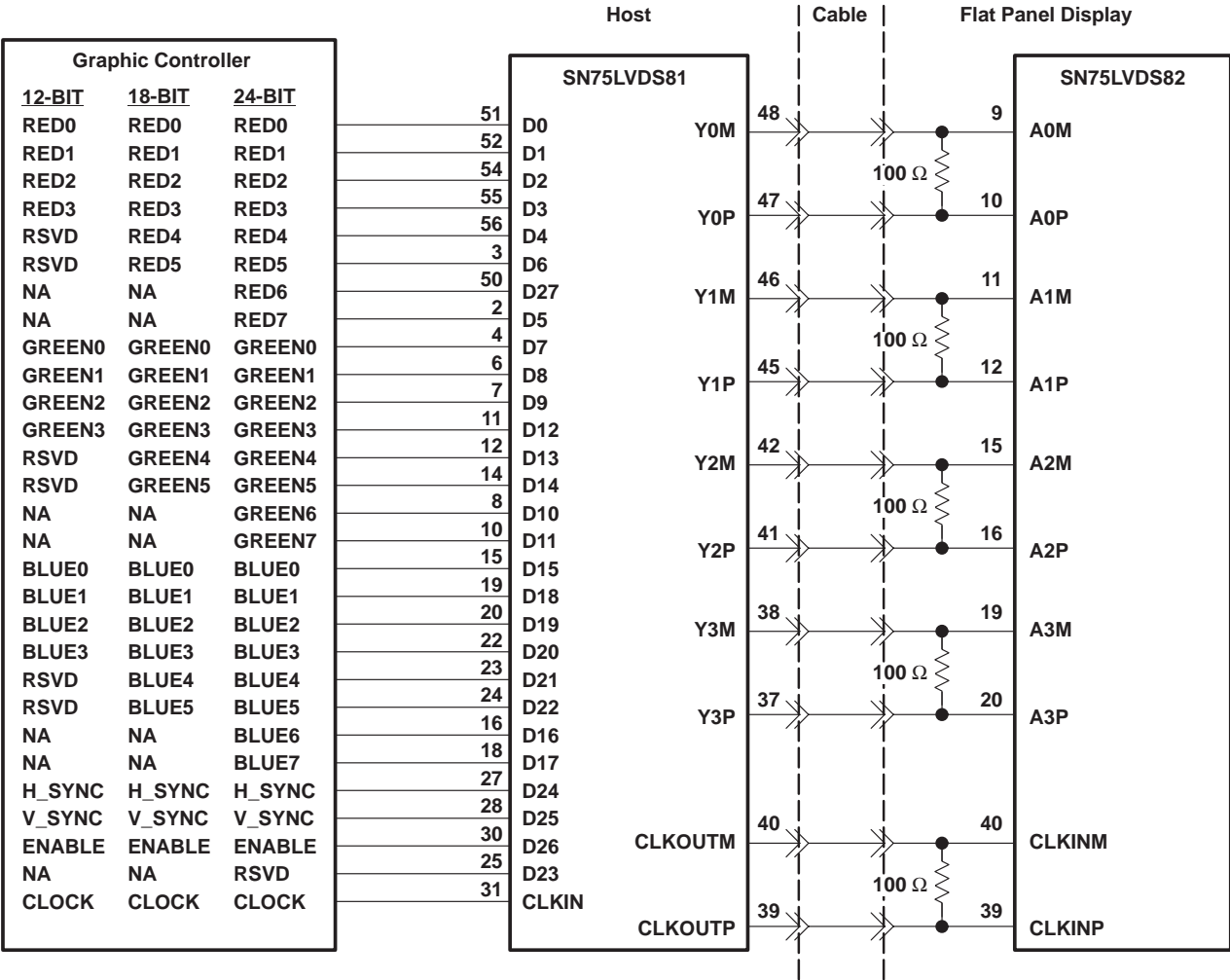
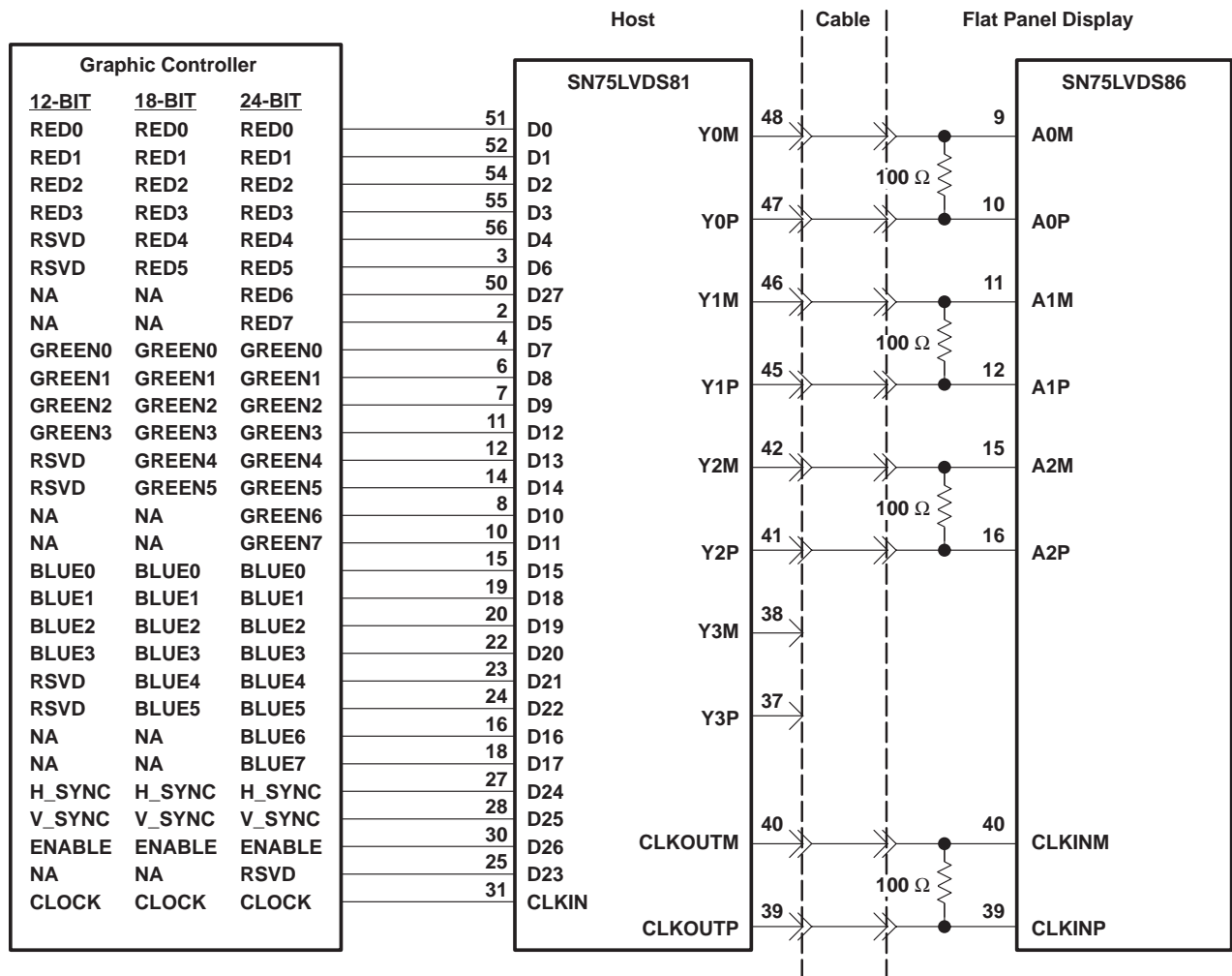


Figure 12. 24-Bit Color Host To 24-Bit LCD Panel Display Application

APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA – not applicable, these unused inputs should be left open.

Figure 13. 24-Bit Color Host To 18-Bit LCD Panel Display Application

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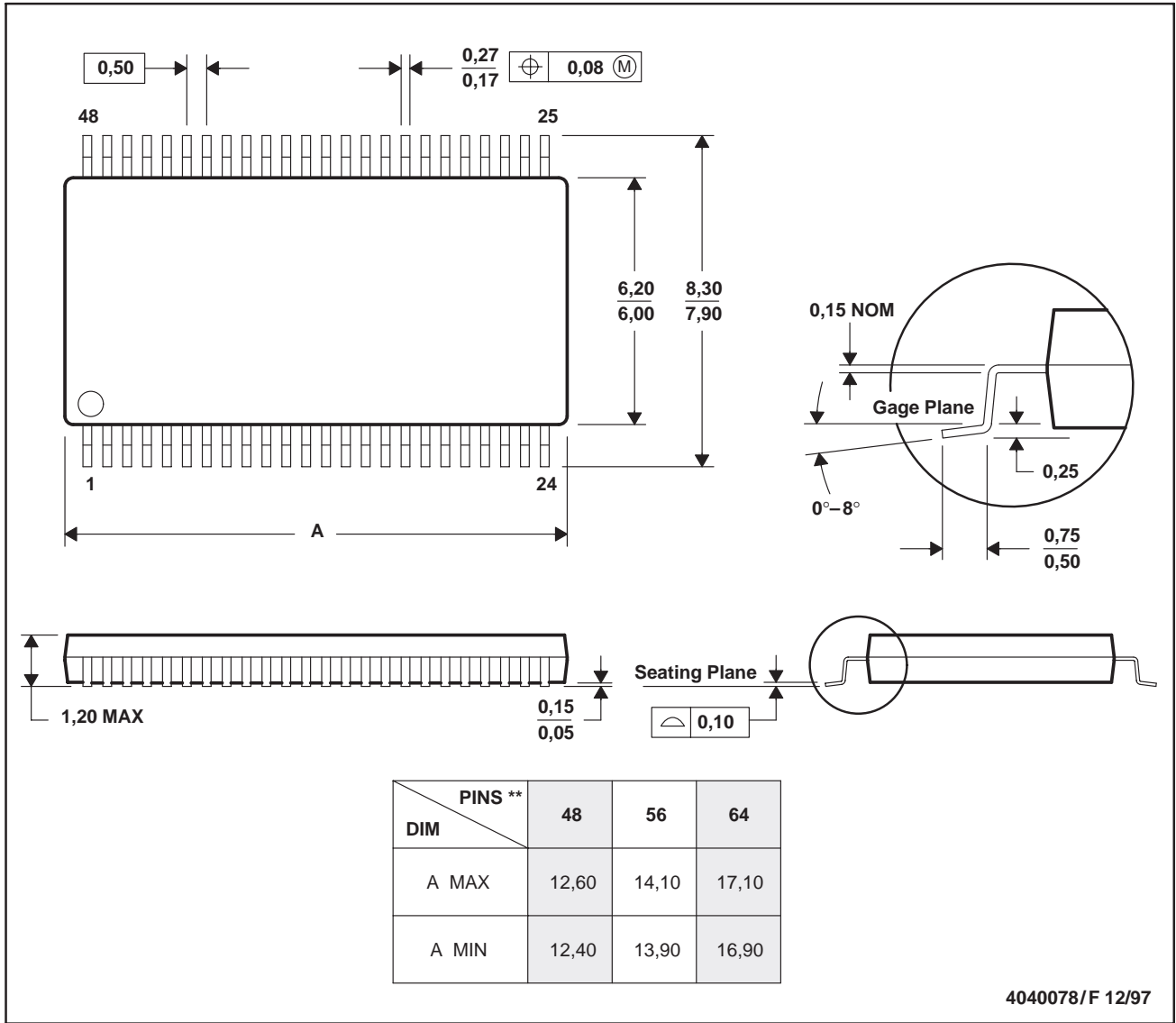
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MECHANICAL INFORMATION

DGG (R-PDSO-G**)

48 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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