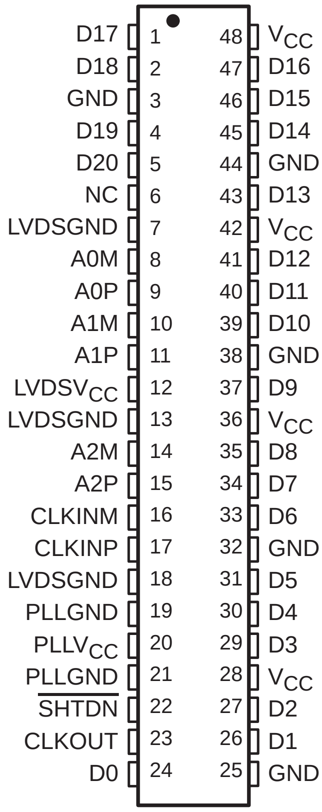
- **3:21 Data Channel Expansion at up to 1.3 Gigabits per Second Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **3 Data Channels and Clock Low-Voltage Differential Channels in and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{SHTDN}$ Input**
- **Rising Clock Edge Triggered Outputs**
- **Bus Pins Tolerate 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 67 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified $T_A = -40°C$ to 85°C**
- **Replacement for the DS90CR216**

DGG PACKAGE (TOP VIEW)



description

The SN65LVDS96 LVDS serdes (serializer/deserializer) receiver contains three serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN65LVDS95, over four balanced-pair conductors and expansion to 21 bits of single-ended LVTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate of seven times the LVDS input clock (CLKIN). The data is then unloaded to a 21-bit wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN65LVDS96 presents valid data on the rising edge of the output clock (CLKOUT).

The SN65LVDS96 requires only four line termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{SHTDN}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS96 is characterized for operation over ambient air temperatures of –40°C to 85°C.

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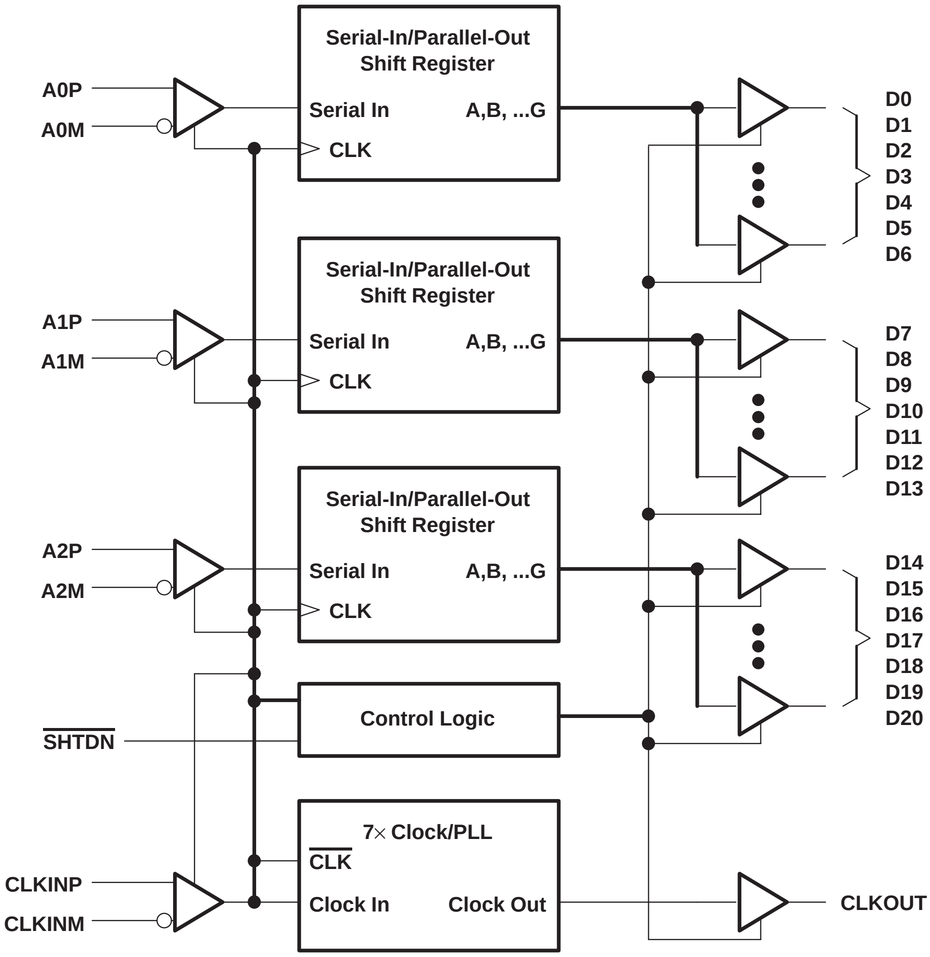
functional block diagram



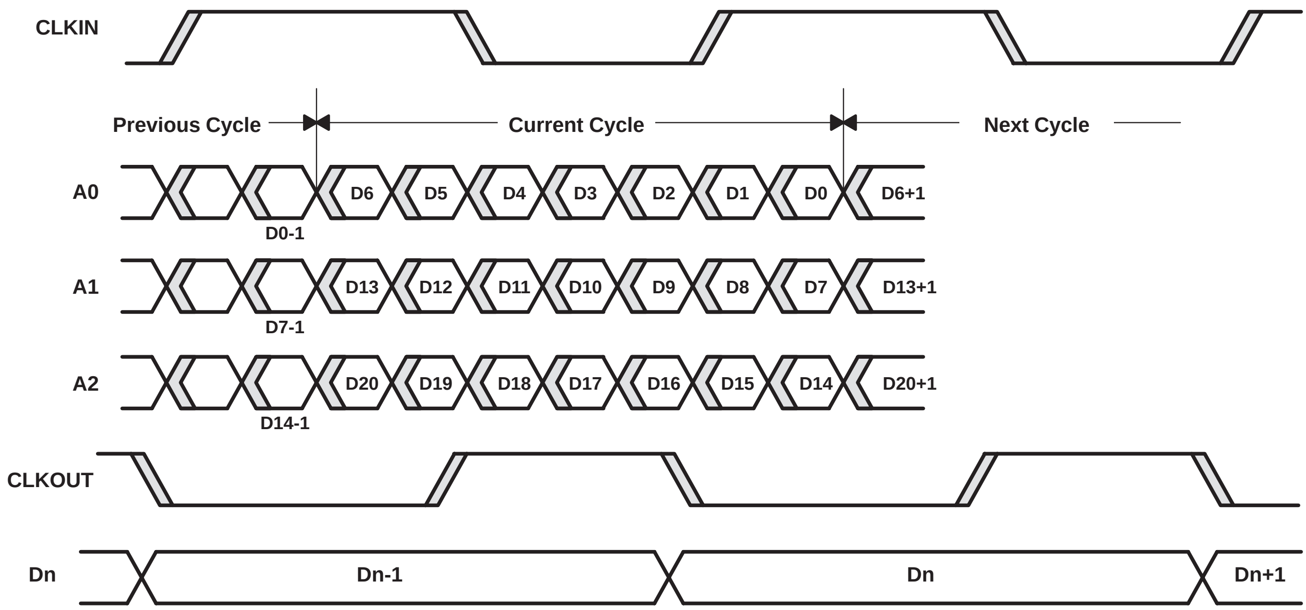
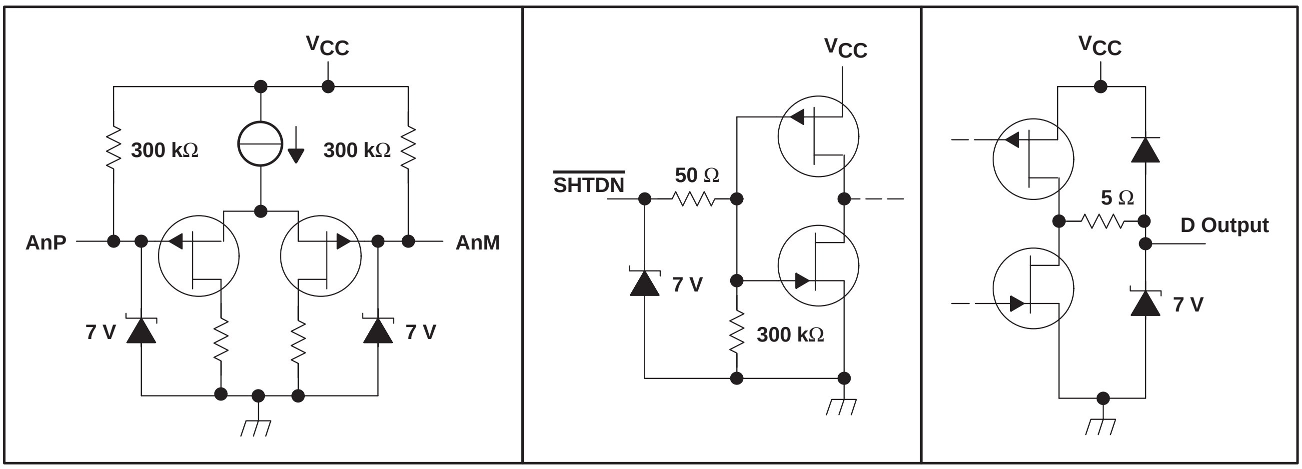


Figure 1. Typical ’LVDS96 Load and Shift Sequences

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Voltage range at any terminal (except $\overline{SHTDN}$) . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range at $\overline{SHTDN}$ terminal . . . . –0.5 V to 5.5 V
Electrostatic discharge (see Note 2): Bus pins (Class 3A) . . . . 4 KV
Bus pins (Class 2B) . . . . 200 V
All pins (Class 3A) . . . . 3 KV
All pins (Class 2B) . . . . 200 V
Continuous total power dissipation . . . . (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals unless otherwise noted.
2. This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGG	1316 mW	13.1 mW/°C	724 mW	526 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	$\overline{SHTDN}$	2			V
Low-level input voltage, V_{IL}	$\overline{SHTDN}$			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID}\rvert$		0.1		0.6	V
Common-mode input voltage, V_{IC}		$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 \times \frac{\lvert V_{ID}\rvert}{2}$ V_{CC}–0.8	V
Operating free-air temperature, T_A		–40		85	°C

timing requirements

PARAMETERS		MIN	NOM	MAX	UNIT
t_c§	Input clock period	15.4	t_c	50	ns

§ t_c is defined as the mean duration of a minimum of 32,000 clock periods.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential Input voltage threshold				100	mV
V_{IT-}	Negative-going differential Input voltage threshold‡		–100			mV
V_{OH}	High-level output voltage	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OH} = 4 mA			0.4	V
I_{CC}	Quiescent current (average)	Disabled, all inputs open			280	µA
		Enabled, AnP at 1 V and AnM at 1.4 V, t_c = 15.38 ns		60	82	mA
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 4), t_c = 15.38 ns		94		mA
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0 V			±20	µA
I_{IN}	Input current (A inputs)	0 V ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impedance output current	V_O = 0 V to V_{CC}			±10	µA

† All typical values are V_{CC} = 3.3 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{su}	Data setup time, D0 through D20 to CLKOUT↑	C_L = 8 pF,	See Figure 5	4	6		ns
t_h	Data hold time, CLKOUT↑ to D0 through D20	C_L = 8 pF,	See Figure 5	4	6		ns
t_{RSKM}	Receiver input skew margin§ (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| <50 ps¶	T_A = 0°C to 85°C	490	800		ps
			T_A = –40°C to 0°C	350			ps
t_d	Delay time, input clock to output clock (see Figure 7)	t_c = 15.38 ns (±0.2%)			3.7		ns
$\Delta t_{C(O)}$	Change in output clock period from cycle to cycle#	t_c = 15.38 + 0.75 sin (2π500E3t) ±0.05 ns, See Figure 7			±80		ps
		t_c = 15.38 + 0.75 sin (2π3E6t) ±0.05 ns, See Figure 7			±300		ps
t_{en}	Enable time, $\overline{SHTDN}$ to phase lock	See Figure 8			1		ms
t_{dis}	Disable time, $\overline{SHTDN}$ to Off state	See FIgure 9			400		ns
t_t	Output transition time (10% to 90% t_r or t_f)	C_L = 8 pF			3		ns
t_w	Output clock pulse duration				0.43 t_c		ns

§ t_{RSKM} is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from

$$\frac{tc}{14} - 600 \text{ ps.}$$

¶ |Input clock jitter| is the magnitude of the change in the input clock period.
# $\Delta t_{C(O)}$ is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

PARAMETER MEASUREMENT INFORMATION

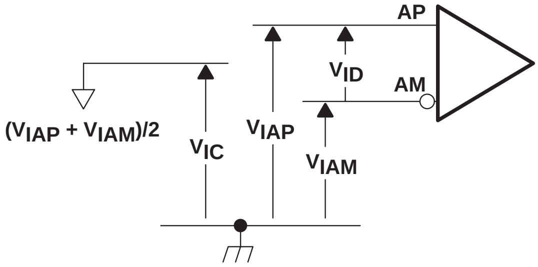


Figure 2. Voltage Definitions

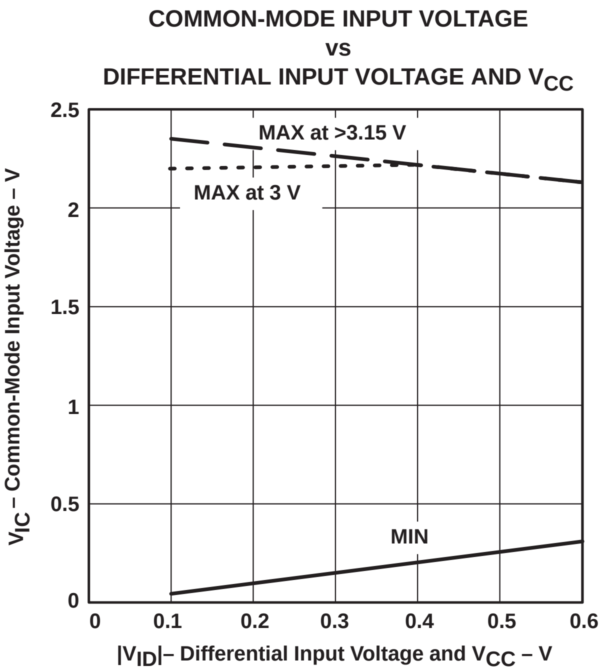


Figure 3. Maximum V_{IC} versus V_{ID} and V_{CC}

PARAMETER MEASUREMENT INFORMATION

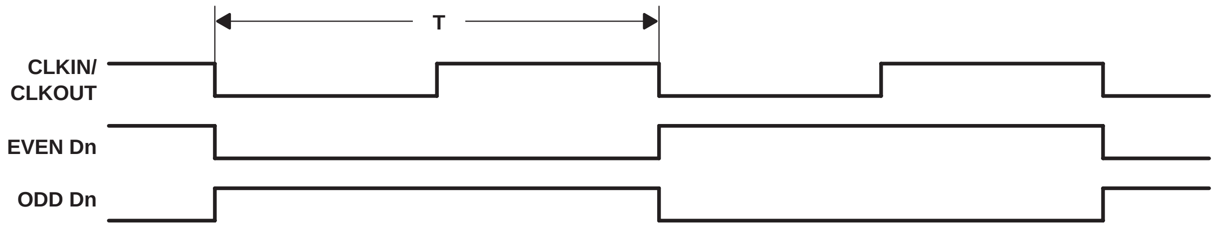


Figure 4. Worst-Case† Test Pattern

† The worst-case test pattern produces nearly the maximum switching frequency for all of the LV-TTL outputs.

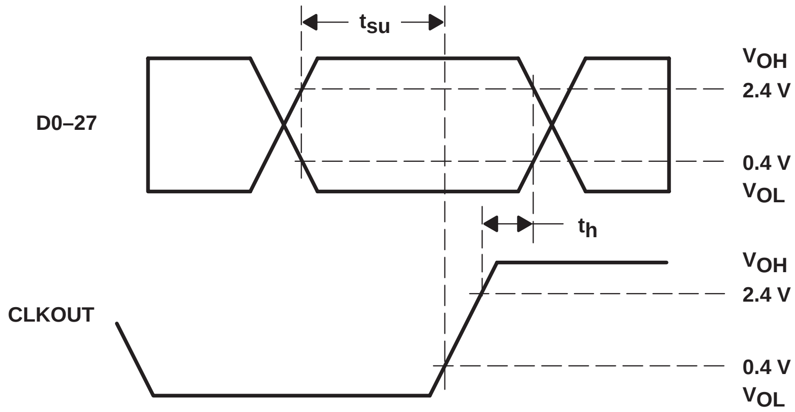
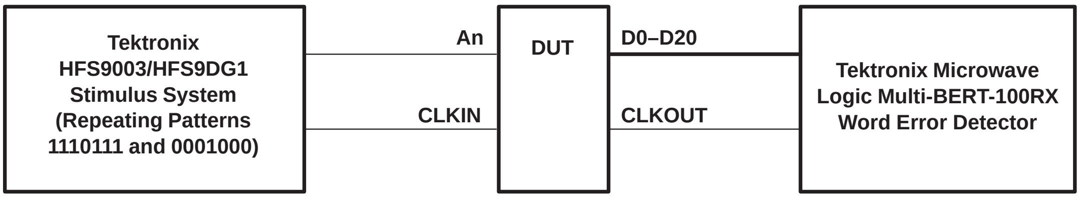


Figure 5. Setup and Hold-Time Measurements

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs.
B. The advance or delay is then reduced until there are no data errors observed.
C. The magnitude of the advance or delay from step 2 is t_{RSKM}.

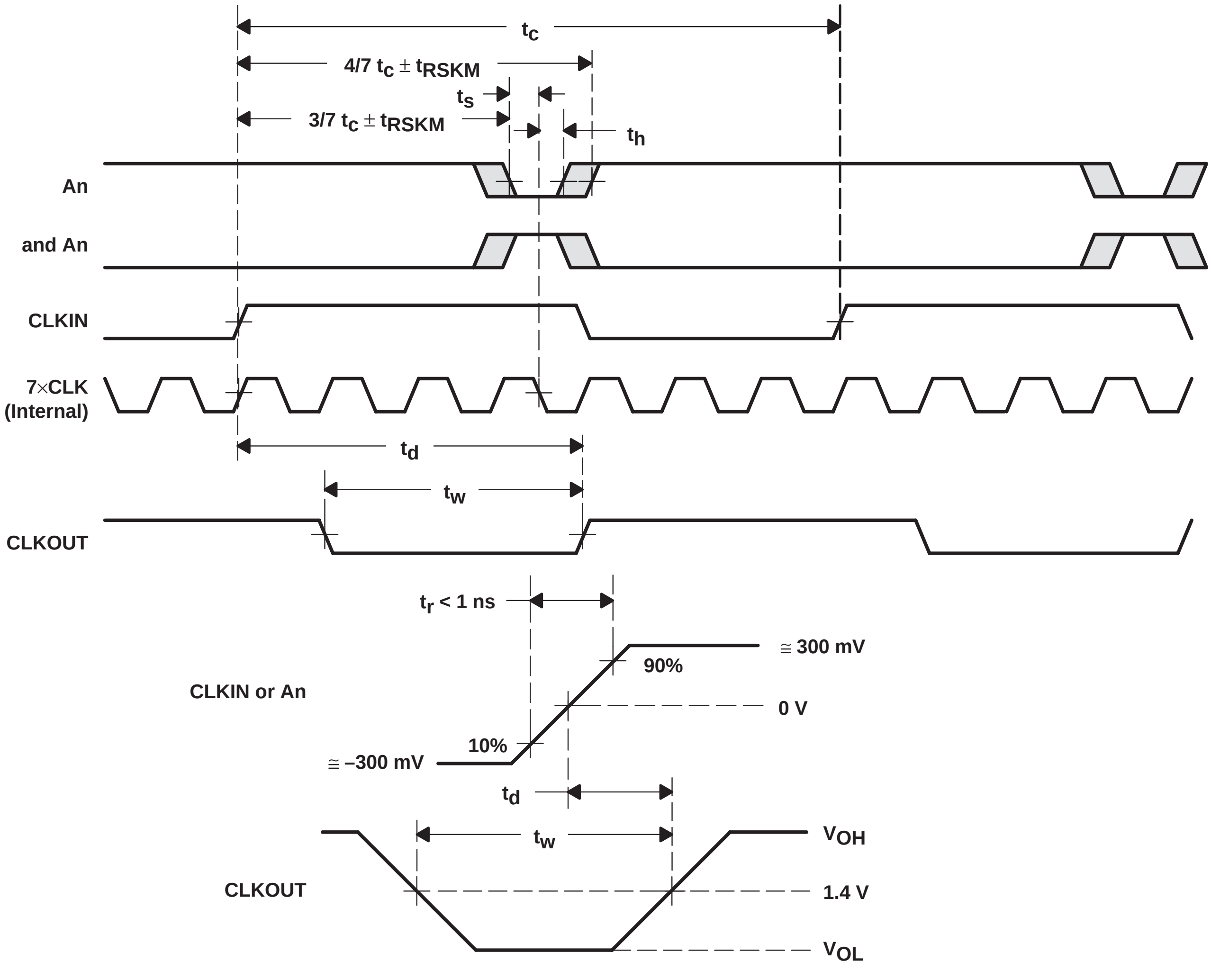


Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and t_d Definitions

PARAMETER MEASUREMENT INFORMATION

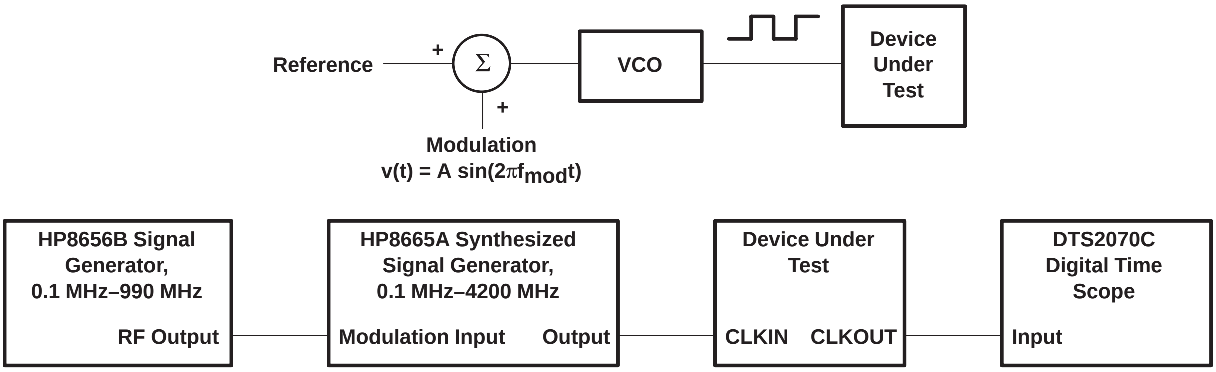


Figure 7. Output Clock Jitter Test Setup

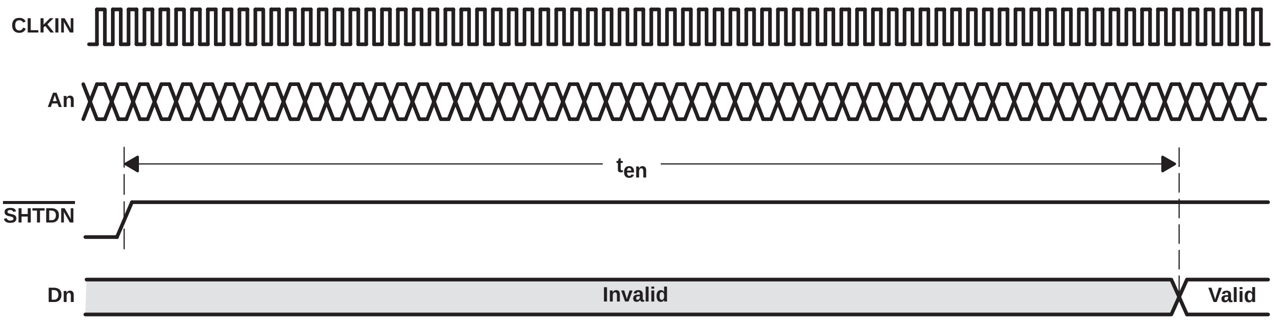


Figure 8. Enable Time Waveforms

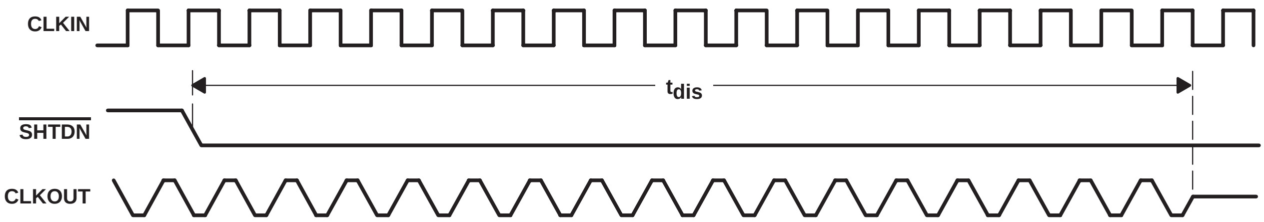


Figure 9. Disable Time Waveforms

TYPICAL CHARACTERISTICS

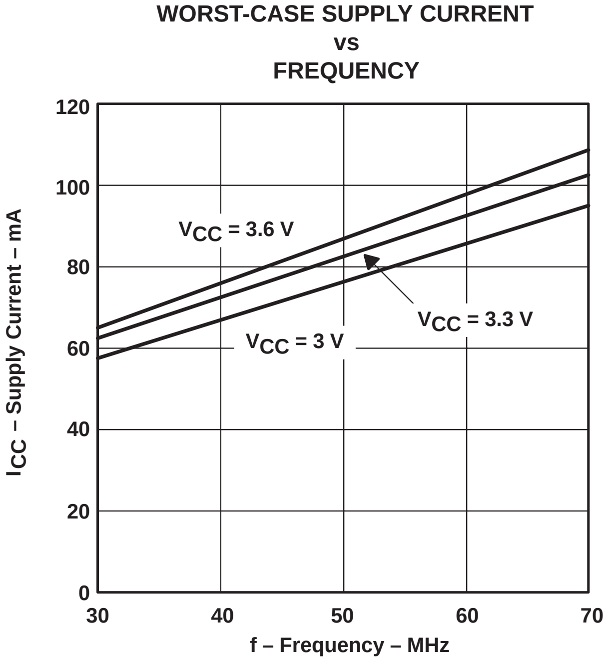


Figure 10

SLLS296F – MAY 1998 – REVISED FEBRUARY 2000

APPLICATION INFORMATION

16-bit bus extension

In a 16-bit bus application (Figure 11), TTL data and clock coming from bus transceivers that interface the backplane bus arrive at the Tx parallel inputs of the LVDS serdes transmitter. The clock associated with the bus is also connected to the device. The on-chip PLL synchronizes this clock with the parallel data at the input. The data is then multiplexed into three different line drivers which perform the TTL to LVDS conversion. The clock is also converted to LVDS and presented to a separate driver. This synchronized LVDS data and clock at the receiver, which recovers the LVDS data and clock, performs a conversion back to TTL. Data is then demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data, and then all are presented to the parallel output port of the receiver.

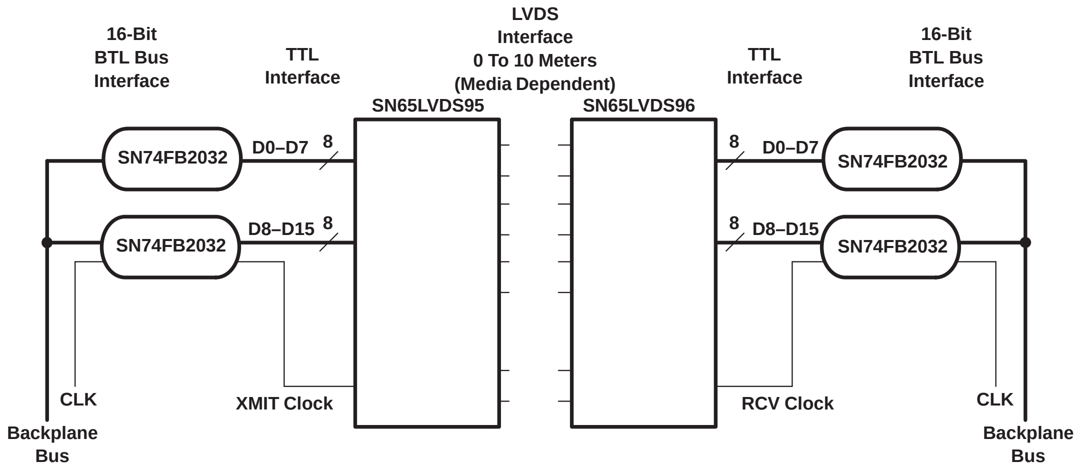


Figure 11. 16-Bit Bus Extension

16-bit bus extension with parity

In the previous application we did not have a checking bit that would provide assurance that the data crosses the link. If we add a parity bit to the previous example, we would have a diagram similar to the one in Figure 12. The device following the SN74FB2032 is a low cost parity generator. Each transmit-side transceiver/parity generator takes the LVTTL data from the corresponding transceiver, performs a parity calculation over the byte, and then passes the bits with its calculated parity value on the parallel input of the LVDS serdes transmitter. Again, the on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock arrive at the receiver.

The receiver performs the conversion from LVDS to LVTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit. The transceiver/parity generator will assert its parity error output if a mismatch is detected.

APPLICATION INFORMATION

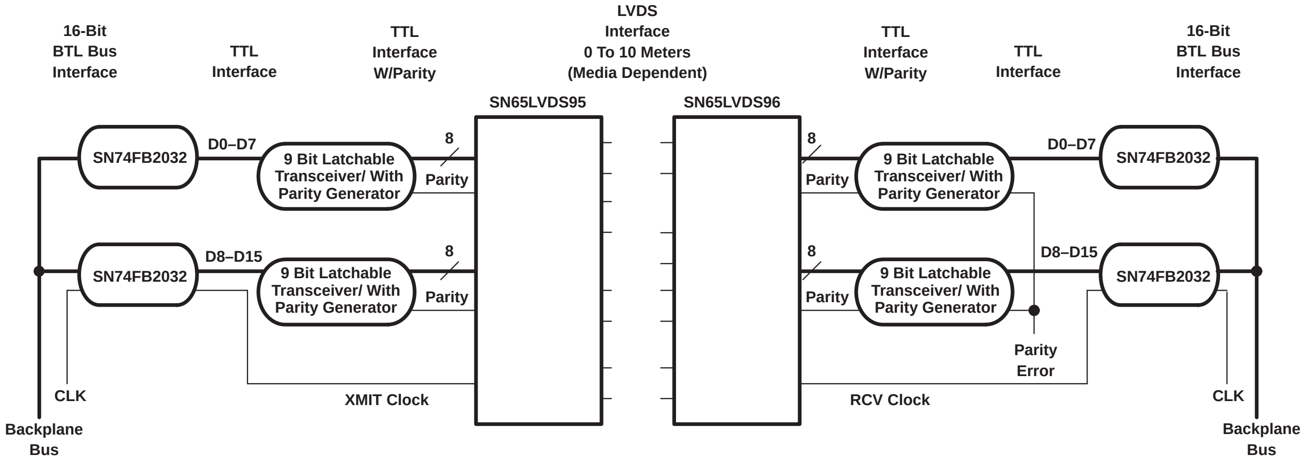


Figure 12. 16-Bit Bus Extension With Parity

low cost virtual backplane transceiver

Figure 13 represents LVDS serdes in an application as a virtual backplane transceiver (VBT). The concept of a VBT can be achieved by implementing individual LVDS serdes chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in Figure 13, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement an independent clock oscillator at each end of the link and then use a PLL to synchronize LVDS serdes's parallel I/O to the backplane bus. Resynchronizing FIFOs may also be required.

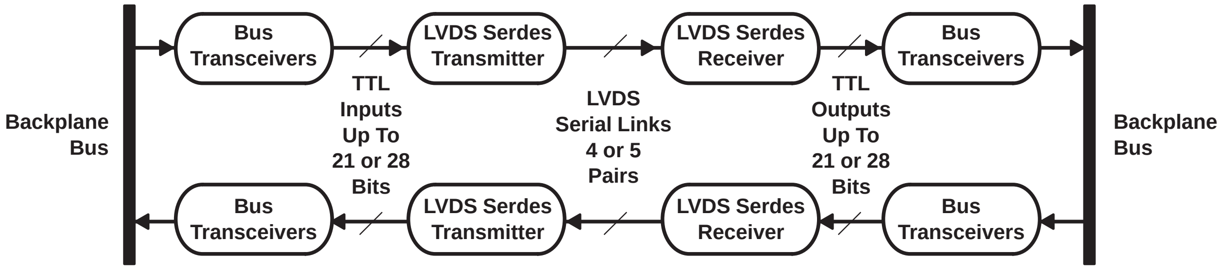


Figure 13. Virtual Backplane Transceiver

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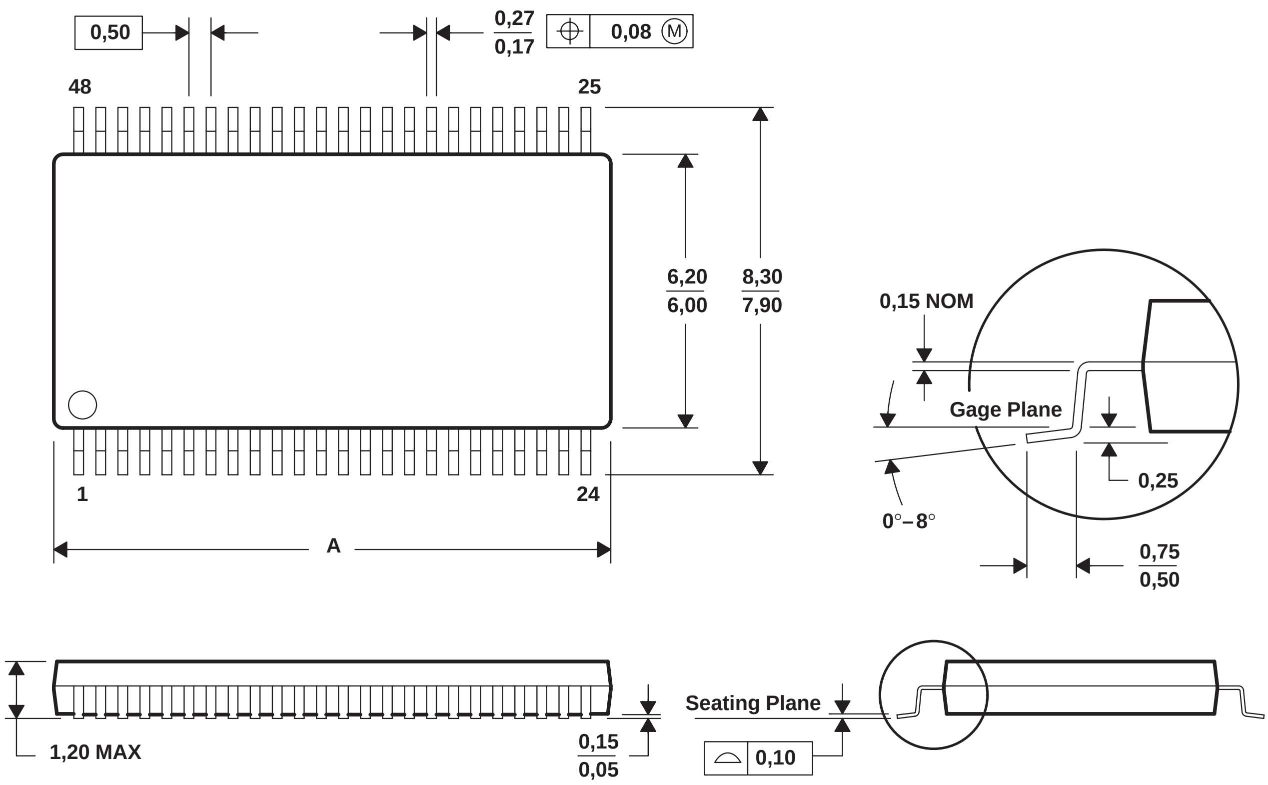
MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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