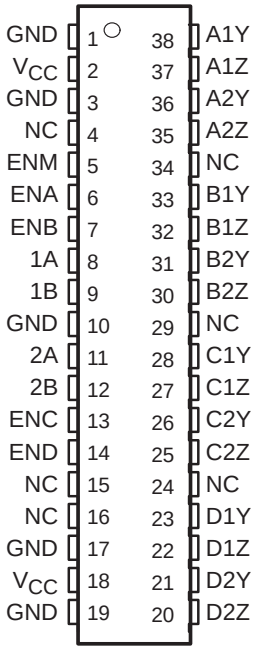
SN65LVDS109, SN65LVDS117
DUAL 4-PORT AND DUAL 8-PORT LVDS REPEATERS

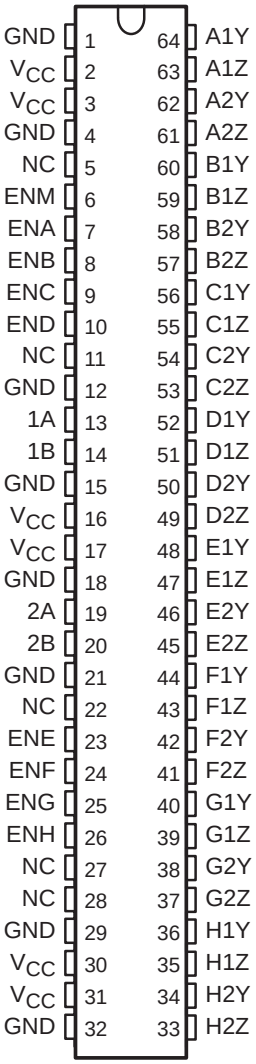
SLLS369C – AUGUST 1999 – REVISED MARCH 2000

- **Two Line Receivers and Eight (’109) or Sixteen (’117) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Designed for Signaling Rates up to 632 Mbps**
- **Outputs Arranged in Pairs From Each Bank**
- **Enabling Logic Allows Individual Control of Each Driver Output Pair, Plus all Outputs**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100Ω Load**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks**
- **Propagation Delay Times < 4.5 ns**
- **Output Skew Less Than 550 ps**
  Bank Skew Less Than 150 ps
  Part-to-Part Skew Less Than 1.5 ns
- **Total Power Dissipation Typically < 500 mW With All Ports Enabled and at 200 MHz**
- **Driver Outputs or Receiver Input Equals High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

SN65LVDS109
DBT PACKAGE
(TOP VIEW)



SN65LVDS117
DGG PACKAGE
(TOP VIEW)



description

The SN65LVDS109 and SN65LVDS117 are configured as two identical banks, each bank having one differential line receiver connected to either four (’109) or eight (’117) differential line drivers. The outputs are arranged in pairs having one output from each of the two banks. Individual output enables are provided for each pair of outputs and an additional enable is provided for all outputs.

The line receivers and line drivers implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers low power, low noise emission, high noise immunity, and high switching speeds. It can be used to transmit data at speeds up to at least 622 Mbps and over relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

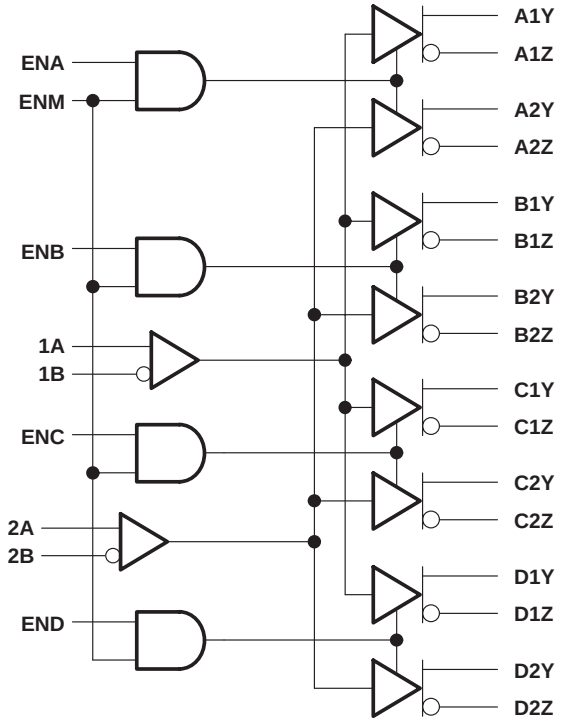
description (continued)

The intended application of these devices, and the LVDS signaling technique, is for point-to-point or point-to-multipoint (distributed simplex) baseband data transmission on controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same silicon substrate, along with the low pulse skew of balanced signaling, provides extremely precise timing alignment of the signals being repeated from the inputs. This is particularly advantageous for implementing system clock and data distribution trees.

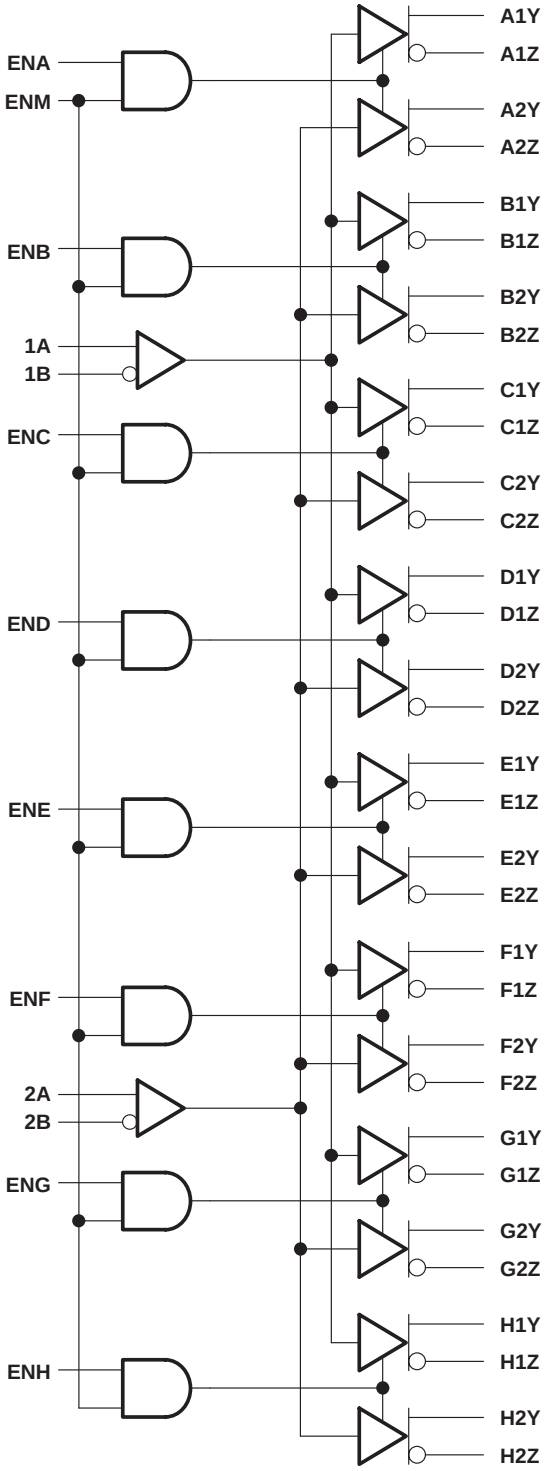
The SN65LVDS109 and SN65LVDS117 are characterized for operation from –40°C to 85°C.

logic diagram (positive logic)

SN65LVDS109



SN65LVDS117



selection guide to LVDS splitters

The SN65LVDS109 and SN75LVDS117 are both members of a family of LVDS splitters and repeaters. A brief overview of the family is provided by the following table.

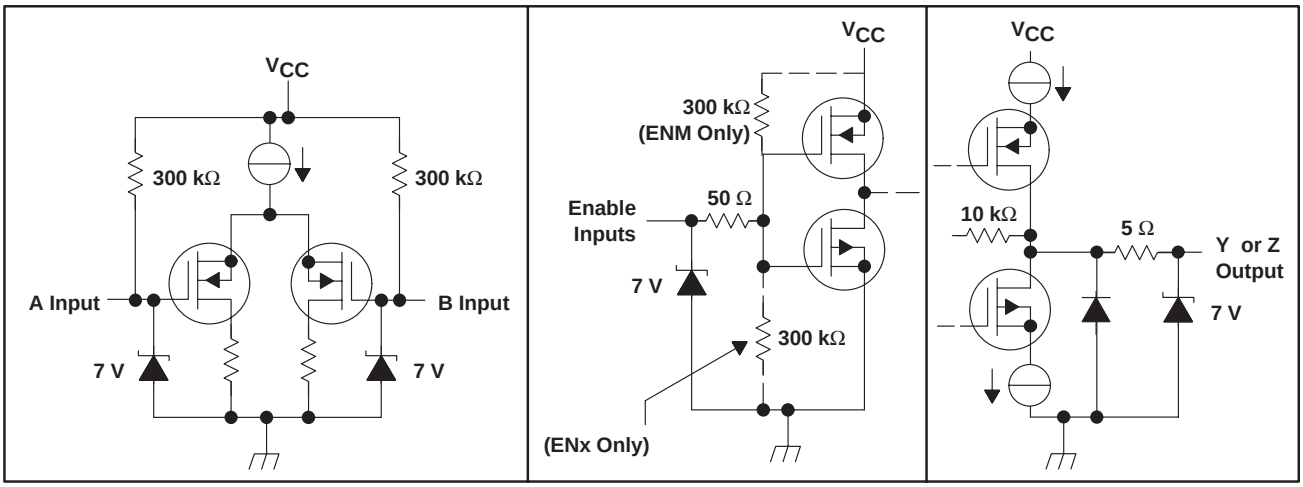
LVDS SPLITTER AND REPEATER FAMILY

DEVICE	NUMBER OF INPUTS	NUMBER OF OUTPUTS	PACKAGE	COMMENTS
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-Port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

FUNCTION TABLE

INPUTS			OUTPUTS	
$V_{ID} = V_A - V_B$	ENM	ENx	$\overline{xY}$	$\overline{xZ}$
X	L	X	Z	Z
X	X	L	Z	Z
$V_{ID} \geq 100$ mV	H	H	H	L
-100 mV $< V_{ID} < 100$ mV	H	H	?	?
$V_{ID} \leq -100$ mV	H	H	L	H

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range, Enable inputs . . . . . –0.5 V to 6 V
A, B, Y or Z . . . . . –0.5 V to 4 V
Electrostatic discharge, Y, Z, and GND (see Note 2) . . . . . Class 3, A:12 kV, B: 500 V
All pins . . . . . Class 3, A: 4 kV, B: 400 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DBT	1277 mW	10.2 mW/°C	644 mW
DGG	2094 mW	16.7 mW/°C	1089 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		3.6	V
Common-mode input voltage, V_{IC}	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			$V_{CC} - 0.8$	V
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 1 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold			–100			
$\|V_{OD}\|$	Differential output voltage magnitude		R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	
I_{CC}	Supply current	SN65LVDS109	Enabled, R_L = 100 Ω		46	64	mA
			Disabled		6	8	
		SN65LVDS117	Enabled, R_L = 100 Ω		85	122	
			Disabled		6	8	
I_I	Input current (A or B inputs)		V_I = 0 V	–2		–20	µA
			V_I = 2.4 V	–1.2			
$I_{I(OFF)}$	Power-off input current (A or B inputs)		V_{CC} = 1.5 V, V_I = 2.4 V			20	µA
I_{IH}	High-level input current (enables)		V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V			±24	mA
			V_{OD} = 0 V			±12	
I_{OZ}	High-impedance output current		V_O = 0 V or V_{CC}			±1	µA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 1.5 V, V_O = 3.6 V			±1	µA
C_{IN}	Input capacitance (A or B inputs)		V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF
C_O	Output capacitance (Y or Z outputs)		V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		

† All typical values are at 25°C and with a 3.3 V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 4	1.6	2.8	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.6	2.8	4.5	
t_r	Differential output signal rise time		0.3	0.8	1.2	ns
t_f	Differential output signal fall time		0.3	0.8	1.2	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)‡			140	500	ps
$t_{sk(o)}$	Output skew§			100	550	
$t_{sk(b)}$	Bank skew¶			40	150	ps
$t_{sk(pp)}$	Part-to-part skew#				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		5.7	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7.7	15	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.2	15	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			3.2	15	ns

† All typical values are at 25°C and with a 3.3 V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
§ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of any outputs with both inputs tied together.
¶ $t_{sk(b)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of the two outputs of any bank of a single device.
# $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

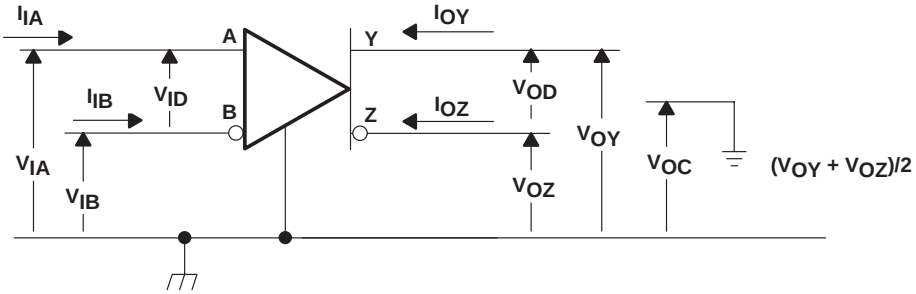


Figure 1. Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

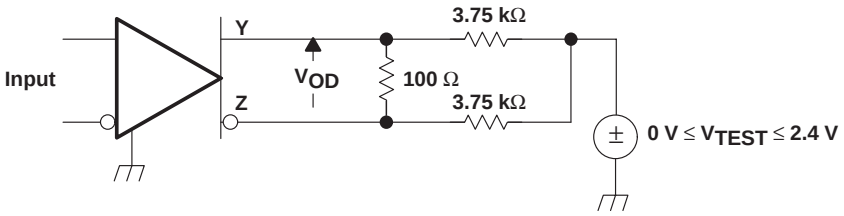
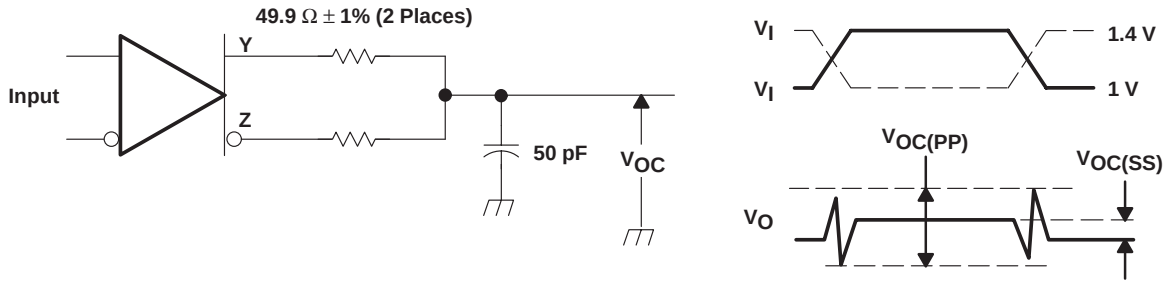


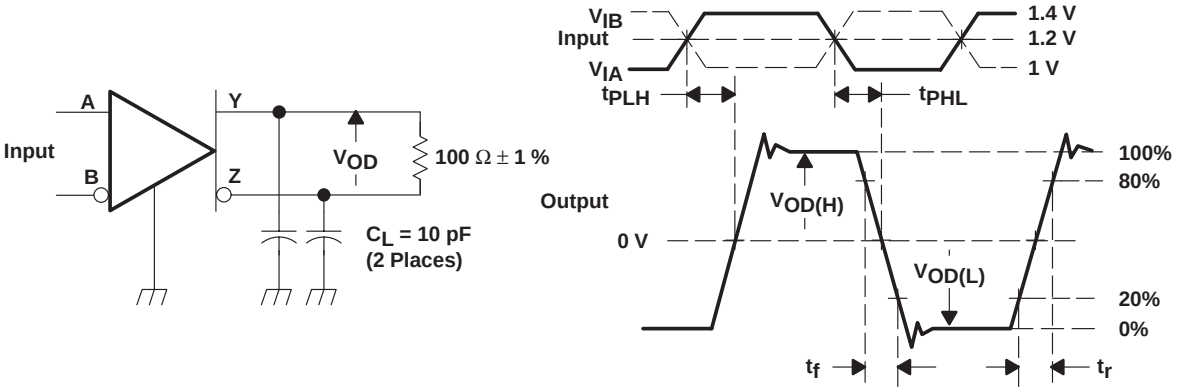
Figure 2. VOD Test Circuit



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

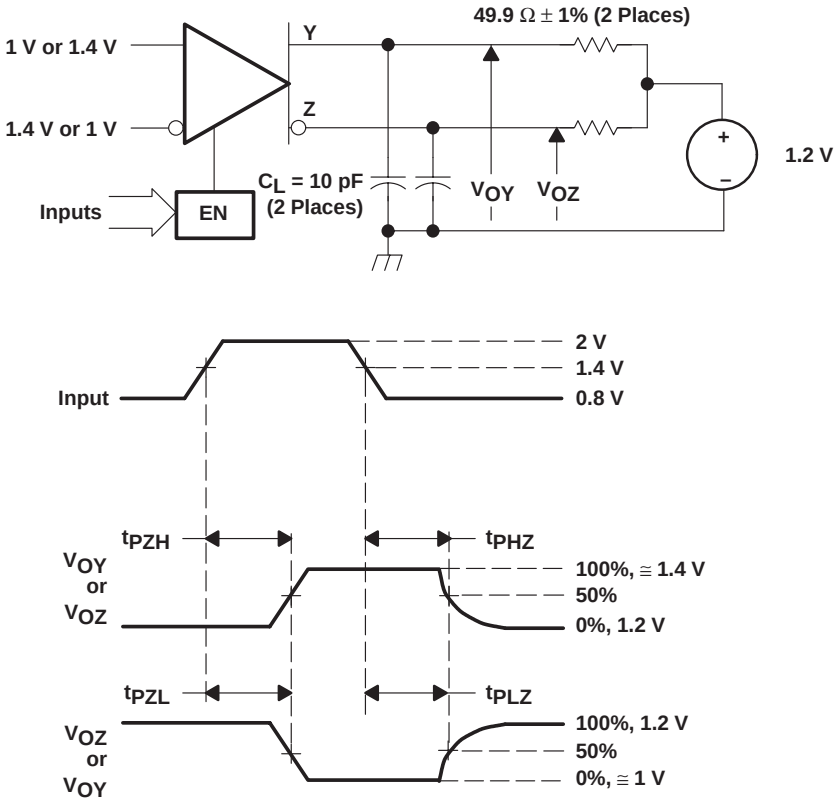
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

SN65LVDS109
SUPPLY CURRENT
vs
SWITCHING FREQUENCY

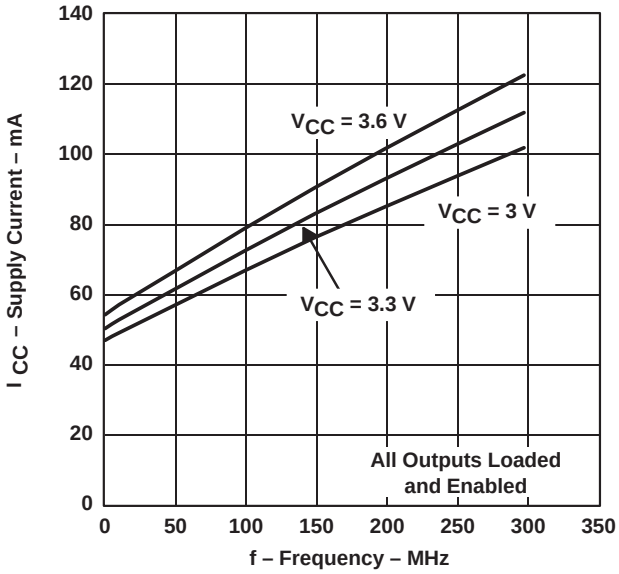


Figure 6

SN65LVDS117
SUPPLY CURRENT
vs
SWITCHING FREQUENCY

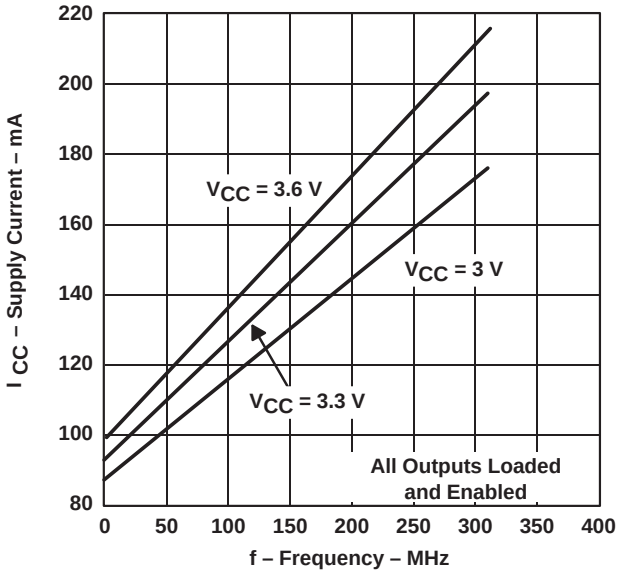


Figure 7

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

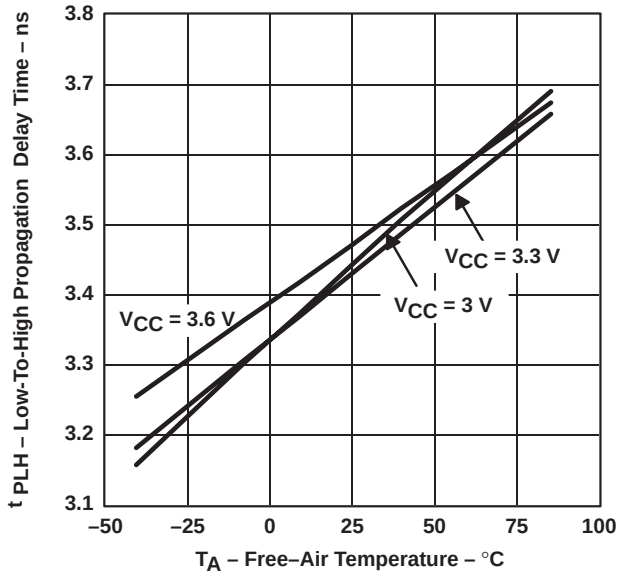


Figure 8

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

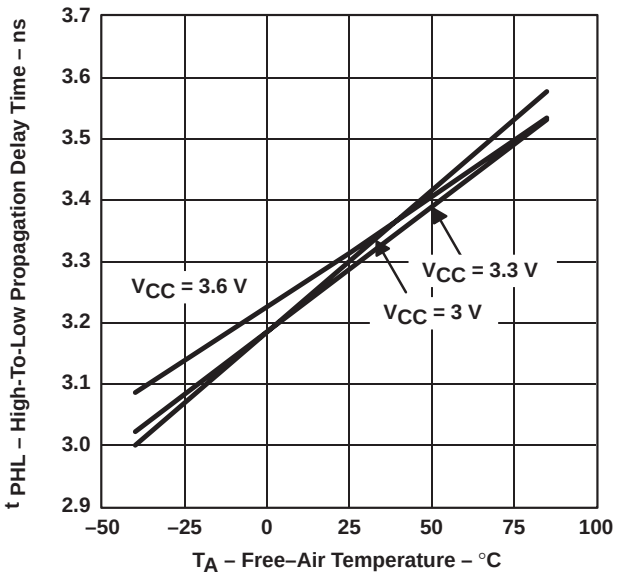


Figure 9

TYPICAL CHARACTERISTICS

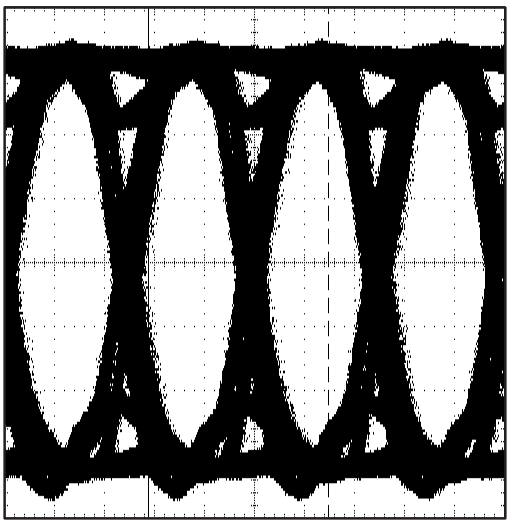


Figure 10. Typical Differential Eye Pattern at 400 Mbps

APPLICATION INFORMATION

The SN65LVDS109 and SN65LVDS117 devices solve several problems common to the distribution of timing critical clock and data signals. These problems include:

- Excessive skew between the signals
- Noise pickup over long signaling paths
- High power consumption
- Control of which signal paths are enabled or disabled
- Elimination of radiation from unterminated lines

Buffering and splitting the two related signals on the same silicon die minimizes corruption of the timing relation between the two signals. Buffering and splitting the two signals in separate devices will introduce considerably higher levels of uncontrolled timing skew between the two signals. Higher speed operation and more timing tolerance for other components of the system is enabled by the tighter system timing budgets provided by the single die implementations of the SN65LVDS109 and SN65LVDS117.

The use of LVDS signaling technology for both the inputs and the outputs provides superior common–mode and noise tolerance compared to single-ended I/O technologies. This is particularly important because the signals that are being distributed must be transmitted over longer distances, and at higher rates, than can be accommodated with single-ended I/Os. In addition, LVDS consumes considerably less power than other high-performance differential signaling schemes.

The enable inputs provided for each output pair may be used to turn on or off any of the paths. This function is required to prevent radiation of signals from the unterminated signal lines on open connectors, such as when boards or devices are being swapped in the end equipment. The individual bank enables are also required if redundant paths are being utilized for reliability reasons.

The diagram below shows how a pair of clock (C) and data (D) input signals is being identically repeated out two of the available output pairs. A third output pair is shown in the disabled state.

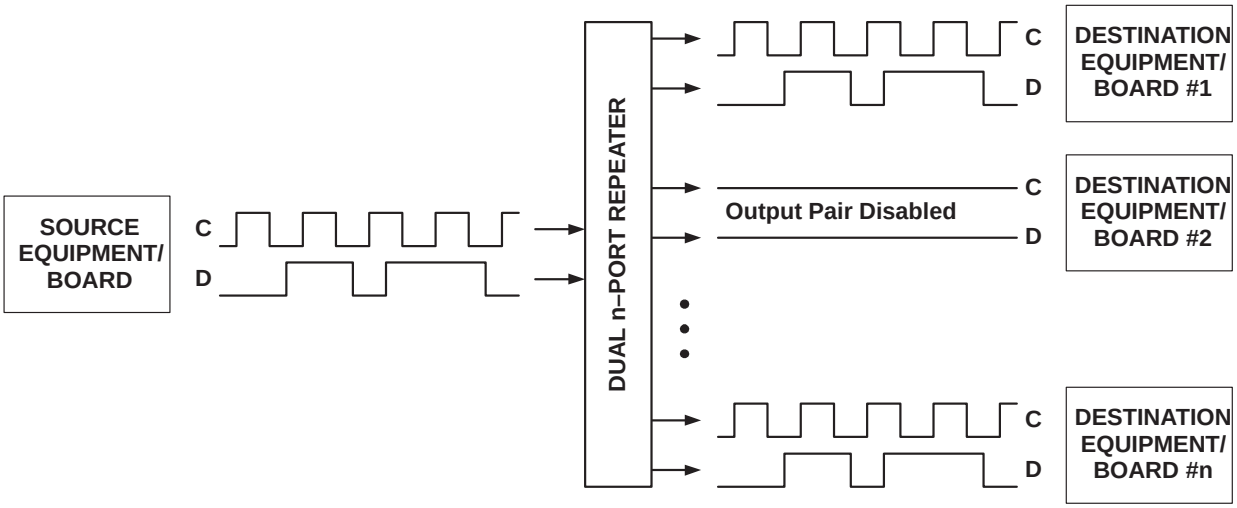


Figure 11. LVDS Repeating Splitter Application Example Showing Individual Path Control

APPLICATION INFORMATION

A LVDS receiver can be used to receive various other types of logic signals. Figure 12 through Figure 20 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

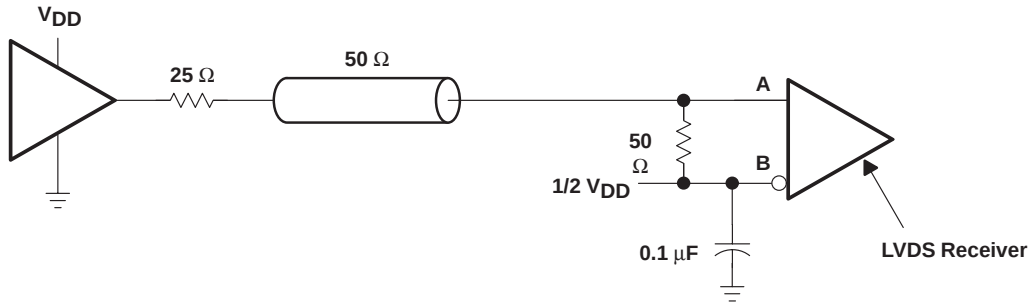


Figure 12. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

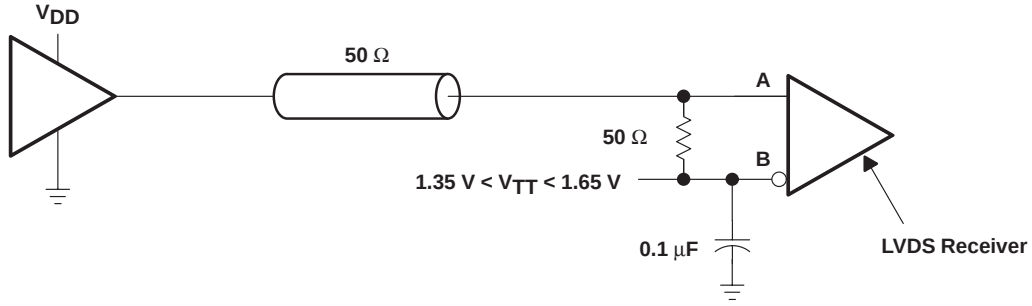


Figure 13. Center-Tap Termination (CTT)

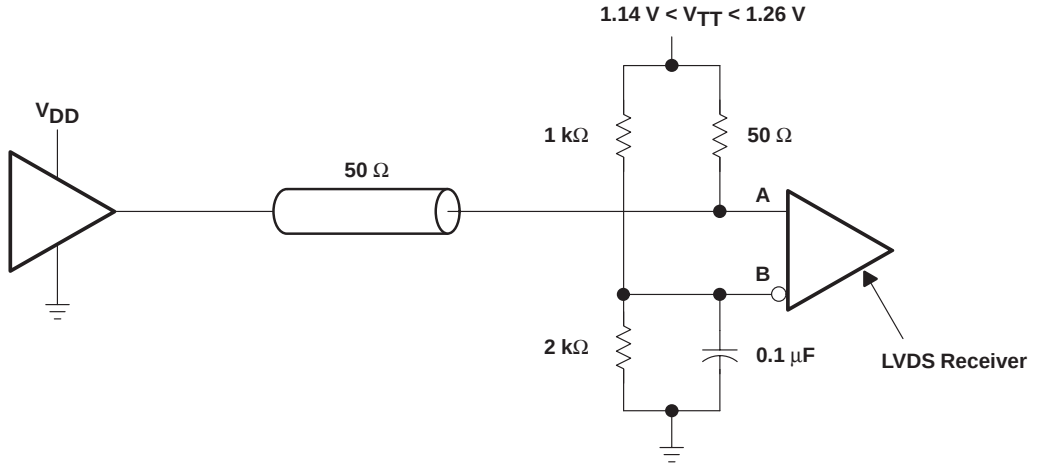


Figure 14. Gunning Transceiver Logic (GTL)

APPLICATION INFORMATION

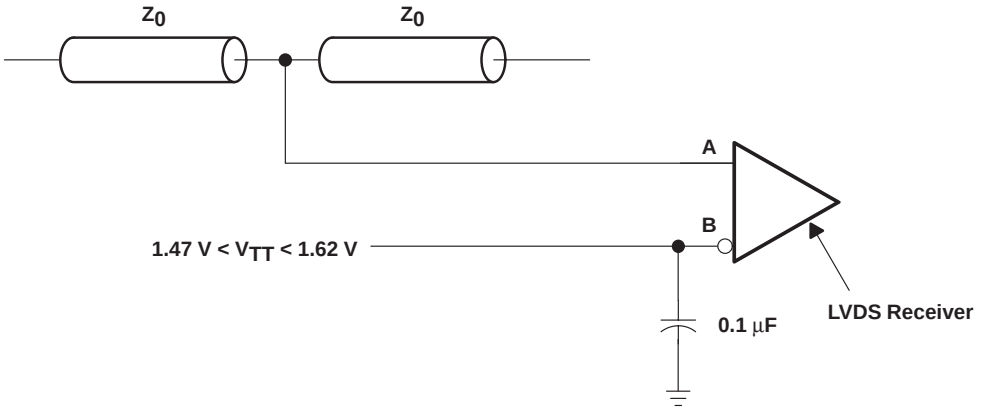


Figure 15. Backplane Transceiver Logic (BTL)

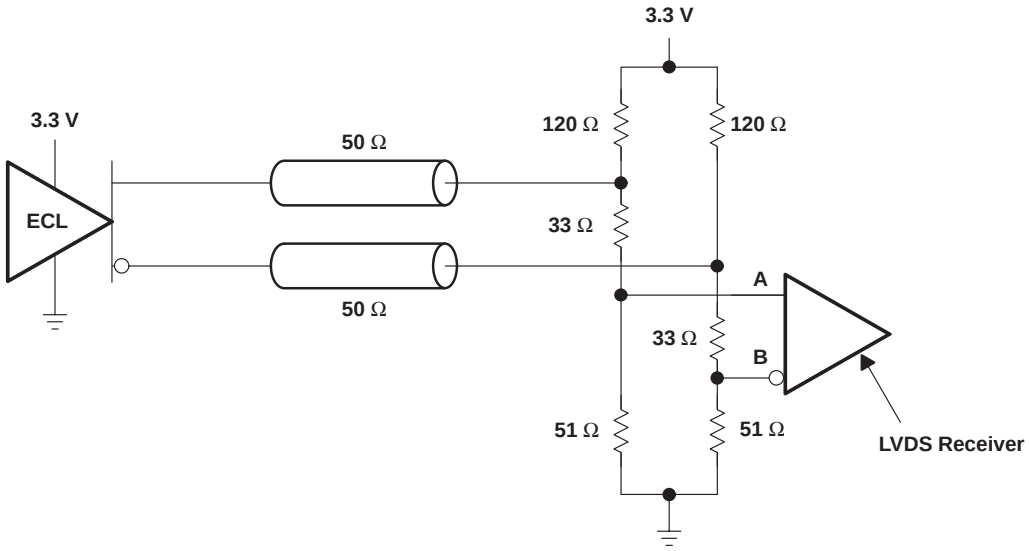


Figure 16. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

APPLICATION INFORMATION

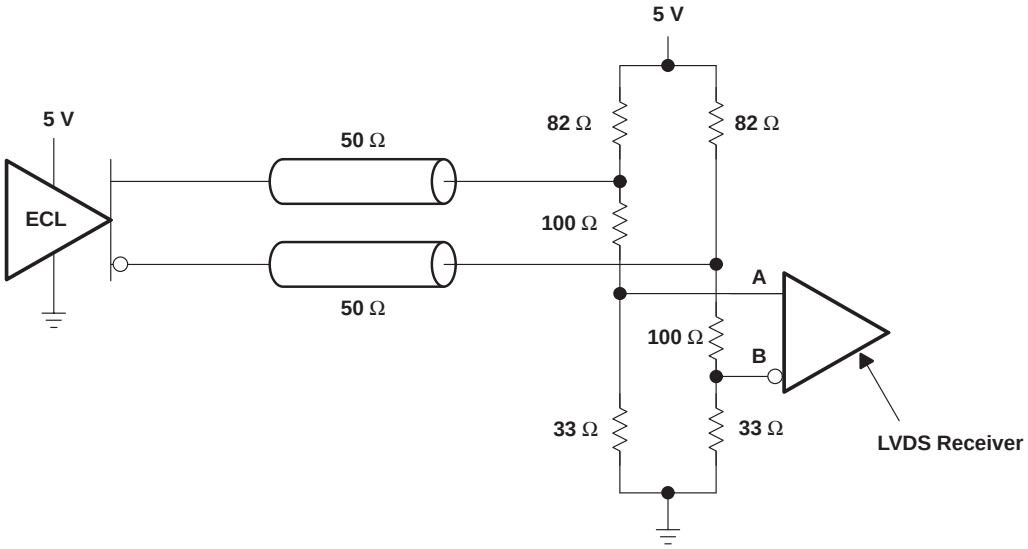


Figure 17. Positive Emitter-Coupled Logic (PECL)

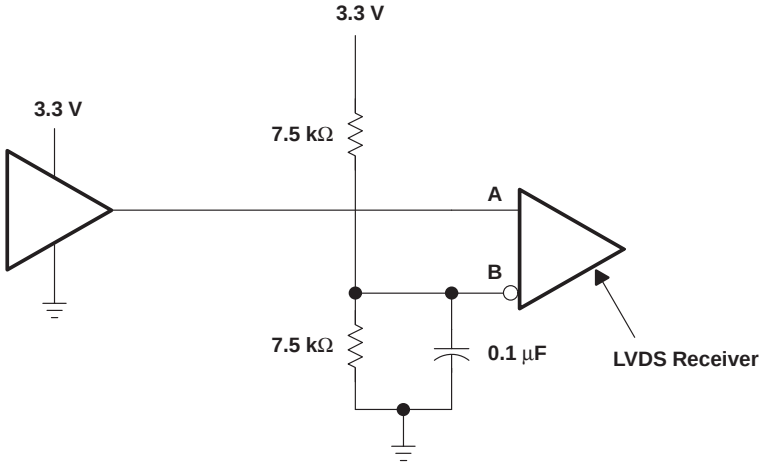


Figure 18. 3.3-V CMOS

APPLICATION INFORMATION

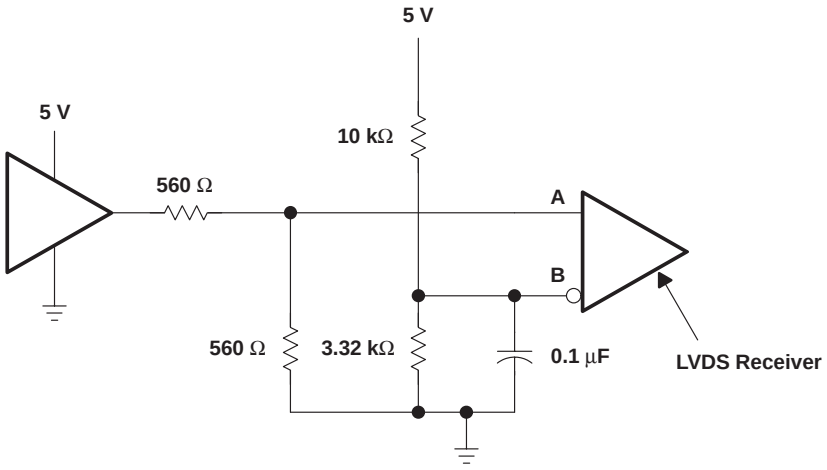


Figure 19. 5-V CMOS

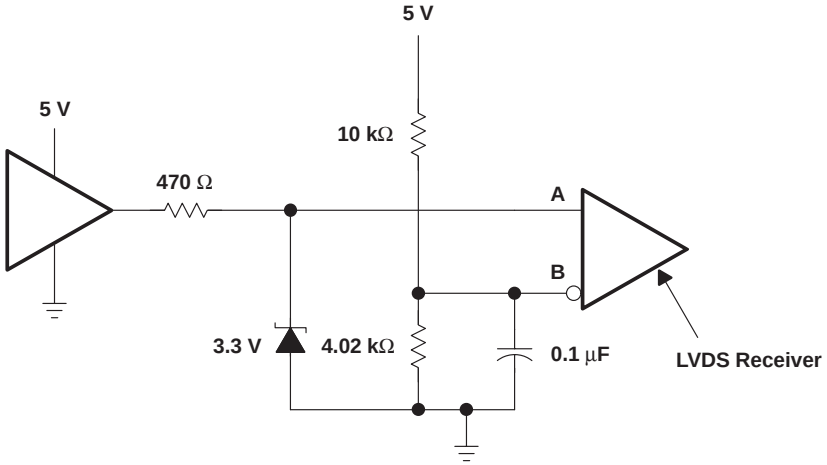
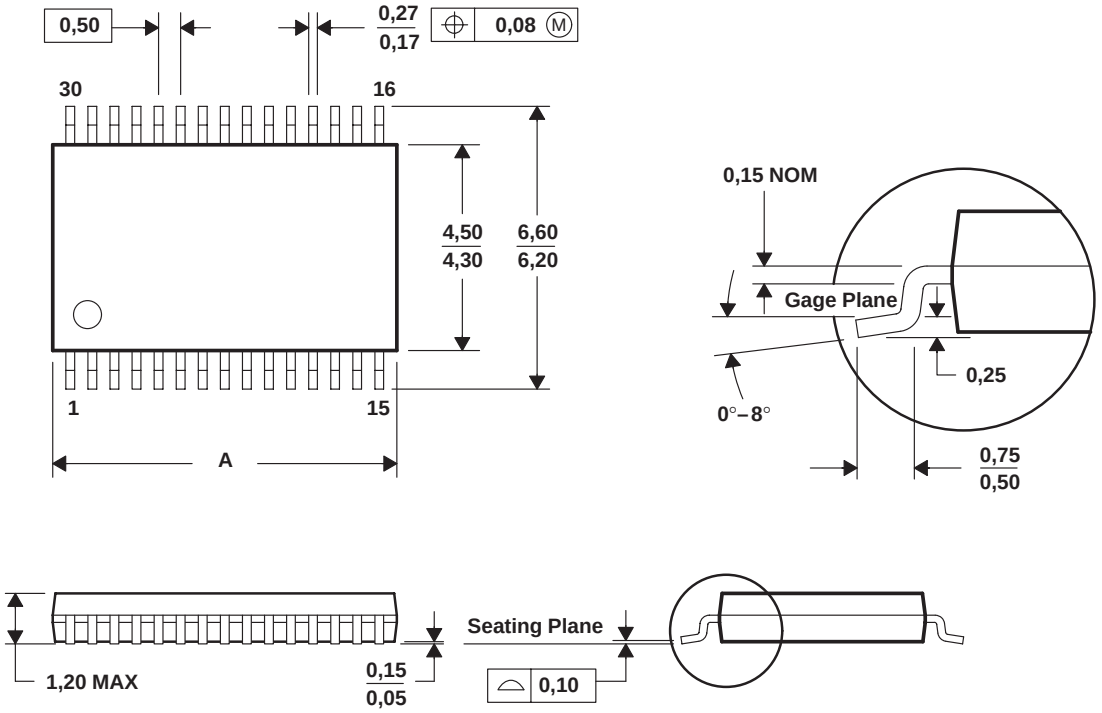


Figure 20. TTL

MECHANICAL DATA

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

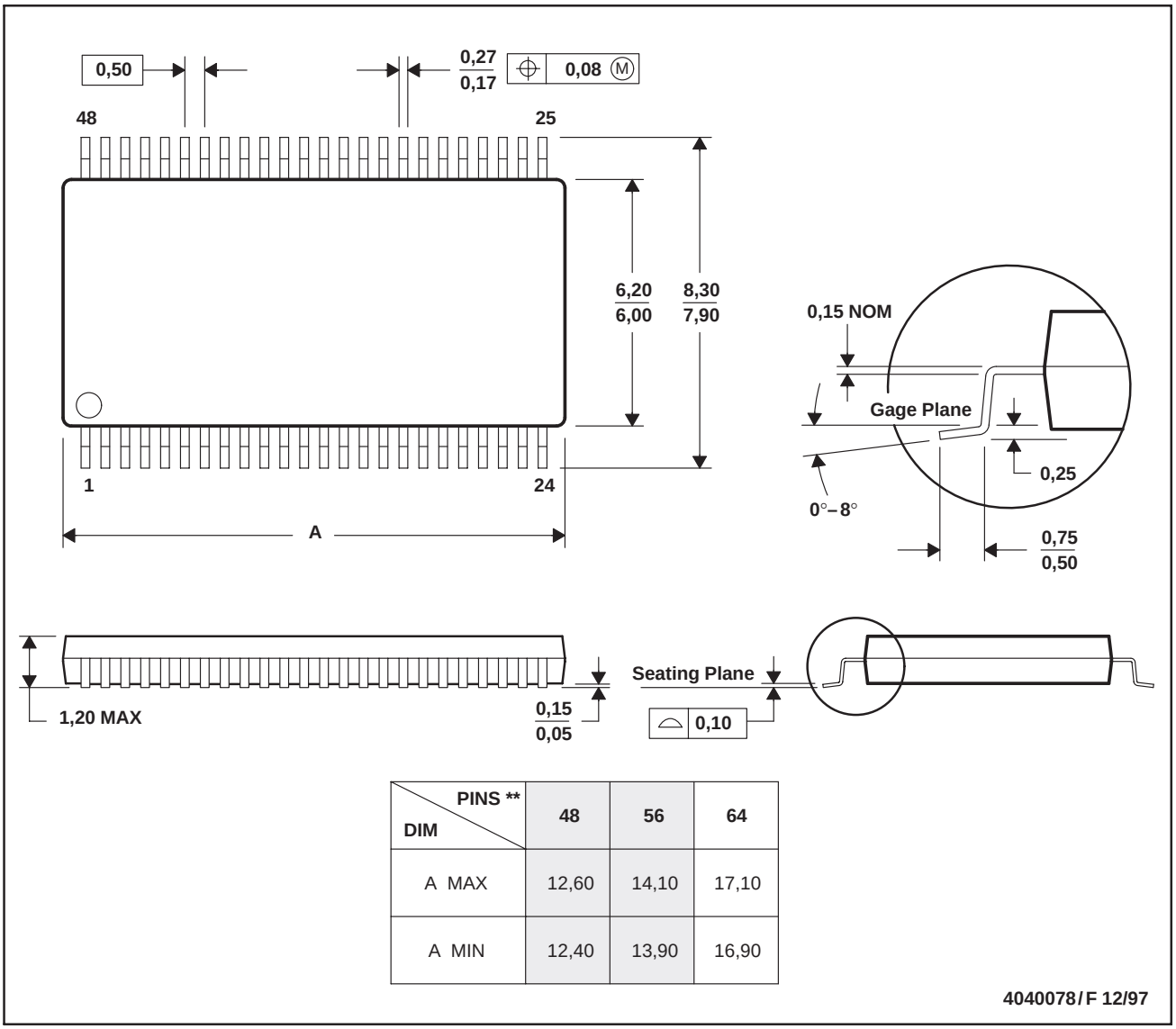
4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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