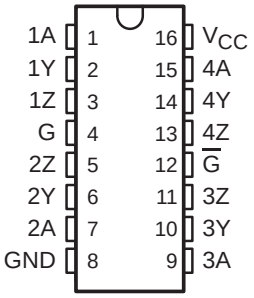
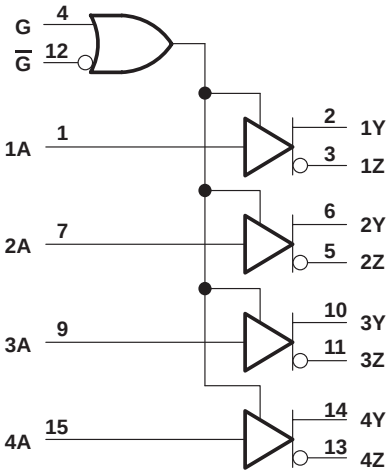
- **Designed for Signaling Rates† up to 150 Mbps**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 700 mV and a 100-Ω Load**
- **Propagation Delay Time of 2.3 ns, Typical**
- **Single 3.3-V Supply Operation**
- **One Driver's Power Dissipation at 75 MHz, 50 mW, Typical**
- **High Impedance Outputs When Disabled or With V_{CC} < 1.5 V**
- **Bus-Pin ESD Protection Exceeds 12 kV**
- **Low-Voltage CMOS (LVCMOS) Logic Input Levels Are 5-V Tolerant**

D PACKAGE
(TOP VIEW)



functional block diagram



description

The SN65LVDM31 incorporates four differential line drivers that implement the electrical characteristics of low-voltage differential signaling. This product offers a low-power alternative to 5-V PECL drivers with similar signal levels. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 540 mV into a 100-Ω load when enabled by either an active-low or active-high enable input.

The intended application of this device and signaling technique is for both point-to-point and multiplexed baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDM31 is characterized for operation from –40°C to 85°C.

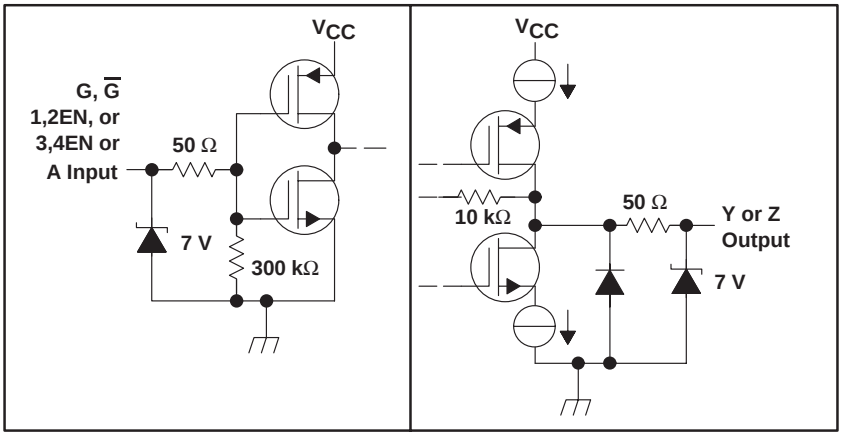
FUNCTION TABLE

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate is the number of voltage transitions that can be made per second.

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range (see Note 1) V_{CC} . . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to 6 V
VOY or VOZ . . . . . –0.5 V to 4 V
Electrostatic discharge, (see Note 2): Y, Z, and GND . . . . . Class 3, A:12 kV, B:600 V
All pins . . . . . Class 3, A:7 kV, B:500 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2.5			V
Low-level input voltage, V_{IL}			0.9	V
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω,	See Figure 2	540	700	860	mV
		R_L = 50 Ω,	See Figure 2	270	350	430	
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	See Figure 2		–25	0	25	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		1.14	1.2	1.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–30	0	30	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				70	100	
I_{CC}	Supply current	Enabled, No load	V_{IN} = 0 or V_{CC}		6	10	mA
		Enabled, R_L = 100 Ω			35	40	
		Disabled			0.5	0.7	
I_{IH}	High-level input current	V_{IH} = 3 V		–10	3	10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V		–10	0	10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			7	10	mA
		V_{OD} = 0 V			7	10	
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{CC}				±1	μA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V,	V_O = 3.6 V			±1	μA

† All typical values are at 25°C and with a 3.3 V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	1.8	2.3	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.8	2.3	2.9	ns
t_r	Differential output signal rise time		0.4	0.6	1.0	ns
t_f	Differential output signal fall time		0.4	0.6	1.0	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			50	350	ns
$t_{sk(o)}$	Channel-to-channel output skew (see Note 3)				200	ns
$t_{sk(pp)}$	Part-to-part skew (see Note 4)	See Figure 5			1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			6	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low level output			6	15	ns
t_{PHz}	Propagation delay time, high-level-to-high-impedance output			6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			6	15	ns

NOTES: 3. $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.
4. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

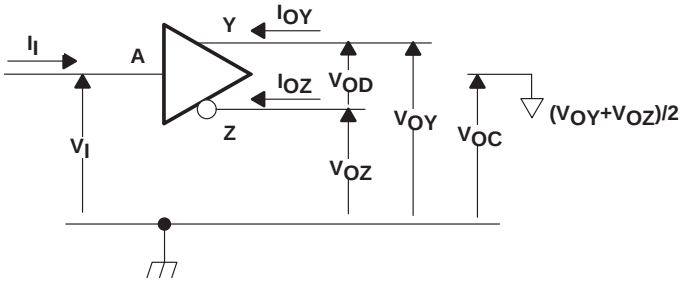


Figure 1. Driver Voltage and Current Definitions

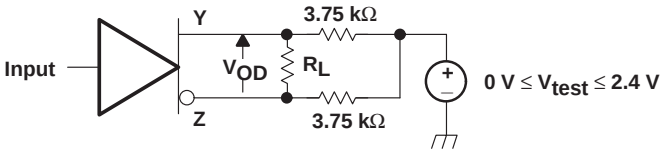
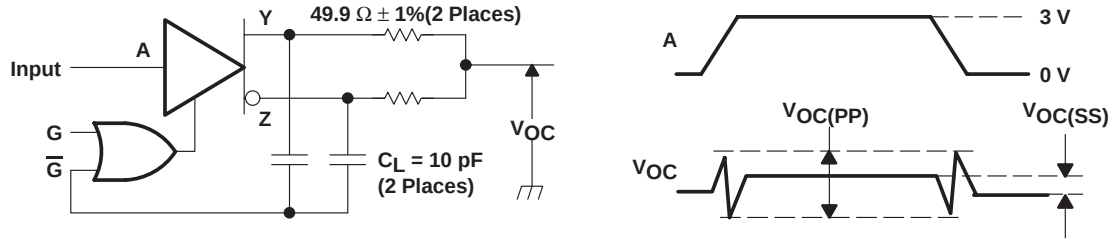


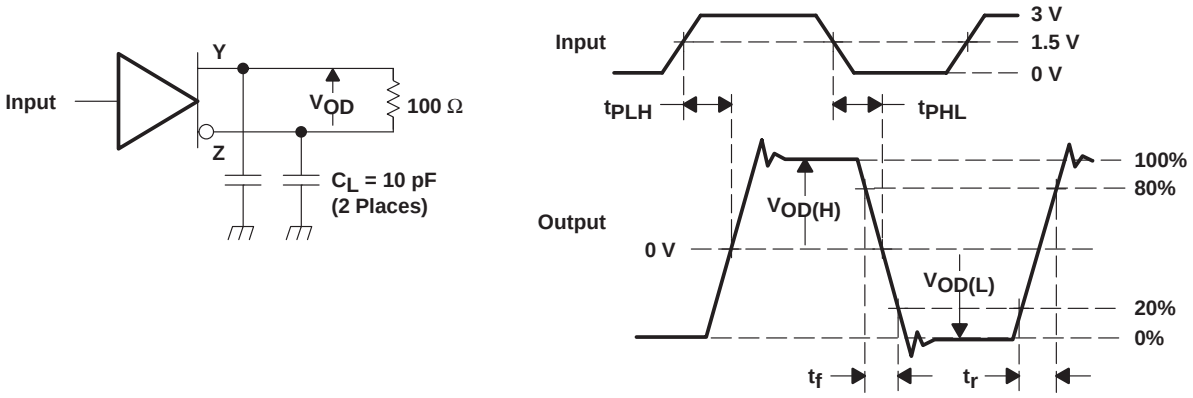
Figure 2. V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

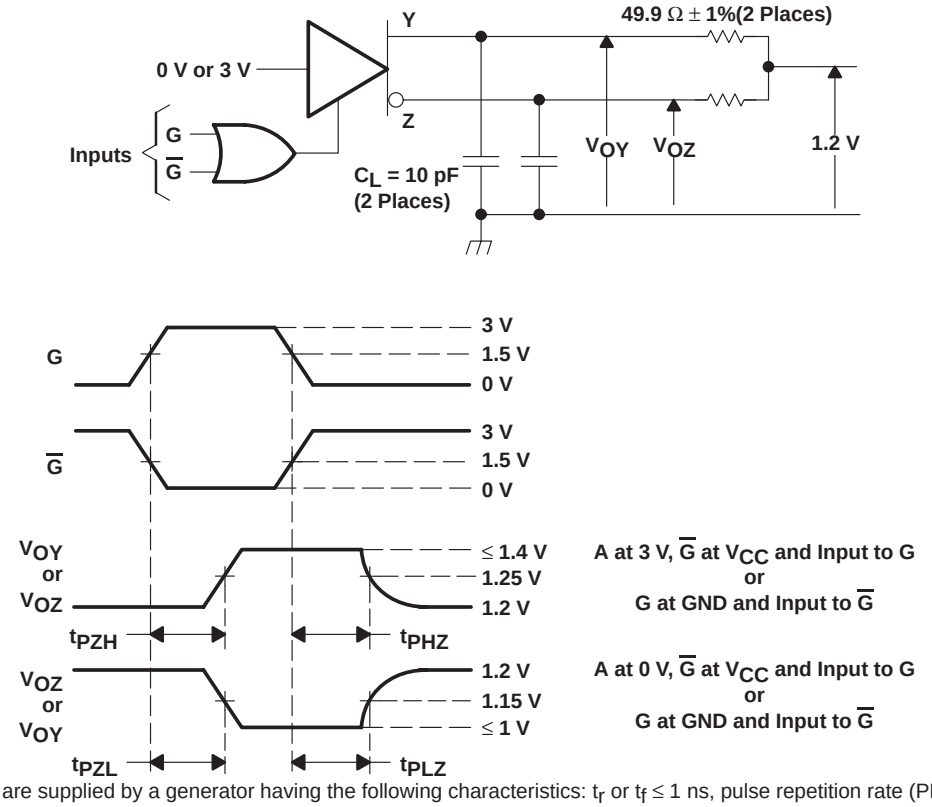
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



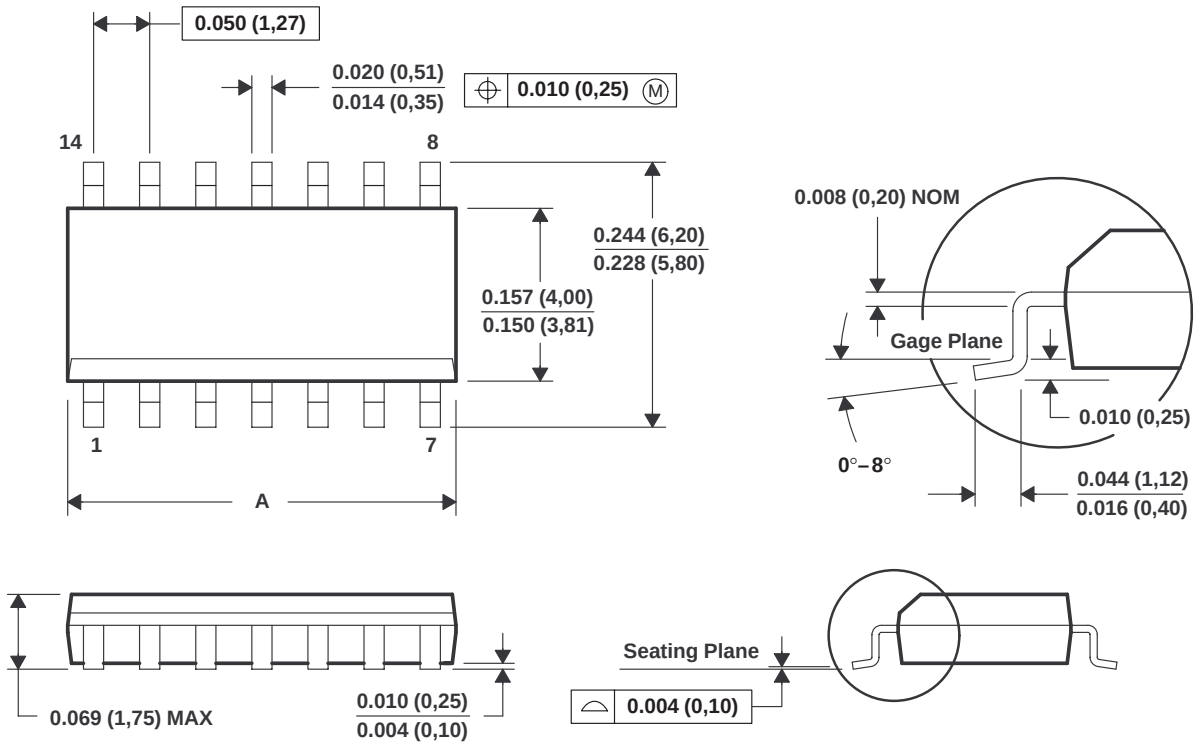
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT.

Figure 5. Enable and Disable Time Circuit and Definitions

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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