

# TPIC1533 QUAD AND HEX POWER DMOS ARRAY

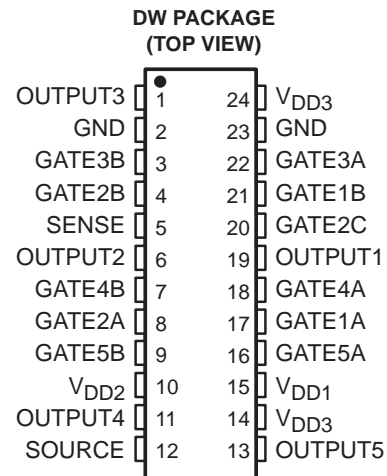
SLIS064 – OCTOBER 1996

- **Low  $r_{DS(on)}$ :**  
0.1  $\Omega$  Typ (Full H-Bridge)  
0.22  $\Omega$  Typ (Triple Half H-Bridge)
- **Pulsed Current:**  
12 A Per Channel (Full H-Bridge)  
6 A Per Channel (Triple Half H-Bridge)
- **Matched Sense Transistors for Class A-B  
Linear Operation**
- **Fast Commutation Speed**

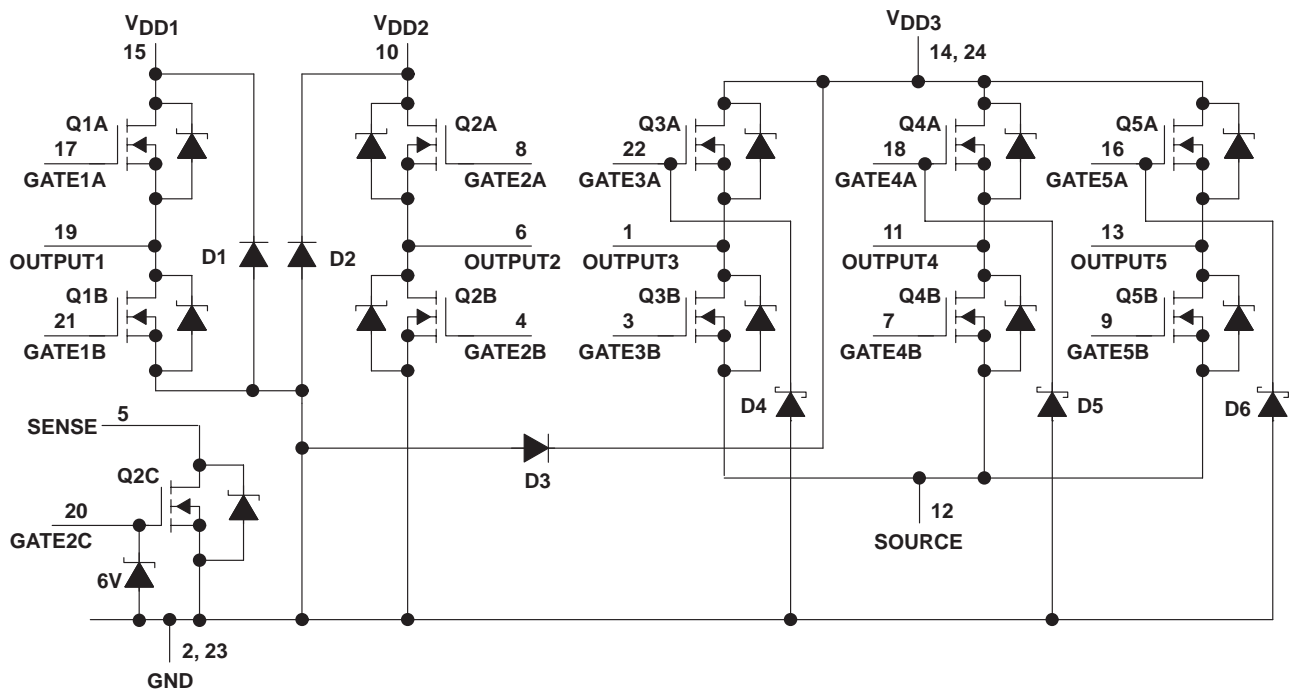
## description

The TPIC1533 is a monolithic power DMOS array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge is provided with an integrated sense-FET to allow biasing of the bridge in class A-B operation.

The TPIC1533 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



## schematic



- NOTES:
- Terminals 2 and 23 must be externally connected.
  - Terminals 14 and 24 must be externally connected.
  - No output may be taken greater than 0.5 V below GND.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# TPIC1533

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### absolute maximum ratings, $T_C = 25^\circ\text{C}$ (unless otherwise noted)<sup>†</sup>

Supply-to-GND voltage .....	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A) .....	20 V
Output-to-GND voltage .....	20 V
Sense-to-GND voltage .....	20 V
Gate-to-source voltage range, $V_{GS}$ (Q1A, Q1B, Q2A, Q2B) .....	$\pm 20$ V
Gate-to-source voltage range, $V_{GS}$ (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) .....	-0.3 V to 20 V
Gate-to-source voltage, $V_{GS}$ (Q2C) .....	-0.7 V to 6 V
Continuous gate-to-source zener-diode current (Q2C) .....	$\pm 10$ mA
Pulsed gate-to-source zener-diode current (Q2C) .....	$\pm 50$ mA
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B) .....	3 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) .....	1.5 A
Continuous drain current (Q2C) .....	15 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B) .....	3 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) .....	1.5 A
Continuous source-to-drain diode current (Q2C) .....	15 mA
Pulsed drain current, each output, $I_{max}$ (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24) .....	12 A
Pulsed drain current, each output, $I_{max}$ (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25) .....	6 A
Pulsed drain current, each output, $I_{max}$ (Q2C) (see Note 1) .....	60 mA
Continuous total power dissipation, $T_C = 70^\circ\text{C}$ (see Note 2 and Figures 24 and 25) .....	2.86 W
Operating virtual junction temperature range, $T_J$ .....	$-40^\circ\text{C}$ to $150^\circ\text{C}$
Operating case temperature range, $T_C$ .....	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	$260^\circ\text{C}$

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Pulse duration = 10 ms, duty cycle = 2%  
2. Package mounted in intimate contact with infinite heatsink.



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## electrical characteristics, Q1A, Q1B, Q2A, Q2B, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$	20			V	
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$ , See Figure 5	$V_{DS} = V_{GS}$	1.4	1.7	2.1	V
		$I_D = 5 \text{ mA}$	$V_{DS} = V_{GS}$	1.65	1.95	2.35	
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	$I_D = 5 \text{ mA}$ , $V_{DS} = V_{GS}$			75	mV	
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = $250 \mu\text{A}$ (D1, D2)	20			V	
$V_{(BR)GS}$	Gate-to-source breakdown voltage, Q2C	$I_{GS} = 100 \mu\text{A}$	6			V	
$V_{(BR)SG}$	Source-to-gate breakdown voltage, Q2C	$I_{SG} = 100 \mu\text{A}$	0.7			V	
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 3 \text{ A}$ , See Notes 3 and 4		0.3	0.36	V	
$V_F$	Forward on-state voltage, GND-to- $V_{DD1}$ , GND-to- $V_{DD2}$	$I_D = 3 \text{ A}$ (D1, D2) See Notes 3 and 4		1.8		V	
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 2 \text{ A}$ , See Notes 3 and 4 and Figure 19	$V_{GS} = 0$	1	1.2	V	
		$I_S = 3 \text{ A}$ , See Notes 3 and 4 and Figure 19	$V_{GS} = 0$	1.1	1.3		
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 16 \text{ V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$	
			$T_C = 125^\circ\text{C}$	0.5	10		
$I_{GSSF}$	Forward gate current, drain short-circuited to source	$V_{GS} = 16 \text{ V}$ , $V_{DS} = 0$		10	100	nA	
$I_{GSSR}$	Reverse gate current, drain short-circuited to source	$V_{SG} = 16 \text{ V}$ , $V_{DS} = 0$		10	100	nA	
$I_{lkg}$	Leakage current, $V_{DD1}$ -to-GND, $V_{DD2}$ -to-GND, gate shorted to source	$V_{DGND} = 16 \text{ V}$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$	
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 2 \text{ A}$ , See Notes 3 and 4 and Figure 9	$T_C = 25^\circ\text{C}$	0.1	0.12	$\Omega$	
			$T_C = 125^\circ\text{C}$	0.14	0.18		
			$T_C = 25^\circ\text{C}$	0.1	0.12		
			$T_C = 125^\circ\text{C}$	0.14	0.18		
$g_{fs}$	Forward transconductance	$V_{DS} = 14 \text{ V}$ , See Notes 3 and 4	$I_D = 1 \text{ A}$	1.5	2.5	S	
			$I_D = 1.5 \text{ A}$ , See Notes 3 and 4 and Figure 13	2	3		
$C_{iss}$	Short-circuit input capacitance, common source	$V_{DS} = 14 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$ , See Figure 17		240		pF	
$C_{oss}$	Short-circuit output capacitance, common source			170			
$C_{rss}$	Short-circuit reverse transfer capacitance, common source			130			
$\alpha_s$	Sense-FET drain current ratio	$V_{DS} = 6 \text{ V}$ , $I_{D(Q2C)} = 40 \mu\text{A}$	100	150	200		

NOTES: 3. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



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### source-to-drain diode characteristics, Q1A, Q2A, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 1.5\text{ A}$ , $V_{DS} = 14\text{ V}$ , See Figures 1 and 23		70		ns
$Q_{RR}$	Total diode charge			90		nC
$t_{rr}$	Reverse-recovery time	$I_S = 2\text{ A}$ , $V_{DS} = 14\text{ V}$ , $V_{GS} = 0$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,		75		ns
$Q_{RR}$	Total diode charge			110		nC

### resistive-load switching characteristics, Q1A, Q1B, Q2A, Q2B, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 14\text{ V}$ , $R_L = 9.1\ \Omega$ , $t_{dis} = 10\text{ ns}$ , See Figure 3		20		ns	
$t_{d(off)}$	Turn-off delay time			30			
$t_r$	Rise time			15			
$t_f$	Fall time			25			
$Q_g$	Total gate charge	$V_{DS} = 14\text{ V}$ , See Figure 4		5.6	7	nC	
$Q_{gs(th)}$	Threshold gate-to-source charge		$I_D = 1.5\text{ A}$ , $V_{GS} = 10\text{ V}$ ,		0.8		1
$Q_{gd}$	Gate-to-drain charge				1.4		1.7
$L_D$	Internal drain inductance			5		nH	
$L_S$	Internal source inductance			5			
$R_g$	Internal gate resistance			0.25		$\Omega$	

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## electrical characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ,	$V_{GS} = 0$	20			V	
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$ ,	$V_{DS} = V_{GS}$ ,	1.4	1.7	2.1	V	
		See Figure 6						
		$I_D = 5\ \text{mA}$ ,	$V_{DS} = V_{GS}$	1.65	1.95	2.35		
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 $\mu\text{A}$ (D3)		20			V	
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 2\ \text{A}$ ,	$V_{GS} = 10\ \text{V}$ ,		0.44	0.6	V	
		See Notes 3 and 4						
$V_F$	Forward on-state voltage, GND-to- $V_{DD3}$	$I_D = 1.5\ \text{A}$ (D3) See Notes 3 and 4			1.7		V	
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1.5\ \text{A}$ ,	$V_{GS} = 0$		1	1.2	V	
		See Notes 3 and 4 and Figure 20						
		$I_S = 2\ \text{A}$ ,	$V_{GS} = 0$		1.1	1.3		
		See Notes 3 and 4 and Figure 20						
$V_F$	Forward on-state voltage, GND-to-GATE 3A, GND-to-GATE4A, GND-to GATE5A	$I_D = 1\ \text{mA}$ (D4, D5, D6)			0.5		V	
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 16\ \text{V}$ ,	$T_C = 25^\circ\text{C}$		0.05	1	$\mu\text{A}$	
			$V_{GS} = 0$	$T_C = 125^\circ\text{C}$		0.5		10
$I_{GSSF}$	Forward gate current, drain short-circuited to source	$V_{GS} = 16\ \text{V}$ ,	$V_{DS} = 0$		10	100	nA	
$I_{lkg}$	Leakage current, $V_{DD3}$ -to-GND, gate shorted to source	$V_{DGND} = 16\ \text{V}$	$T_C = 25^\circ\text{C}$		0.05	1	$\mu\text{A}$	
			$T_C = 125^\circ\text{C}$		0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$ ,	$I_D = 1.5\ \text{A}$ ,	See Notes 3 and 4 and Figures 8 and 10	$T_C = 25^\circ\text{C}$	0.22	0.3	$\Omega$
					$T_C = 125^\circ\text{C}$	0.32	0.4	
					$T_C = 25^\circ\text{C}$	0.22	0.3	
					$T_C = 125^\circ\text{C}$	0.32	0.4	
		$V_{GS} = 10\ \text{V}$ ,	$I_D = 2\ \text{A}$ ,	See Notes 3 and 4 and Figure 10				
$g_{fs}$	Forward transconductance	$V_{DS} = 14\ \text{V}$ ,	$I_D = 500\ \text{mA}$ ,	See Notes 3 and 4		0.3	0.8	S
					$V_{DS} = 14\ \text{V}$ ,	$I_D = 750\ \text{mA}$ ,	See Notes 3 and 4 and Figure 14	
$C_{iss}$	Short-circuit input capacitance, common source				120		pF	
$C_{oss}$	Short-circuit output capacitance, common source				140			
$C_{rss}$	Short-circuit reverse transfer capacitance, common source	$V_{DS} = 14\ \text{V}$ ,	$V_{GS} = 0$ ,	$f = 1\ \text{MHz}$ ,	See Figure 18	80		

NOTES: 3: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

4: These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



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### source-to-drain diode characteristics, Q3A, Q4A, Q5A, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 750\text{ mA}$ , $V_{DS} = 14\text{ V}$ , See Figures 2 and 23		45		ns
$Q_{RR}$	Total diode charge			45		nC
$t_{rr}$	Reverse-recovery time	$I_S = 2\text{ A}$ , $V_{DS} = 14\text{ V}$ , $V_{GS} = 0$ , $di/dt = 100\text{ A}/\mu\text{s}$		70		ns
$Q_{RR}$	Total diode charge			100		nC

### resistive-load switching characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 14\text{ V}$ , $R_L = 18.7\ \Omega$ , $t_{dis} = 10\text{ ns}$ , See Figure 3 $t_{en} = 10\text{ ns}$ ,		18		ns
$t_{d(off)}$	Turn-off delay time			25		
$t_r$	Rise time			13		
$t_f$	Fall time			20		
$Q_g$	Total gate charge	$V_{DS} = 14\text{ V}$ , See Figure 4 $I_D = 750\text{ mA}$ , $V_{GS} = 10\text{ V}$ ,		2.3	3.1	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.4	0.5	
$Q_{gd}$	Gate-to-drain charge			0.6	0.9	
$L_D$	Internal drain inductance			5		nH
$L_S$	Internal source inductance			5		
$R_g$	Internal gate resistance			0.25		$\Omega$

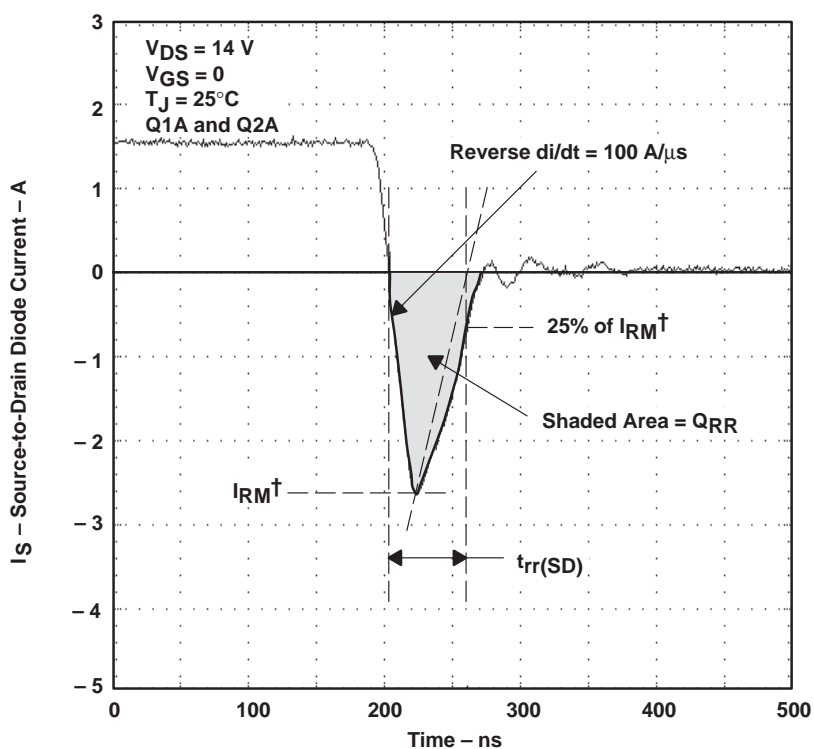
### thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 5 and 8		90		$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 6 and 8		38		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 7 and 8		28		

- NOTES:
5. Package mounted on a FR4 printed-circuit board with no heat sink.
  6. Package mounted on a 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board.
  7. Package mounted in intimate contact with infinite heat sink.
  8. All outputs with equal power



PARAMETER MEASUREMENT INFORMATION



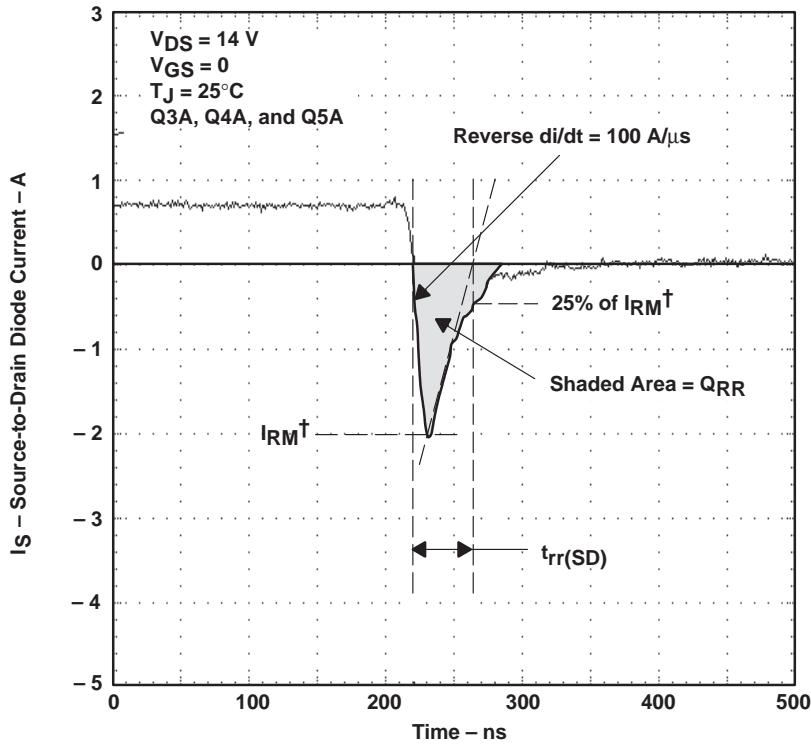
$^\dagger I_{RM}$  = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes

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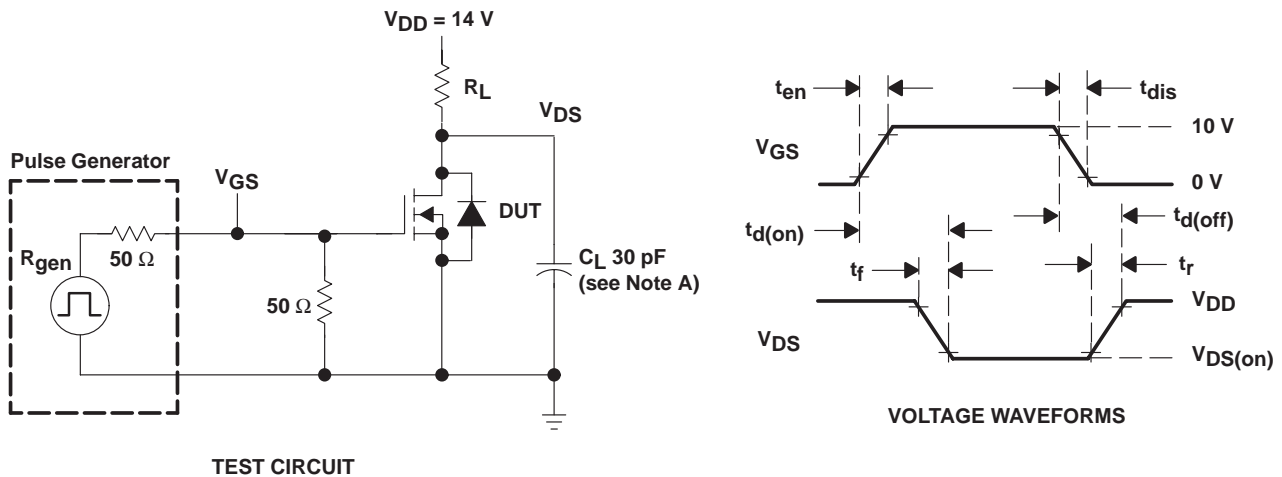
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## PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$  = maximum recovery current

Figure 2. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes



TEST CIRCUIT

NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 3. Resistive-Switching Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION

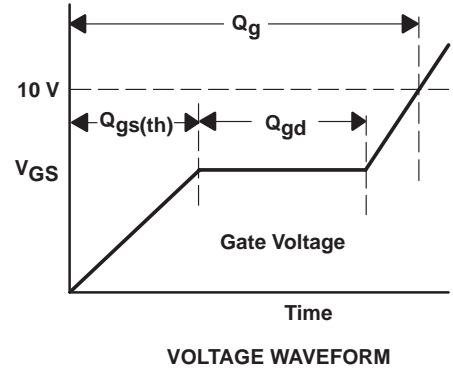
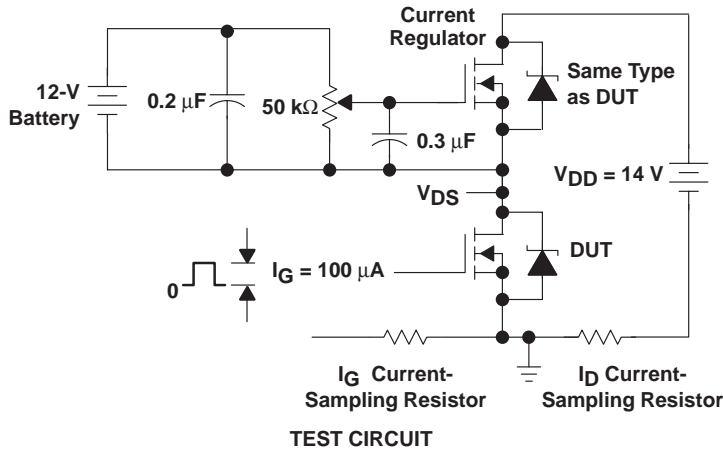


Figure 4. Gate-Charge Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

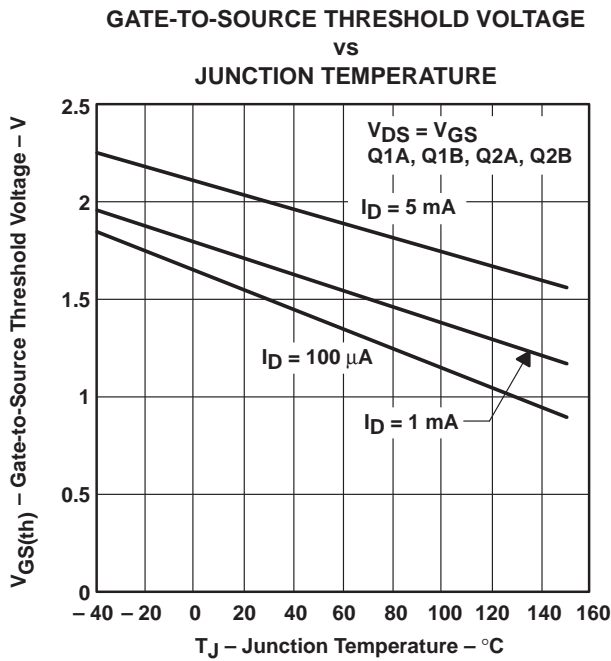


Figure 5

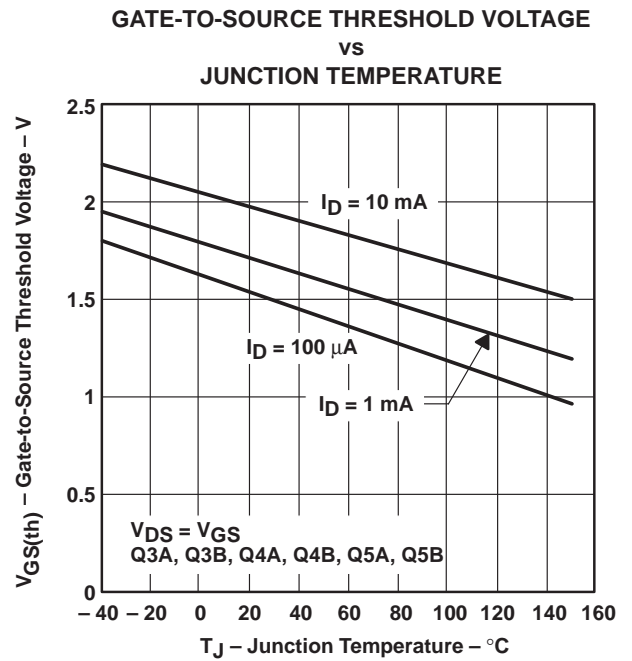


Figure 6

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## TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE  
ON-STATE RESISTANCE  
vs  
JUNCTION TEMPERATURE

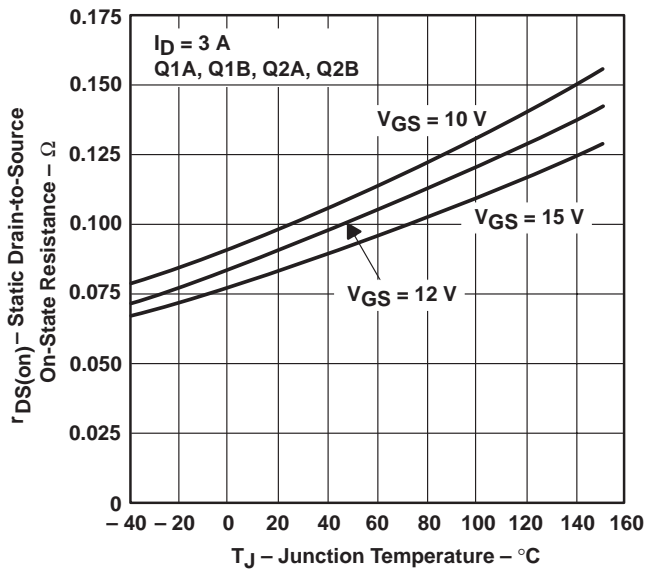


Figure 7

STATIC DRAIN-TO-SOURCE  
ON-STATE RESISTANCE  
vs  
JUNCTION TEMPERATURE

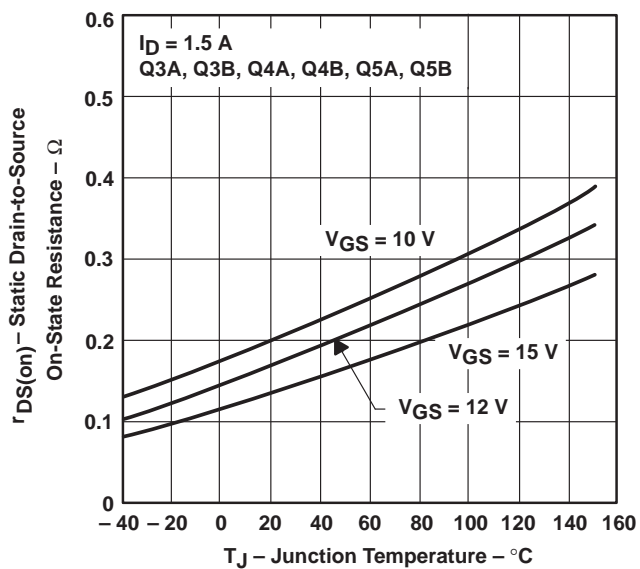


Figure 8

STATIC DRAIN-TO-SOURCE  
ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

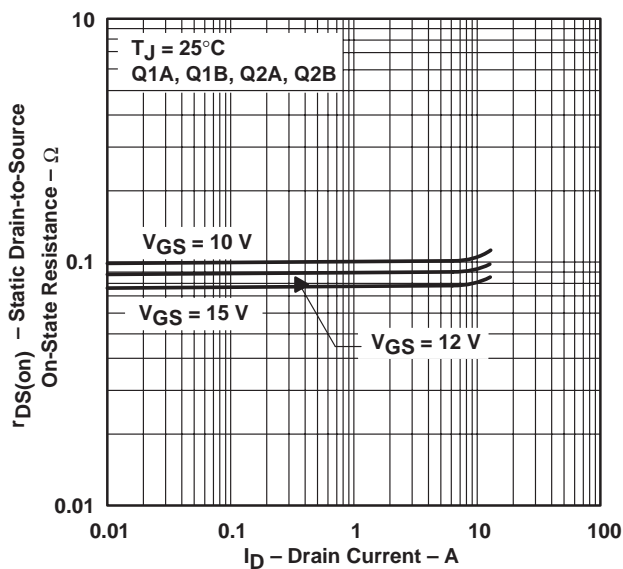


Figure 9

STATIC DRAIN-TO-SOURCE  
ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

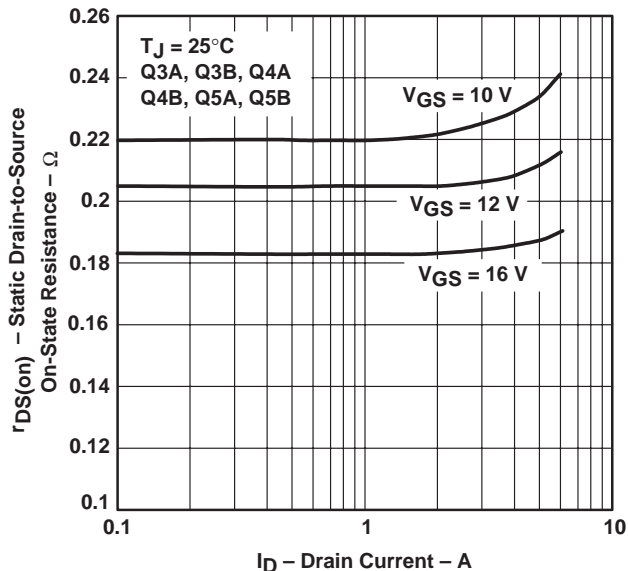


Figure 10



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TYPICAL CHARACTERISTICS

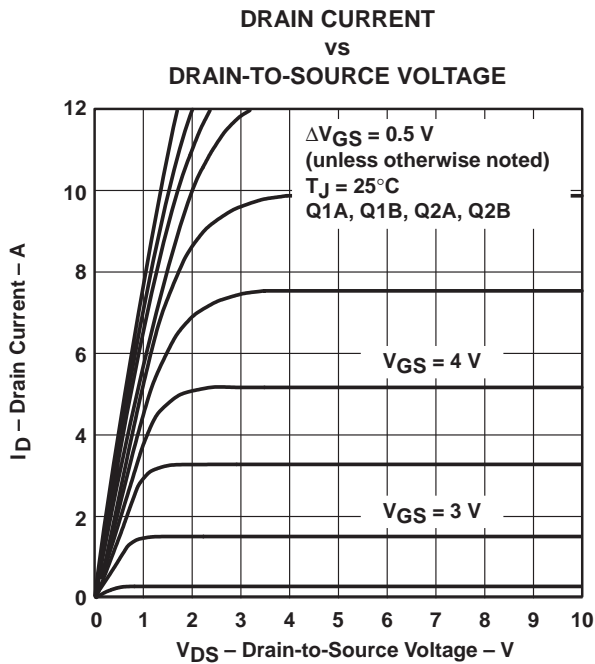


Figure 11

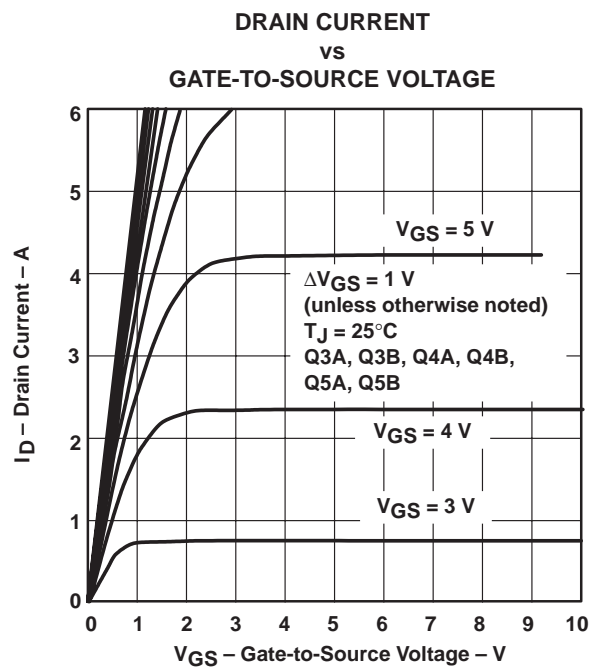


Figure 12

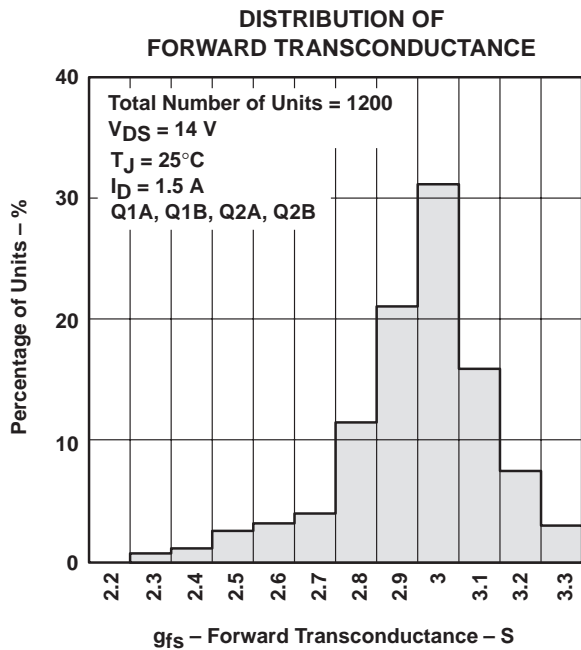


Figure 13

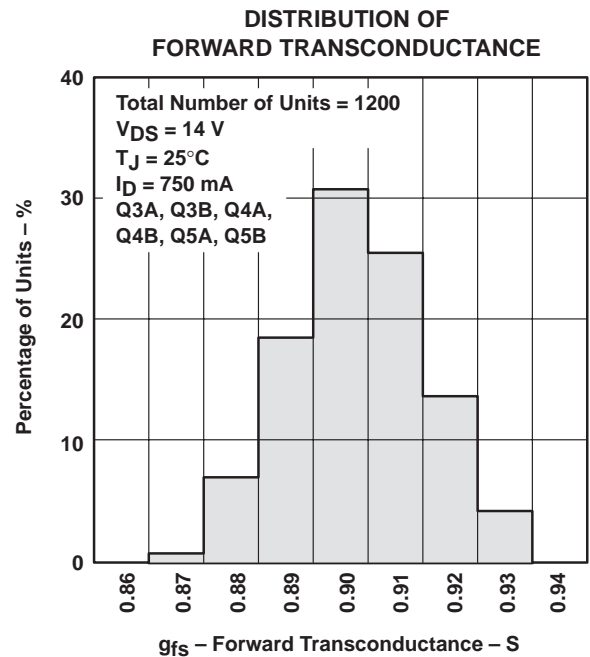


Figure 14

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## TYPICAL CHARACTERISTICS

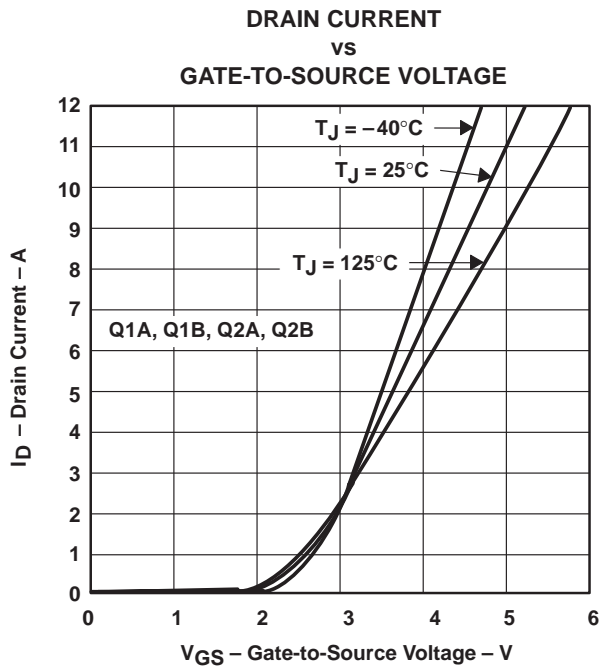


Figure 15

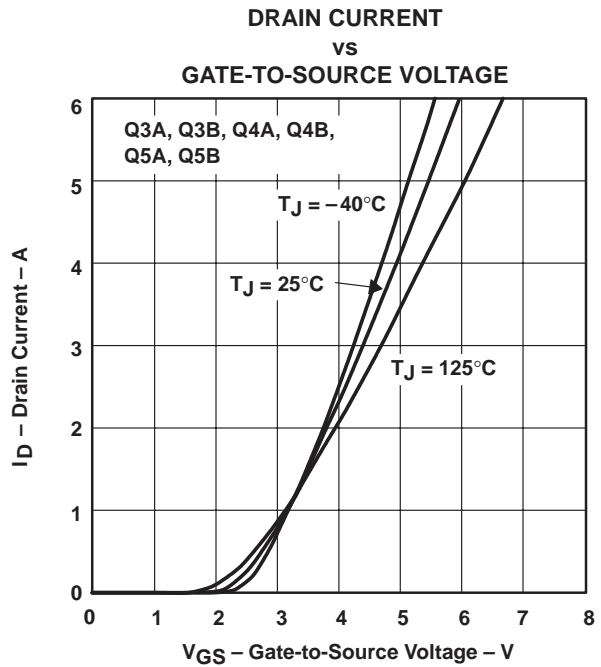


Figure 16

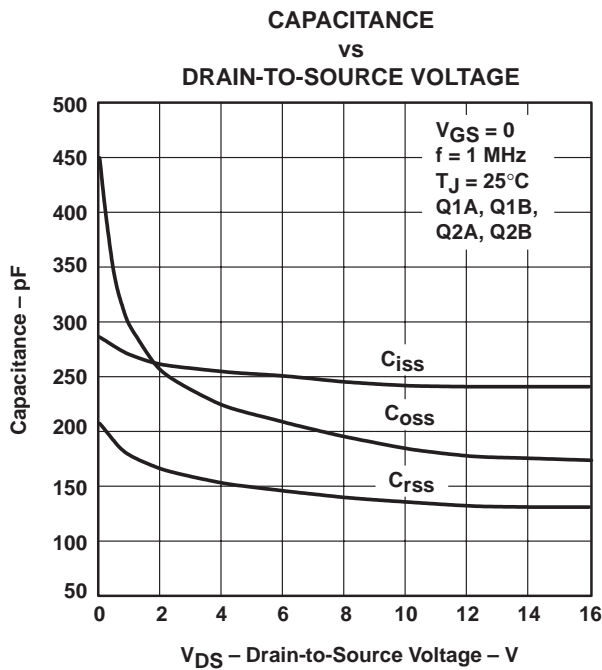


Figure 17

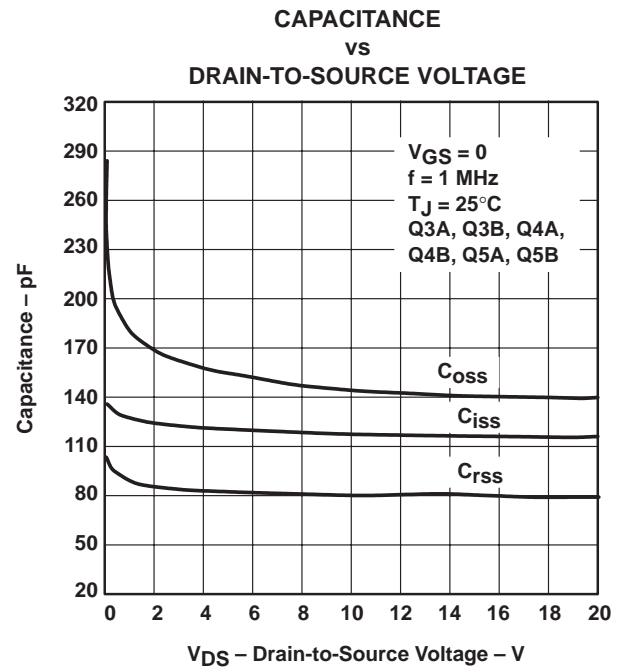


Figure 18



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TYPICAL CHARACTERISTICS

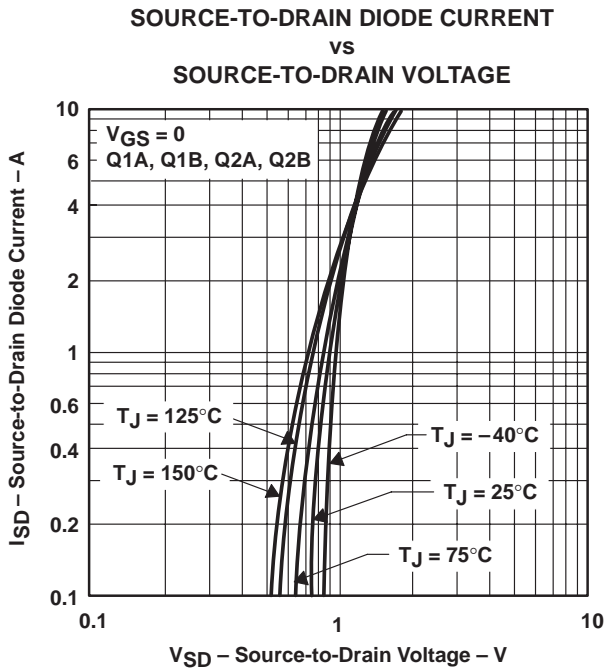


Figure 19

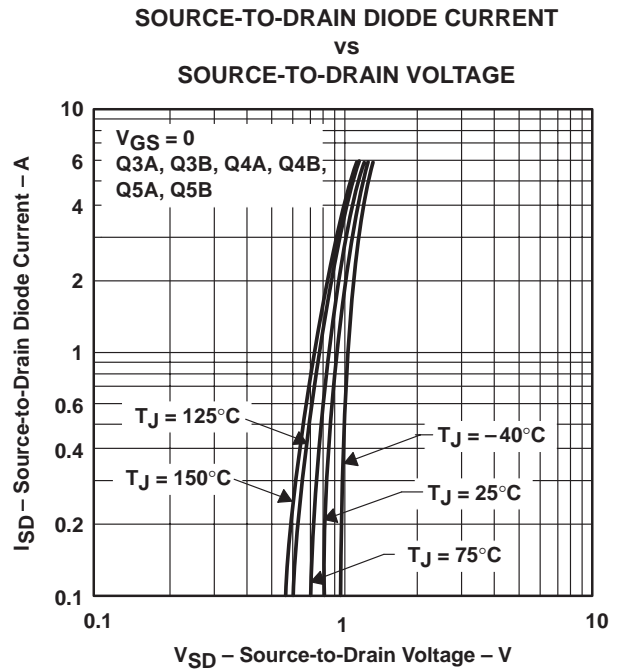


Figure 20

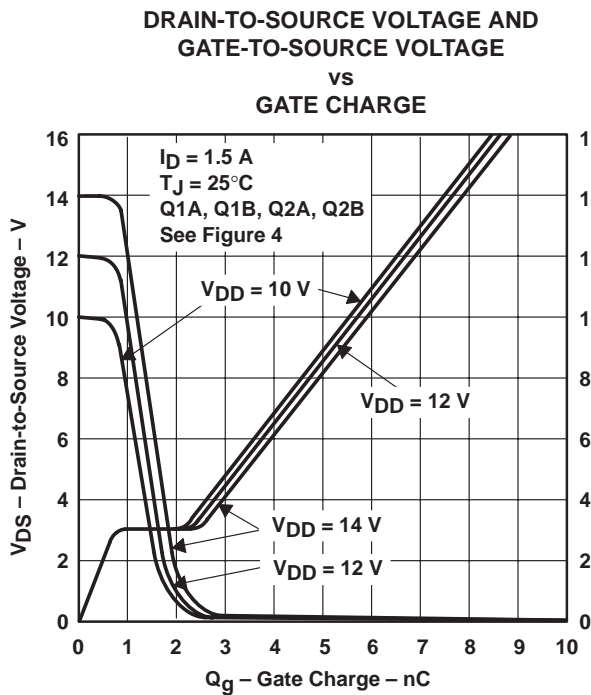


Figure 21

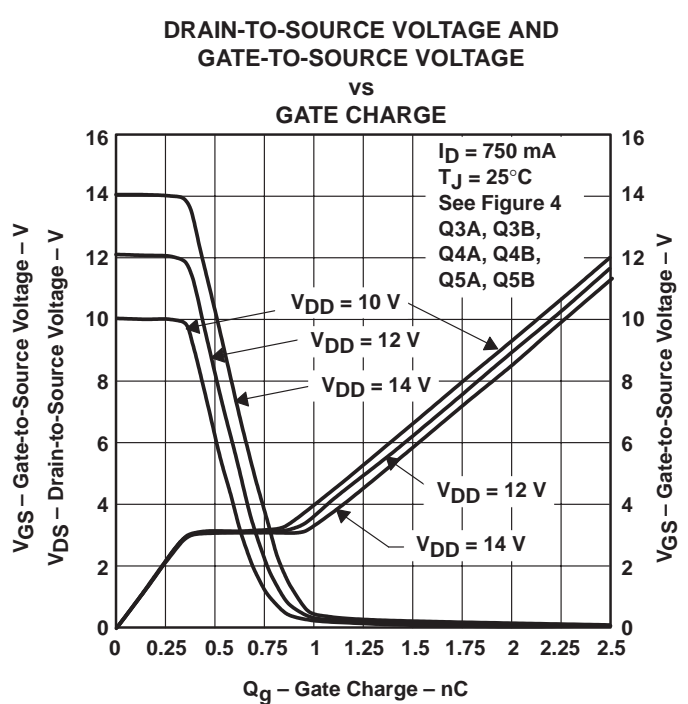


Figure 22

# TPIC1533 QUAD AND HEX POWER DMOS ARRAY

SLIS064 – OCTOBER 1996

## TYPICAL CHARACTERISTICS

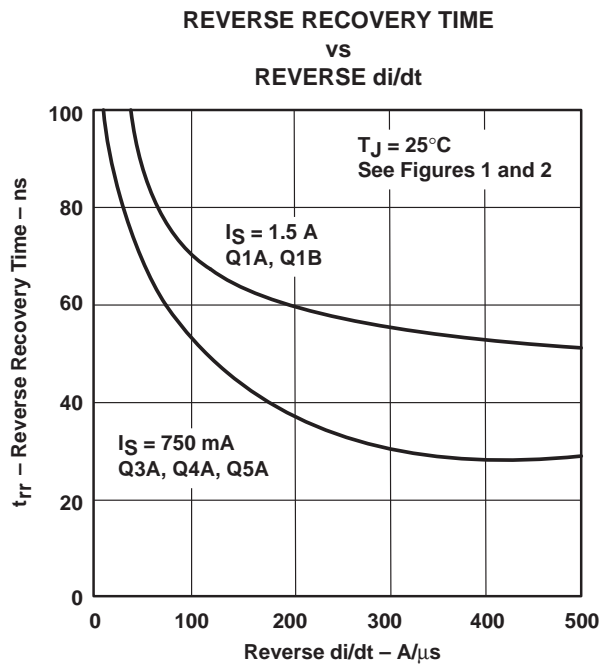


Figure 23

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT  
 vs  
 DRAIN-TO-SOURCE VOLTAGE

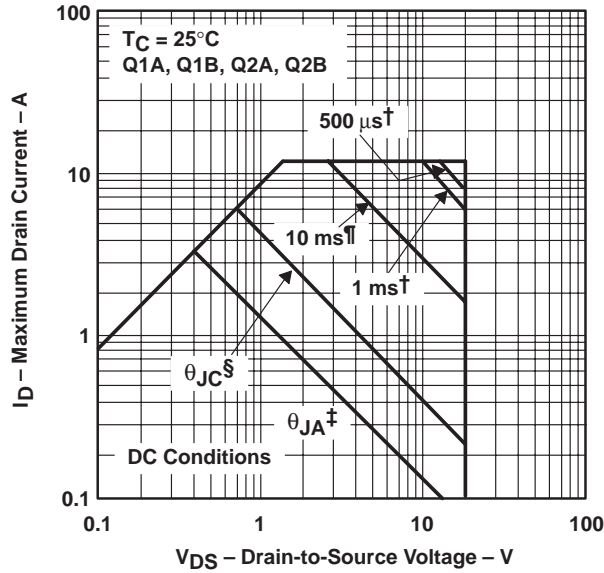


Figure 24

MAXIMUM DRAIN CURRENT  
 vs  
 DRAIN-TO-SOURCE VOLTAGE

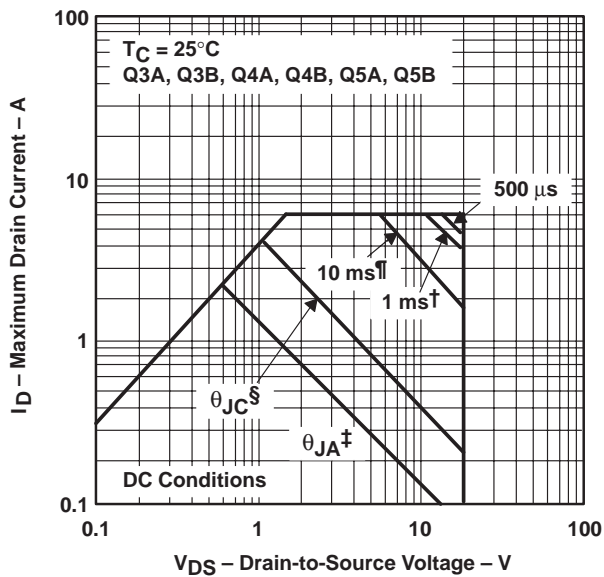


Figure 25

† Less than 10% duty cycle

‡ Device is mounted on FR4 printed-circuit board with no heat sink.

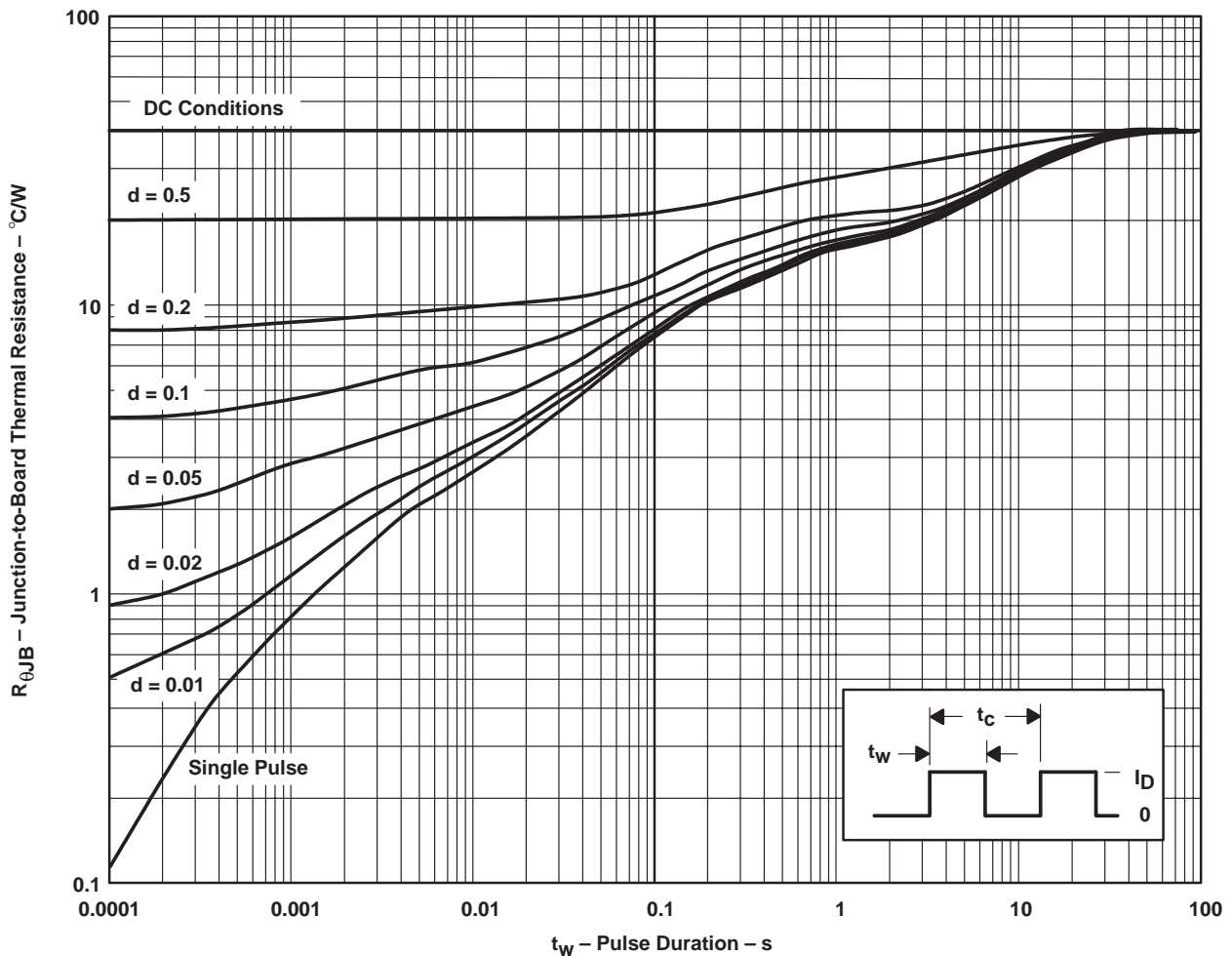
§ Device is mounted in intimate contact with infinite heat sink.

¶ Less than 2% duty cycle

# TPIC1533 QUAD AND HEX POWER DMOS ARRAY

SLIS064 – OCTOBER 1996

## THERMAL INFORMATION DW PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE VS PULSE DURATION



† Device mounted on 24 in<sup>2</sup>, 4 layer FR4 printed-circuit board with no heat sink.

NOTE A:  $Z_{\theta B}(t) = r(t) R_{\theta JB}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 26



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