

TPIC1502 QUAD AND HEX POWER DMOS ARRAY

SLIS054 – OCTOBER 1996

- Low $r_{DS(on)}$:
0.25 Ω Typ (Full H-Bridge)
0.4 Ω Typ (Triple Half H-Bridge)
- Pulsed Current . . . 4 A Per Channel
- Matched Sense Transistors for Class A-B Linear Operation
- Fast Commutation Speed

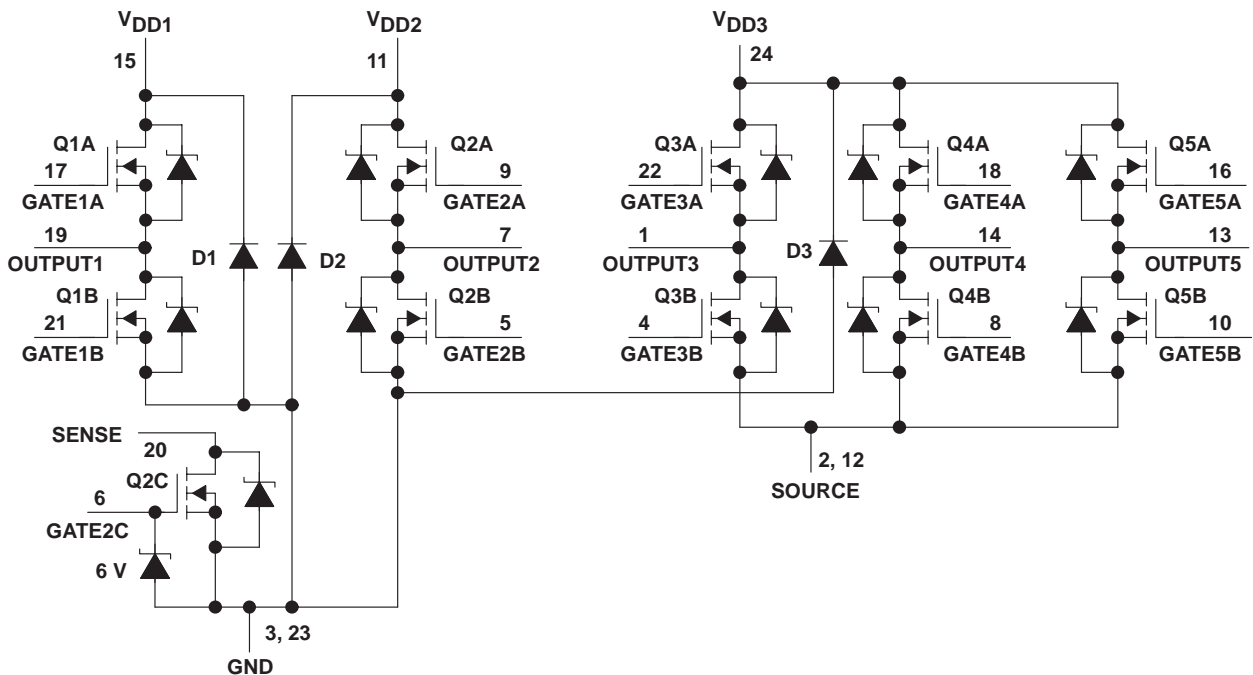
description

The TPIC1502 is a monolithic power DMOS array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge is provided with an integrated sense-FET to allow biasing of the bridge in class A-B operation.

The TPIC1502 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of -40°C to 125°C .

DW PACKAGE (TOP VIEW)			
OUTPUT3	1	24	V _{DD3}
SOURCE	2	23	GND
GND	3	22	GATE3A
GATE3B	4	21	GATE1B
GATE2B	5	20	SENSE
GATE2C	6	19	OUTPUT1
OUTPUT2	7	18	GATE4A
GATE4B	8	17	GATE1A
GATE2A	9	16	GATE5A
GATE5B	10	15	V _{DD1}
V _{DD2}	11	14	OUTPUT4
SOURCE	12	13	OUTPUT5

schematic



- NOTES: A. Terminals 3 and 23 must be externally connected.
B. Terminals 2 and 12 must be externally connected.
C. No output may be taken greater than 0.5 V below GND.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TPIC1502

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absolute maximum ratings, $T_C = 25^\circ\text{C}$ (unless otherwise noted)†

Supply-to-GND voltage	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A)	20 V
Output-to-GND voltage	20 V
Sense-to-GND voltage	20 V
Gate-to-source voltage range, V_{GS} (Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	± 20 V
Gate-to-source voltage, V_{GS} (Q2C)	-0.7 V to 6 V
Continuous gate-to-source zener-diode current (Q2C)	± 10 mA
Pulsed gate-to-source zener-diode current (Q2C)	± 50 mA
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous drain current (Q2C)	5 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1.5 A
Continuous source-to-drain diode current (Q2C)	5 mA
Pulsed drain current, each output, I_{max} (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24)	4 A
Pulsed drain current, each output, I_{max} (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25)	4 A
Pulsed drain current, each output, I_{max} (Q2C) (see Note 1)	20 mA
Continuous total power dissipation, $T_C = 70^\circ\text{C}$ (see Note 2 and Figures 24 and 25)	2.86 W
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Pulse duration = 10 ms, duty cycle = 2%
 2. Package mounted in intimate contact with infinite heat sink.



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electrical characteristics, Q1A, Q1B, Q2A, Q2B, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5	1.5	1.85	2.2	V
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	$I_D = 1\ \text{mA}$, $V_{DS} = V_{GS}$			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = $250\ \mu\text{A}$ (D1, D2)	20			V
$V_{(BR)GS}$	Gate-to-source breakdown voltage, Q2C	$I_{GS} = 100\ \mu\text{A}$	6			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage, Q2C	$I_{GS} = 100\ \mu\text{A}$	0.7			V
$V_{(DS)on}$	Drain-to-source on-state voltage	$I_D = 1.5\ \text{A}$, $V_{GS} = 10\ \text{V}$, See Notes 3 and 4		0.375	0.45	V
V_F	Forward on-state voltage, GND-to- V_{DD1} , GND-to- V_{DD2}	$I_D = 1.5\ \text{A}$ (D1, D2) See Notes 3 and 4		1.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1.5\ \text{A}$, $V_{GS} = 0$, See Notes 3 and 4 and Figure 19		0.93	1.2	V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 16\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	μA
			$T_C = 125^\circ\text{C}$	0.5	10	
I_{GSSF}	Forward gate current, drain short-circuited to source	$V_{GS} = 16\ \text{V}$, $V_{DS} = 0$		10	100	nA
I_{GSSR}	Reverse gate current, drain short-circuited to source	$V_{SG} = 16\ \text{V}$, $V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, V_{DD1} -to-GND, V_{DD2} -to-GND, gate shorted to source	$V_{DGND} = 16\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1	μA
			$T_C = 125^\circ\text{C}$	0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$, $I_D = 1.5\ \text{A}$, See Notes 3 and 4 and Figure 9	$T_C = 25^\circ\text{C}$	0.25	0.3	Ω
			$T_C = 125^\circ\text{C}$	0.38	0.51	
g_{fs}	Forward transconductance	$V_{DS} = 14\ \text{V}$, $I_D = 750\ \text{mA}$, See Notes 3 and 4 and Figure 13	0.75	1.2		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 14\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$, See Figure 17		98		μF
C_{oss}	Short-circuit output capacitance, common source			70		
C_{rss}	Short-circuit reverse transfer capacitance, common source			54		
α_S	Sense-FET drain current ratio	$V_{DS} = 6\ \text{V}$, $I_D(Q2B) = 1.5\ \text{mA}$	100	150	200	

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, Q1A, Q2A, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 750\ \text{mA}$, $V_{GS} = 0$, $V_{DS} = 14\ \text{V}$, $di/dt = 100\ \text{A}/\mu\text{s}$,		18		ns
Q_{RR}	Total diode charge	See Figures 1 and 23		14		nC



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resistive-load switching characteristics, Q1A, Q1B, Q2A, Q2B, T_C = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d(on)} Turn-on delay time	V _{DD} = 14 V, R _L = 18.7 Ω, t _{en} = 10 ns, t _{dis} = 10 ns, See Figure 3		12		ns
t _{d(off)} Turn-off delay time			13		
t _r Rise time			2.2		
t _f Fall time			6		
Q _g Total gate charge	V _{DS} = 14 V, I _D = 750 mA, V _{GS} = 10 V, See Figure 4 and Figure 21		1.7	2.1	nC
Q _{gs(th)} Threshold gate-to-source charge			0.3	0.4	
Q _{gd} Gate-to-drain charge			0.4	0.5	
L _D Internal drain inductance			7		nH
L _S Internal source inductance			7		
R _g Internal gate resistance			0.25		Ω

electrical characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T_C = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{(BR)DSX} Drain-to-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	20			V
V _{GS(th)} Gate-to-source threshold voltage	I _D = 1 mA, V _{DS} = V _{GS} , See Figure 6	1.5	1.85	2.2	V
V _(BR) Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 μA (D3)	20			V
V _{(DS)on} Drain-to-source on-state voltage	I _D = 1.5 A, V _{GS} = 10 V, See Notes 3 and 4		0.6	0.75	V
V _F Forward on-state voltage, GND-to-V _{DD3}	I _D = 1.5 A (D3), See Notes 3 and 4		1.5		V
V _{F(SD)} Forward on-state voltage, source-to-drain	I _S = 1.5 A, V _{GS} = 0 See Notes 3 and 4 and Figure 20		1	1.2	V
I _{DSS} Zero-gate-voltage drain current	V _{DS} = 16 V, V _{GS} = 0		0.05	1	μA
	T _C = 25°C				
	T _C = 125°C		0.5	10	
I _{GSSF} Forward gate current, drain short-circuited to source	V _{GS} = 16 V, V _{DS} = 0		10	100	nA
I _{GSSR} Reverse gate current, drain short-circuited to source	V _{SG} = 16 V, V _{DS} = 0		10	100	nA
I _{lkg} Leakage current, V _{DD3} -to-GND, gate shorted to source	V _{DGND} = 16 V		0.05	1	μA
	T _C = 25°C				
	T _C = 125°C		0.5	10	
r _{DS(on)} Static drain-to-source on-state resistance	V _{GS} = 10 V, I _D = 1.5 A, See Notes 3 and 4 and Figure 10		0.4	0.5	Ω
	T _C = 125°C		0.61	0.85	
g _{fs} Forward transconductance	V _{DS} = 14 V, I _D = 750 mA, See Notes 3 and 4 and Figure 14	0.4	0.74		S
C _{iss} Short-circuit input capacitance, common source	V _{DS} = 14 V, V _{GS} = 0, f = 1 MHz, See Figure 18		73		pF
C _{OSS} Short-circuit output capacitance, common source			65		
C _{rss} Short-circuit reverse transfer capacitance, common source			43		

NOTES: 3: Technique should limit T_J – T_C to 10°C maximum.

4: These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



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source-to-drain diode characteristics, Q3A, Q4A, Q5A, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 750\text{ mA}$, $V_{DS} = 14\text{ V}$, See Figures 2 and 23		26		ns
Q_{RR}	Total diode charge					

resistive-load switching characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 14\text{ V}$, $R_L = 18.7\ \Omega$, $t_{dis} = 10\text{ ns}$, See Figure 3		13		ns
$t_{d(off)}$	Turn-off delay time			13		
t_r	Rise time			3		
t_f	Fall time			7		
Q_g	Total gate charge	$V_{DS} = 14\text{ V}$, See Figure 4 and Figure 22		1	1.3	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.2	0.25	
Q_{gd}	Gate-to-drain charge			0.2	0.25	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		
R_g	Internal gate resistance			0.25		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 5 and 8		90		$^\circ\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 6 and 8		52		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 7 and 8		28		

- NOTES: 5. Package mounted on a FR4 printed-circuit board with no heatsink.
6. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
7. Package mounted in intimate contact with infinite heatsink.
8. All outputs with equal power



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PARAMETER MEASUREMENT INFORMATION

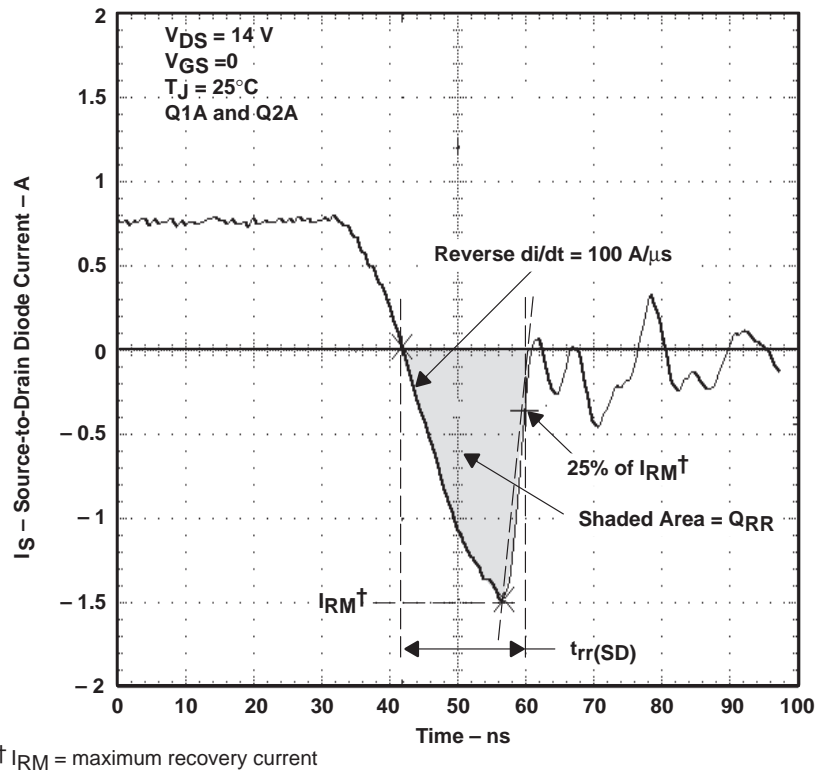
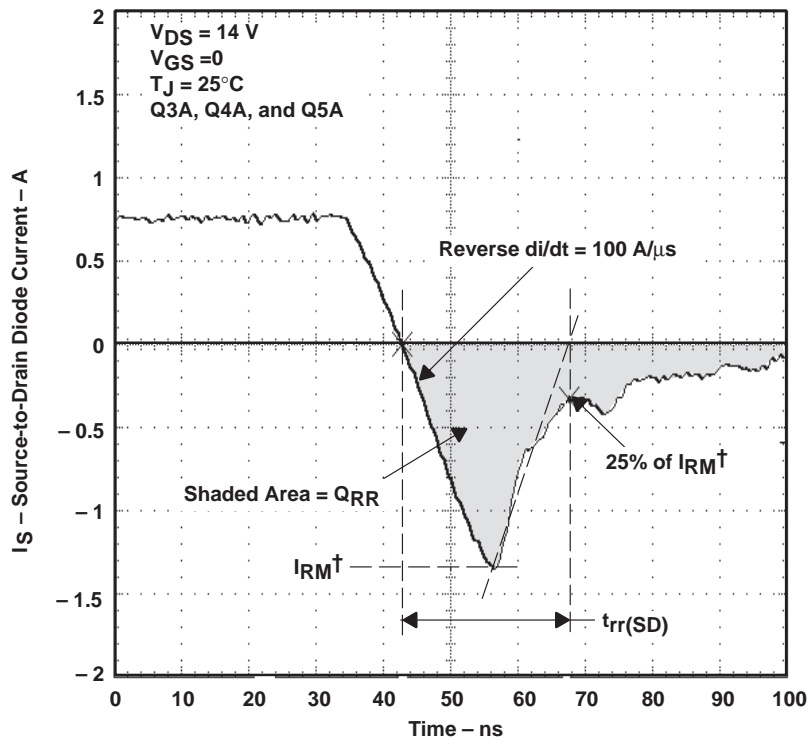


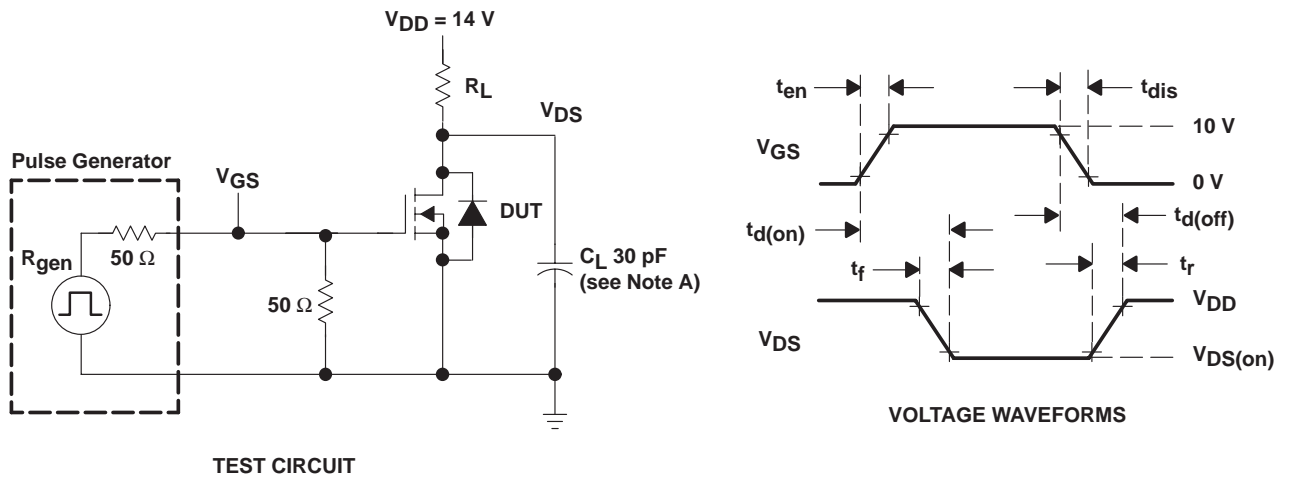
Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes

PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$ = maximum recovery current

Figure 2. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Resistive-Switching Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

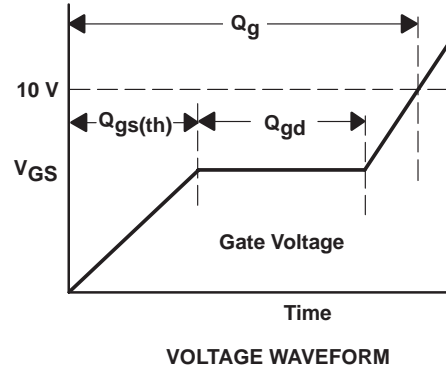
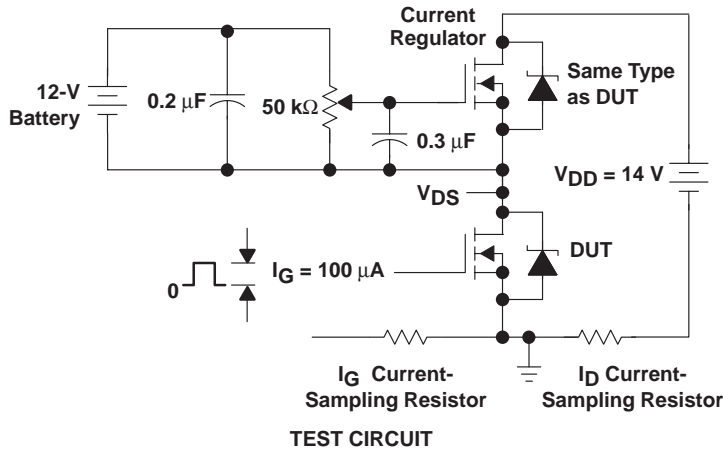


Figure 4. Gate-Charge Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

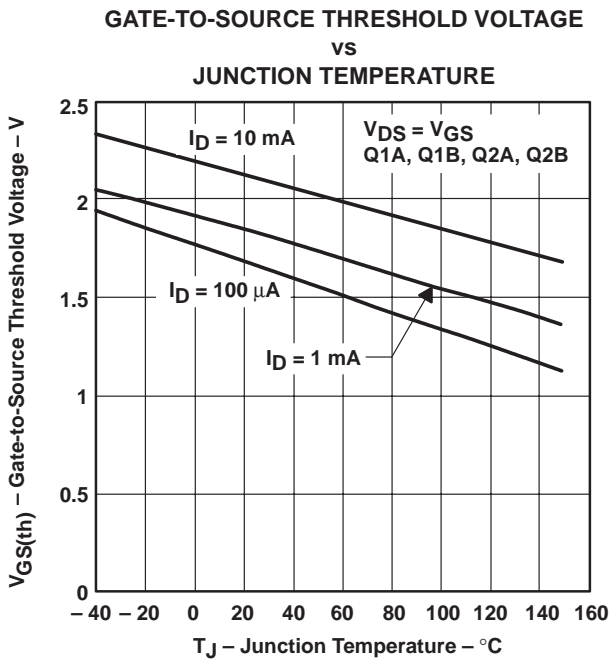


Figure 5

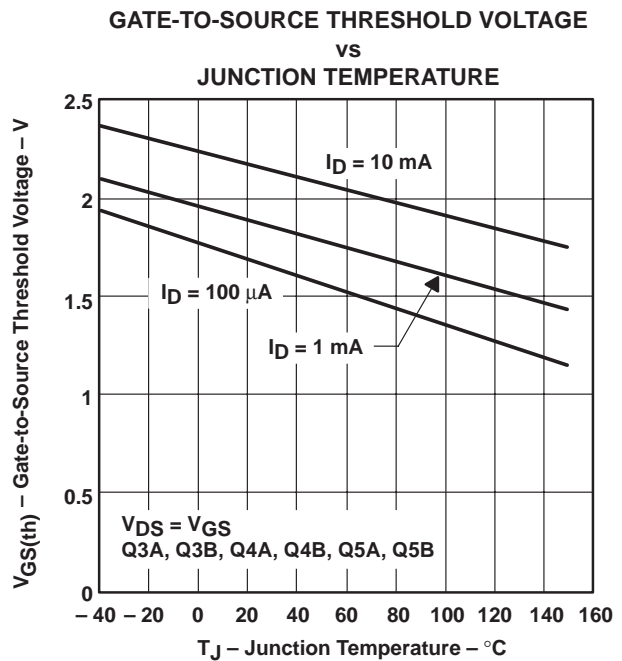


Figure 6

TYPICAL CHARACTERISTICS

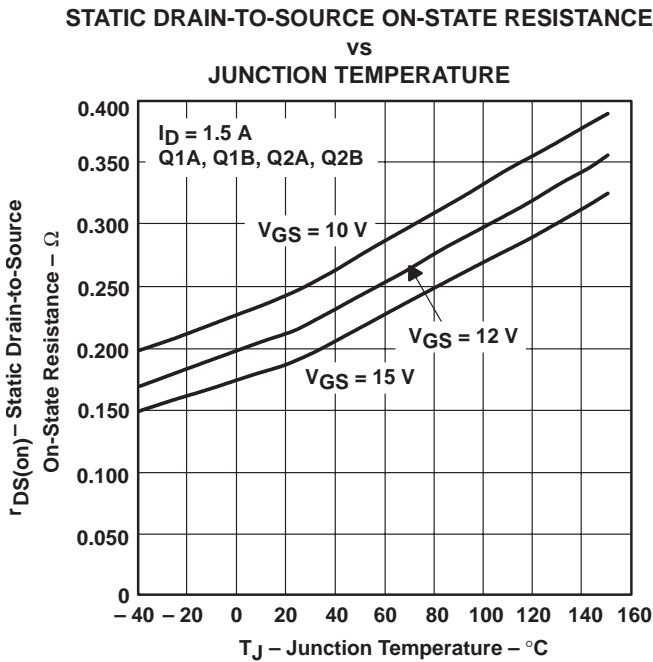


Figure 7

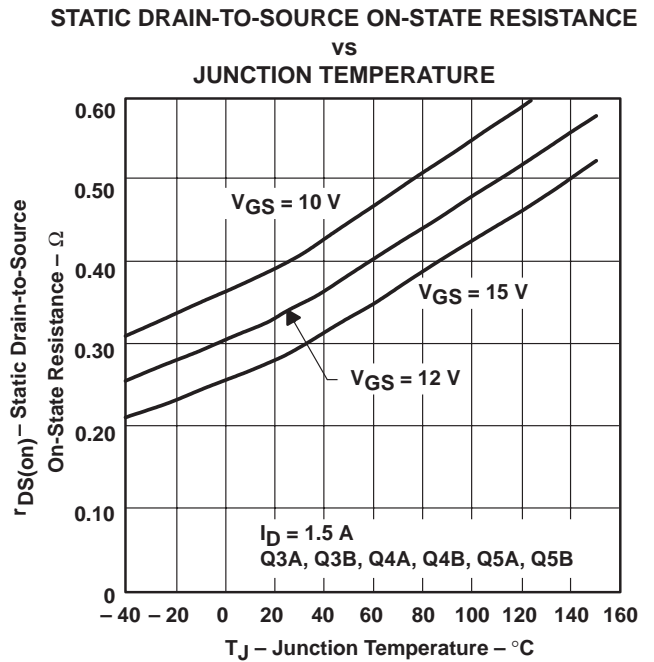


Figure 8

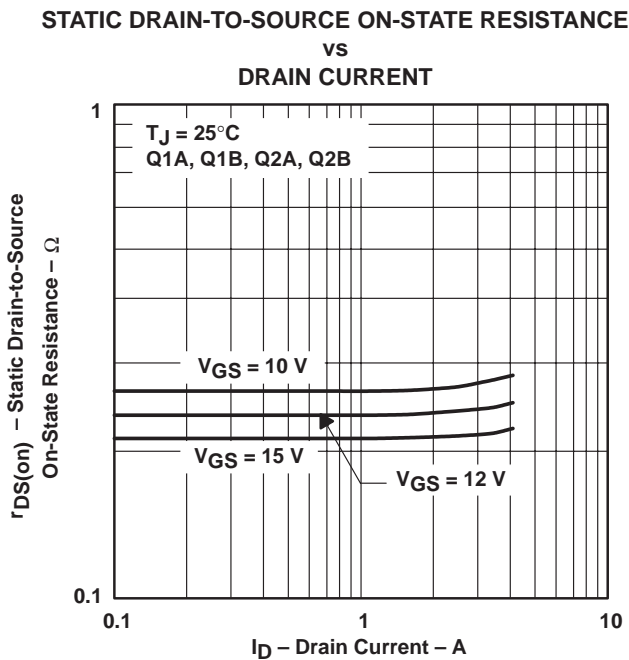


Figure 9

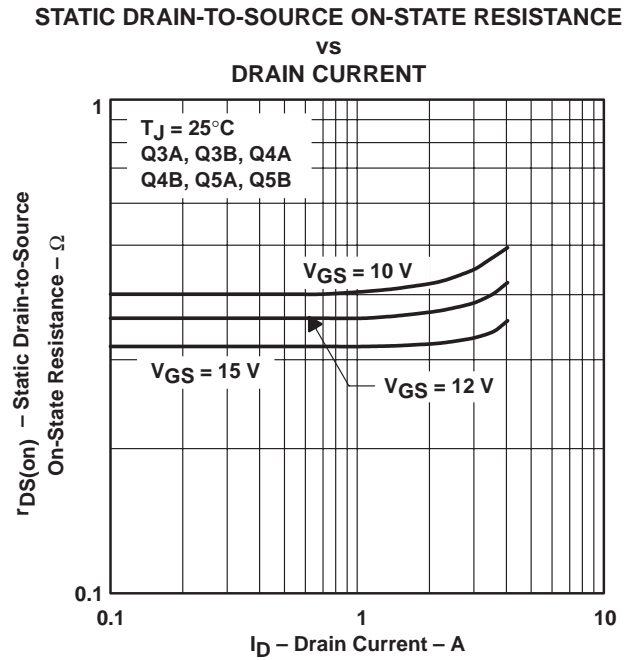


Figure 10

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TYPICAL CHARACTERISTICS

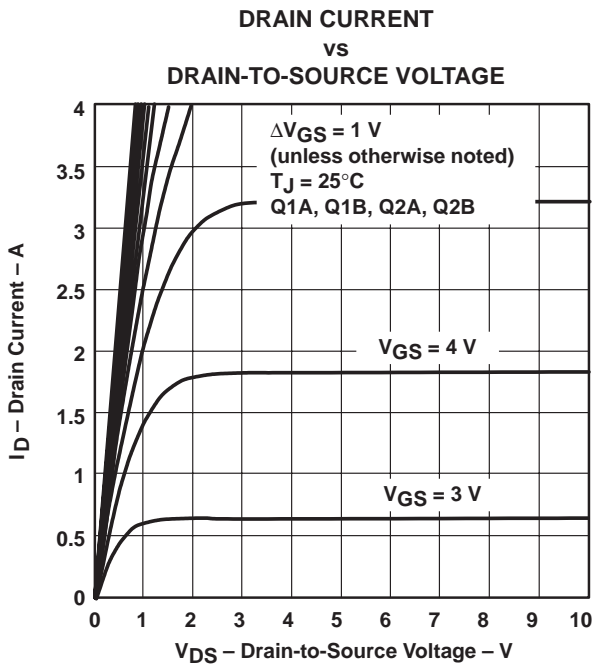


Figure 11

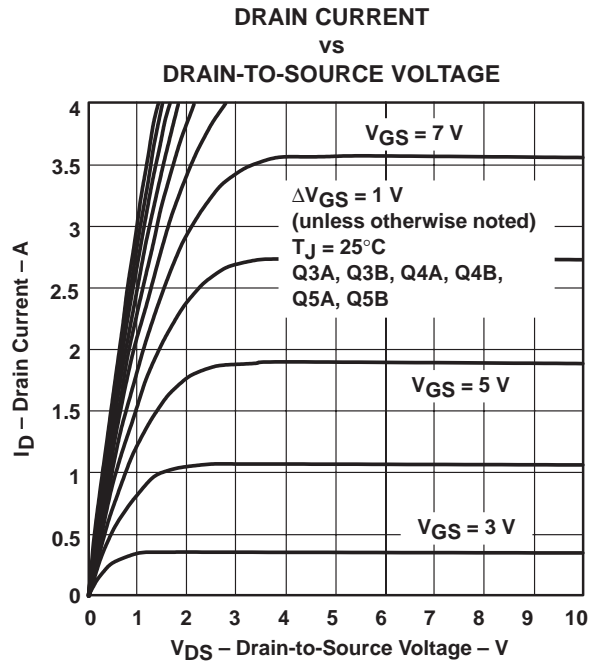


Figure 12

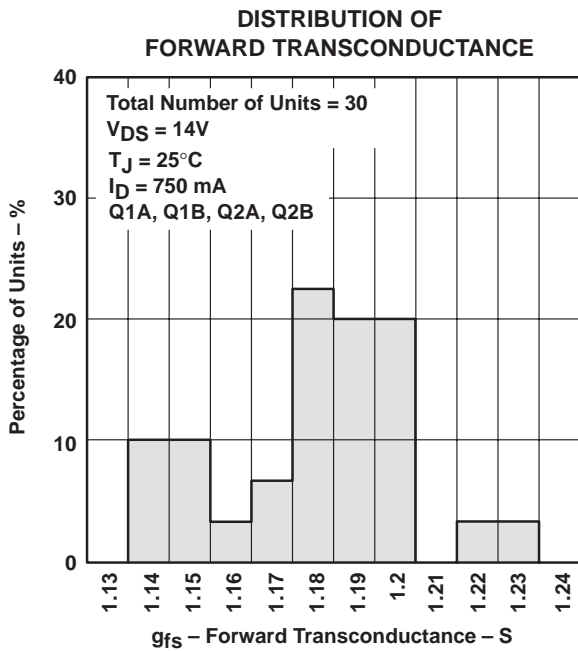


Figure 13

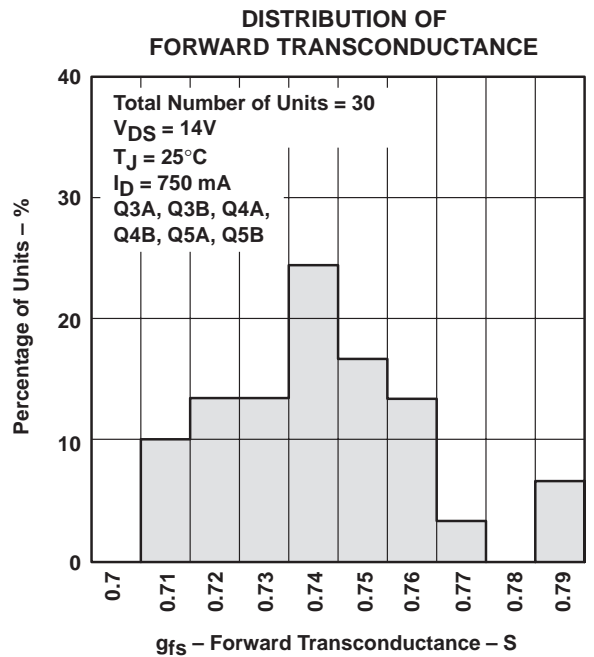


Figure 14

TYPICAL CHARACTERISTICS

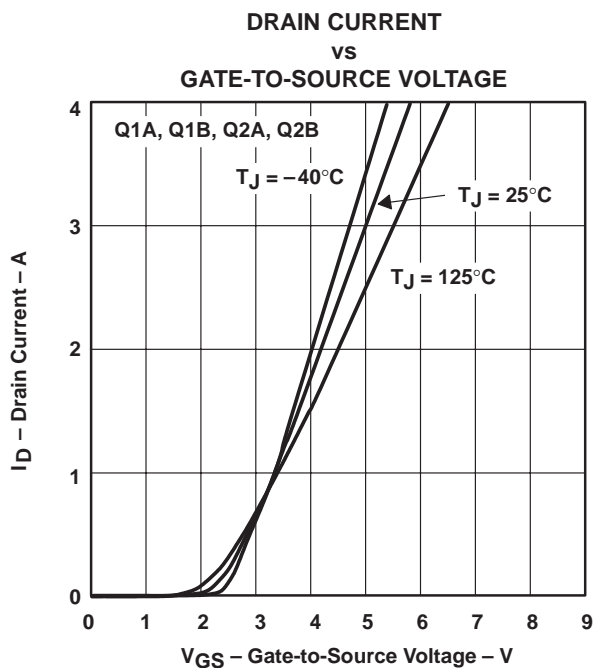


Figure 15

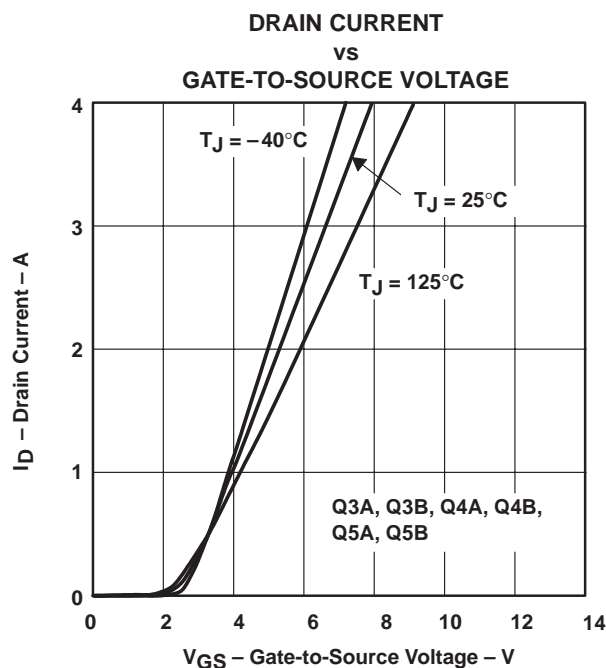


Figure 16

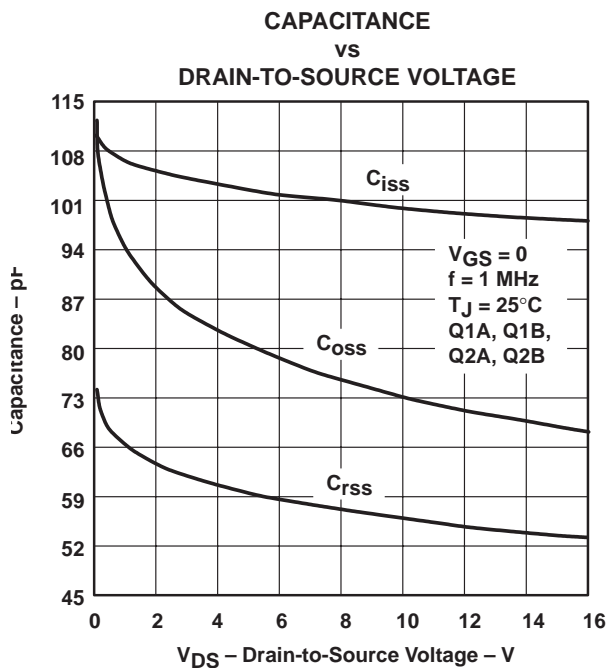


Figure 17

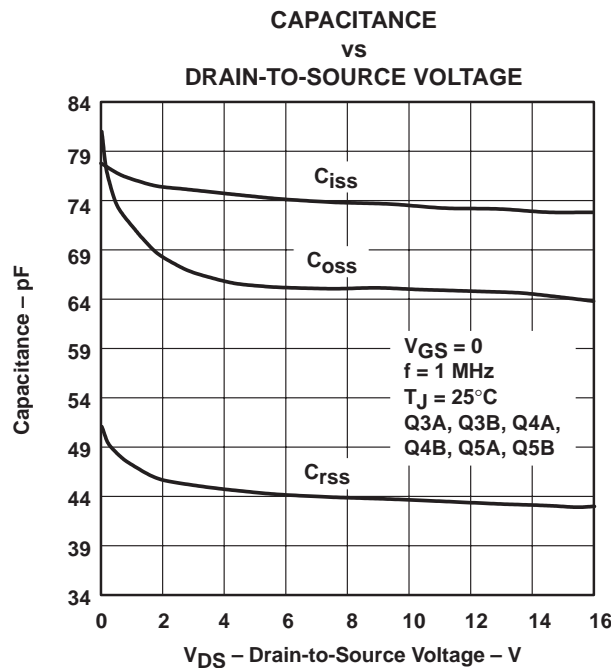


Figure 18

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TYPICAL CHARACTERISTICS

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

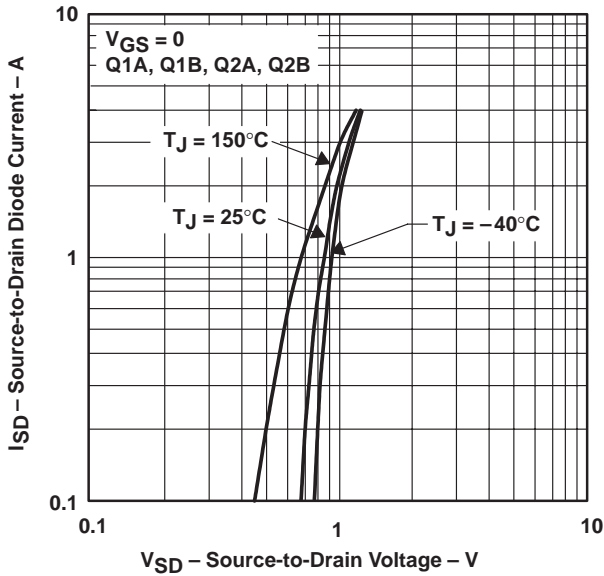


Figure 19

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

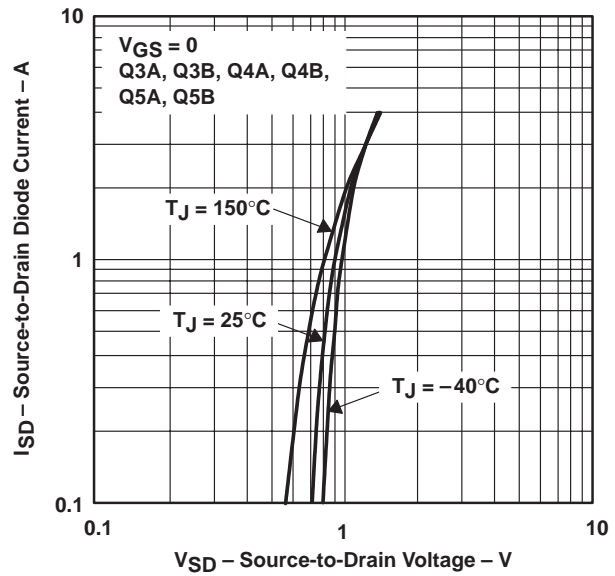


Figure 20

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

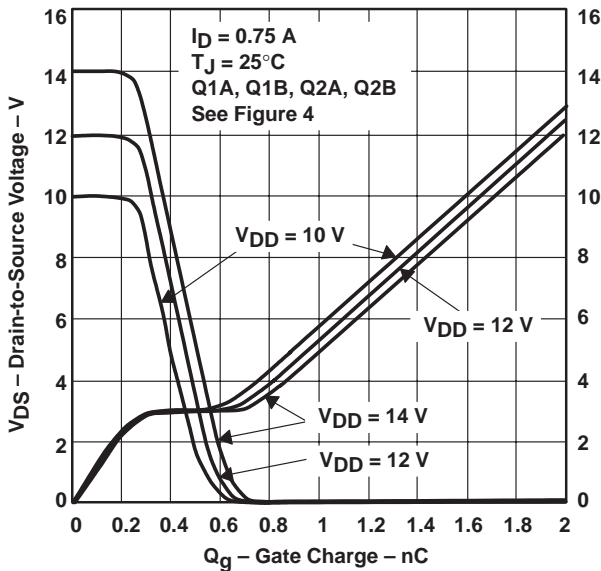


Figure 21

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

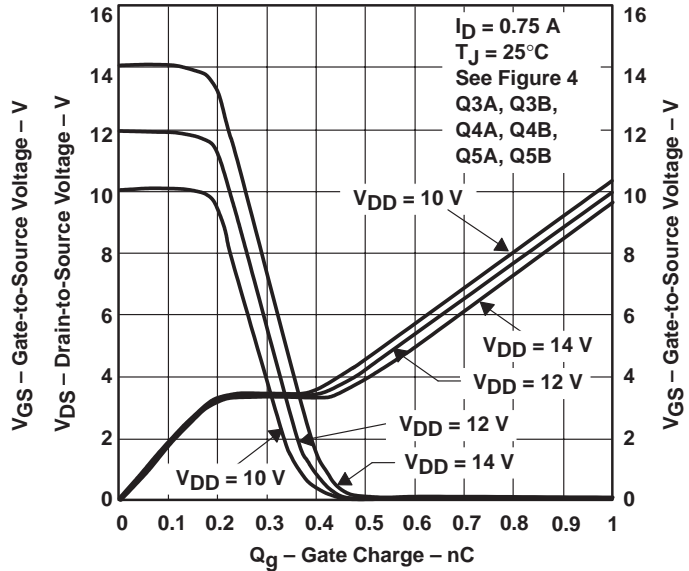


Figure 22



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TYPICAL CHARACTERISTICS

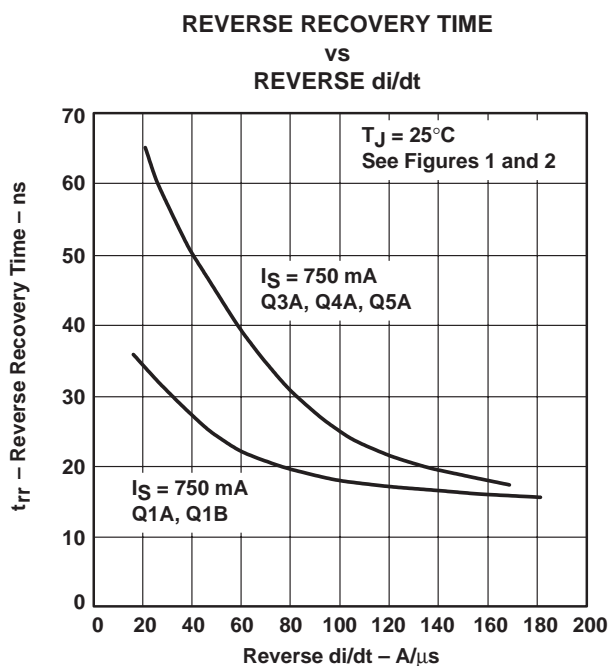


Figure 23

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THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

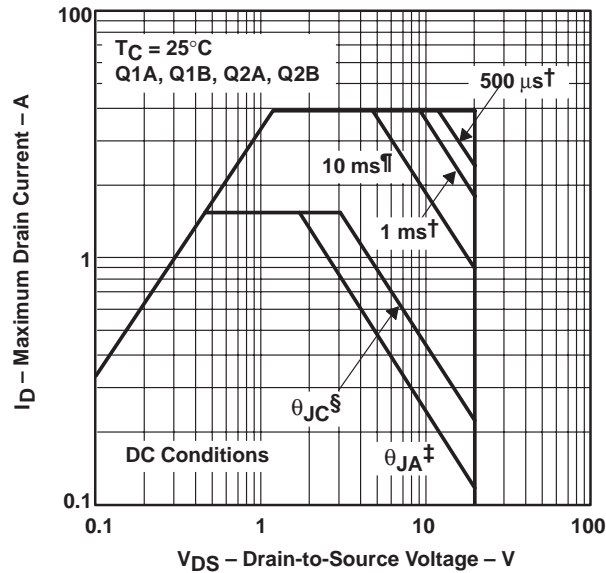


Figure 24

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

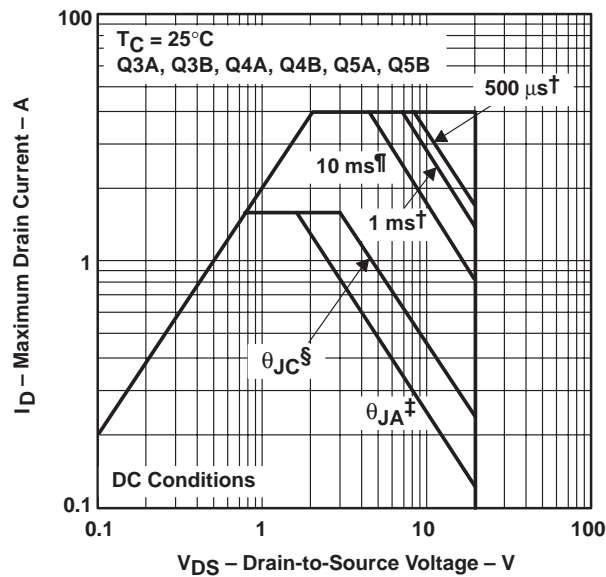


Figure 25

† Less than 10% duty cycle

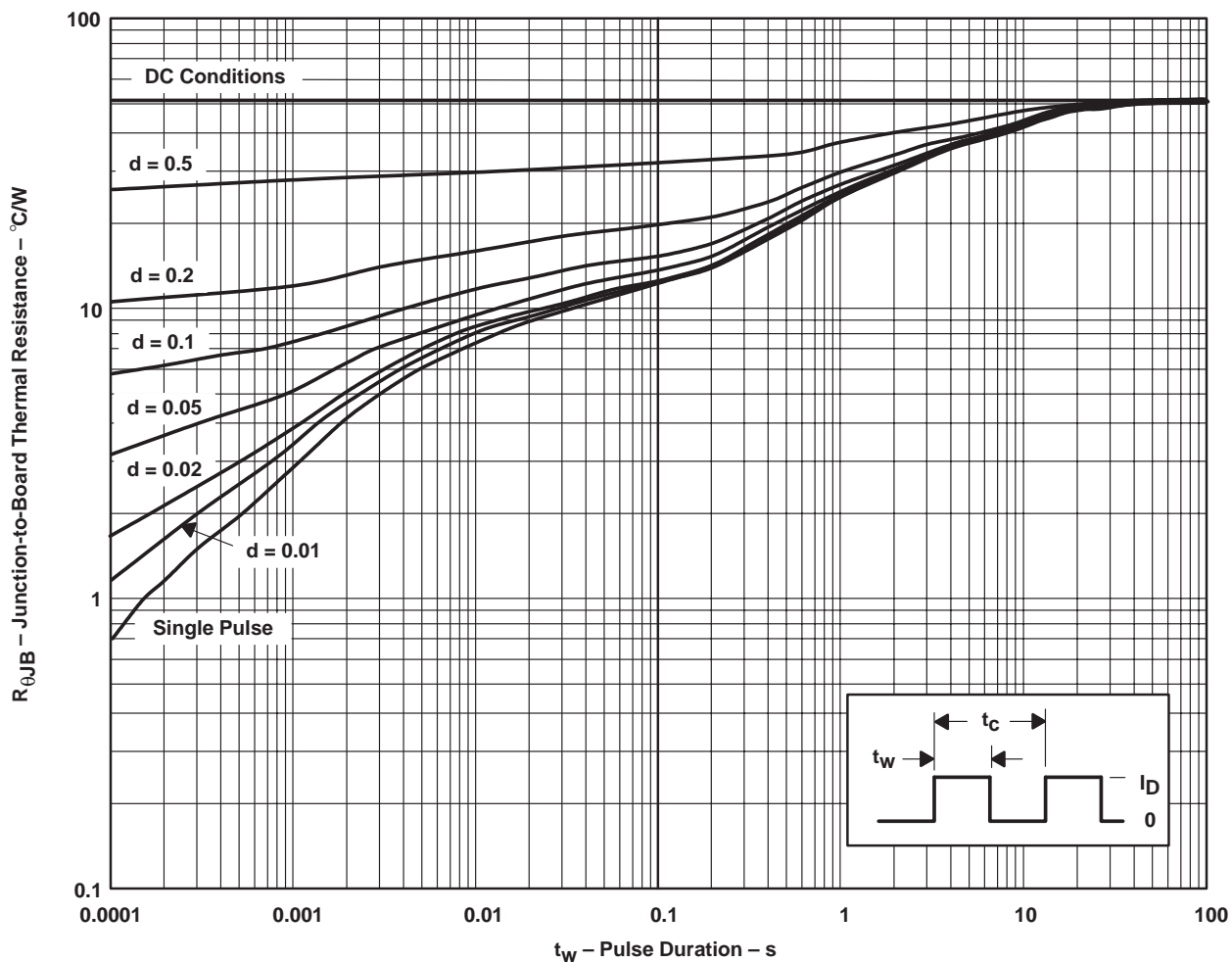
‡ Device is mounted on a 24 in², 4 layer FR4 printed-circuit board.

§ Device is mounted in intimate contact with infinite heatsink.

†† Less than 2% duty cycle

THERMAL INFORMATION

DW PACKAGE†
 JUNCTION-TO-BOARD THERMAL RESISTANCE
 VS
 PULSE DURATION



† Device is mounted on 24 in², 4-layer FR4 printed circuit board with no heat sink.

NOTE A: $Z_{\theta B}(t) = r(t) R_{\theta JB}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

Figure 26

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