Octal Line Receiver

FEATURES

- Meets EIA232E/423A/422A and CCITT V.10, V.11, V.28, X.26, X.27
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35mA Max
- Internal Hysteresis

DESCRIPTION

The UC5181C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA422A, EIA423A and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5181C is similar to the UC5180C, but without the input filtering. Thus, it covers the entire range of data rates up to 10MBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

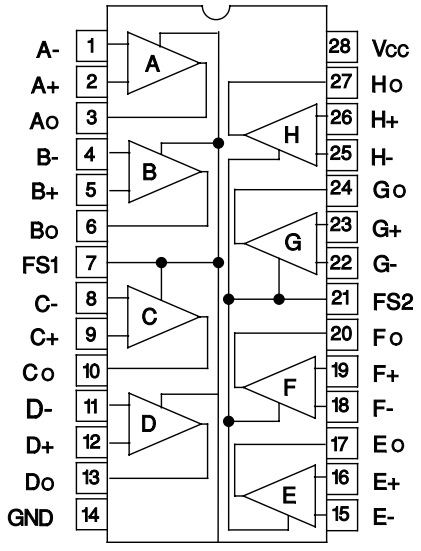
Supply Voltage, V_{CC} 7V
Output Sink Current. 50mA
Output Short Circuit Time . . . . . 1 Sec
Common Mode Input Range 15V
Differential Input Range 25V
Failsafe Voltage. . . . . -0.3 to V_{CC}
PLCC Power Dissipation, T_A=25° C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, T_A=25° C (Note 2) . . . . . 1200 mW
Storage Temperature Range . . . . . -65° C to +150° C
Lead Temperature (Soldering, 10 seconds) . . . . . -300° C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive in, negative out of the specified terminal.

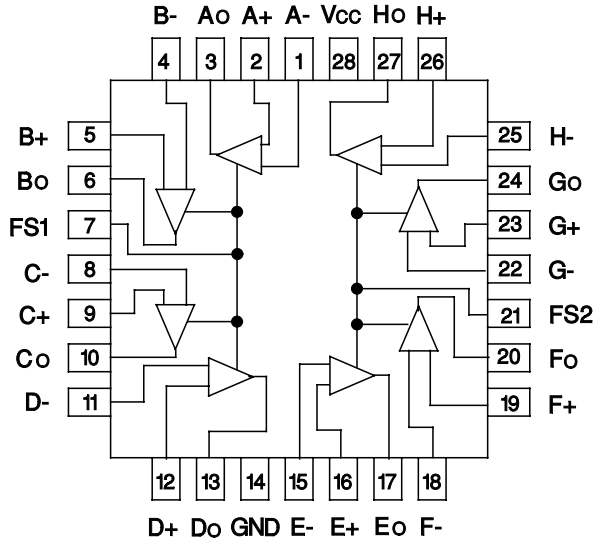
Note 2: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V, T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS		UC5181C MIN	UC5181C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ |V_{IN}|≤25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0≥I_{OUT}≤8mA$V_{FAILSAFE}$=0V		0.45	V
			0≥I_{OUT}≥-400µA, $V_{FAILSAFE}$=V_{CC}	2.7		
Differential Input High Threshold	V_{TL}	V_{OUT}= 0.45V, I_{OUT} = -440µA (See Figure 1)	R_S = 0 (Note3)	50	200	mV
			R_S = 500 (Note 3)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 3)	-200	-50	mV
			R_S = 500 (Note 3)	-400		
Hysteresis	V_H	F_S=0V or V_{CC} (See Figure 1)		45	140	mV
Open Circuit Input Voltage	V_{IOC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, I_{OUT} = -440 µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 4)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 5		20	100	mA
Supply current	I_{CC}	4.75V ≤V_{CC}≤5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IH} = -10V	-3.25		

Note 3: Rs is a resistor in series with each input.
Note 4: Measure after 100 ms warm up (at 0°C).
Note 5: Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
Note 6: The delays, either t_{PLH} or t_{PHL}, shall not vary from receiver to receiver by more than 35ns.

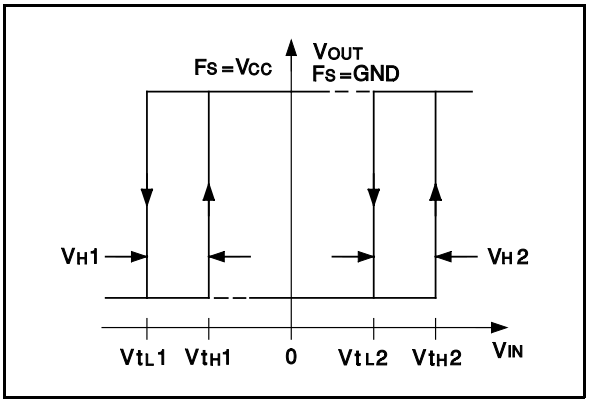


Figure 1. VTL, VTH,VH Definition

AC ELECTRICAL CHARACTERISTICS: V_{CC}=5V ±5%. T_A=0°C to +70°C, Figure 2 T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS	UC5181C MIN	UC5181C MAX	UNITS
Propagation Delay–Low to High	t_{PLH}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Propagation Delay–High to Low	t_{PHL}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Acceptable Input frequency	f_A	Unused Input Grounded, V_{IN}= ±200 mV		5.0	MHz

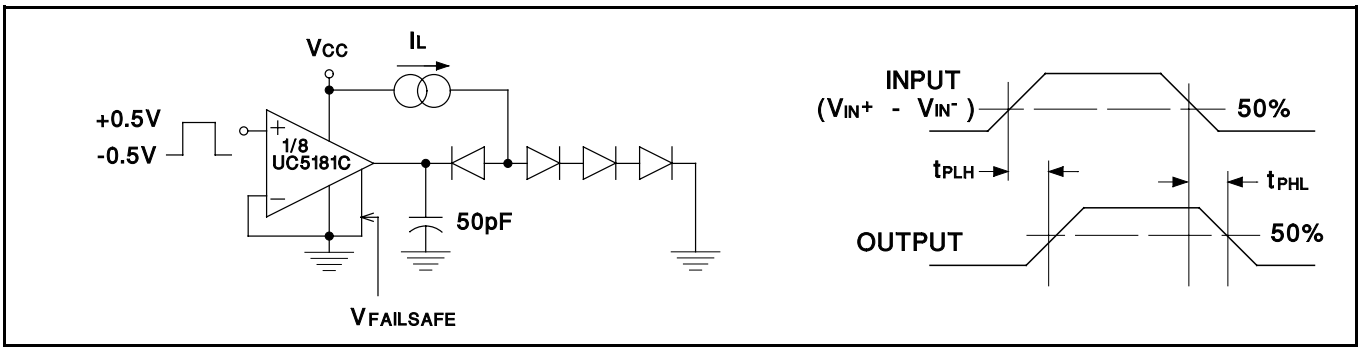


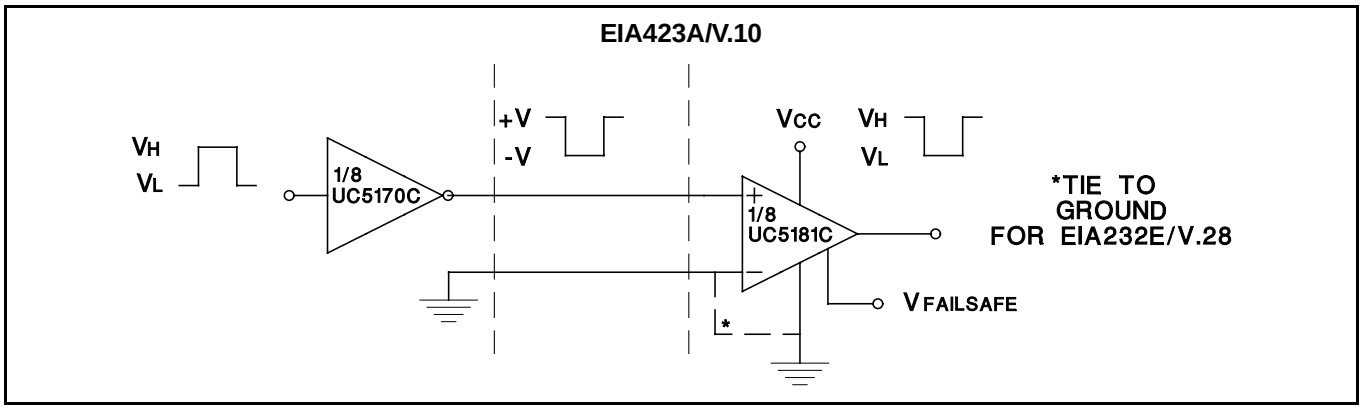
Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

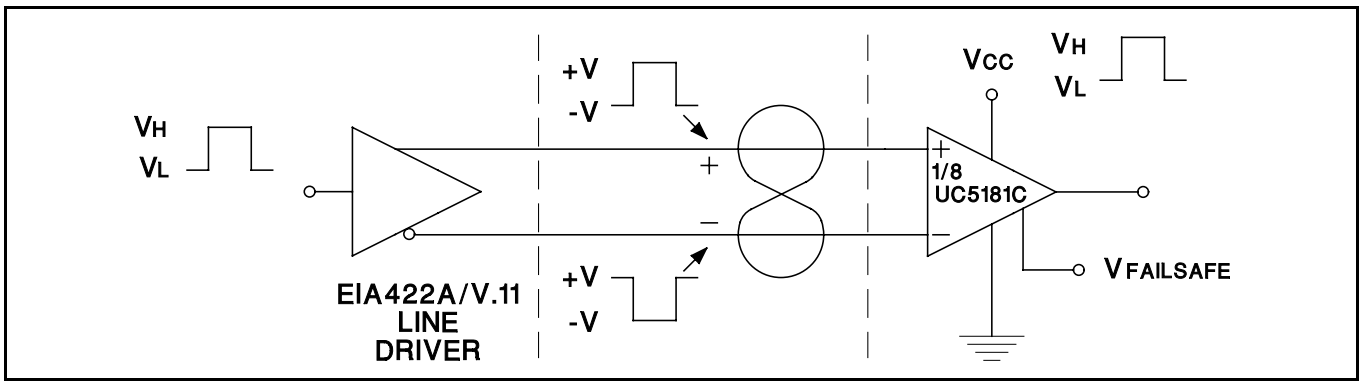
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides a logic “1" output under fault conditions, while a connection to ground provides a logic ”0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5181C where each provides common failsafe control for four receivers.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, and protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5180C and the UC5181C is P6KE22CA.

* Transzorb is a trademark of General Semiconductor Industries.

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