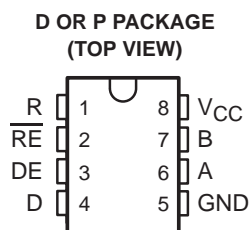


- Bidirectional Transceiver
- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements . . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal-Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 k Ω Min
- Receiver Input Sensitivity . . . ± 200 mV Max
- Receiver Input Hysteresis . . . 120 mV Typ
- Fail Safe . . . High Receiver Output With Inputs Open
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Interchangeable With National DS3695 and DS3695A



description

The TL3695 differential bus transceiver is designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

The TL3695 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TL3695D	TL3695P

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL3695DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

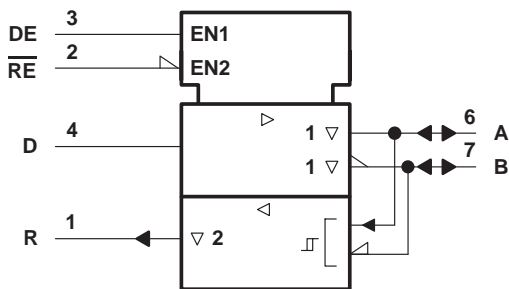
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

RECEIVER

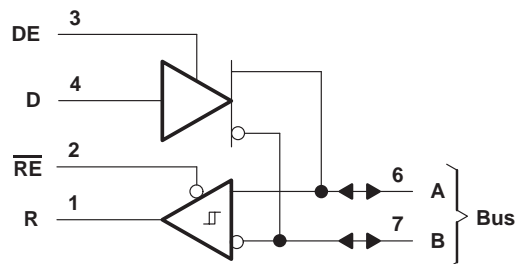
DIFFERENTIAL INPUTS A – B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TL3695

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recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V_{CC}		4.75	5	5.25	V	
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		12			V	
		-7				
High-level Input voltage, V_{IH}	D, DE, and \overline{RE}	2			V	
Low-level Input voltage, V_{IL}	D, DE, and \overline{RE}	0.8			V	
Differential input voltage, V_{ID} (see Note 3)		±12			V	
High-level output current, I_{OH}	Driver	-60			mA	
	Receiver	-400			μA	
Low-level output current, I_{OL}	Driver	60			mA	
	Receiver	8				
Operating free-air temperature, T_A		0			70	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V
V _O	Output voltage	I _O = 0		0		6	V
V _{OD1}	Differential output voltage	I _O = 0		1.5		5	V
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 1	1/2 V _{OD1} or 2§			V
		R _L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V _{OD3}	Differential output voltage	V _{test} = -7 V to 12 V, See Figure 2		1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 54 Ω, See Figure 1				±0.2	V
V _{OC}	Common-mode output voltage					3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage¶					±0.2	V
I _O	Output current	Output disabled, See Note 4	V _O = 12 V			1	mA
			V _O = -7 V			-0.8	
I _{IH}	High-level input current	V _I = 2.4 V				20	μA
I _{IL}	Low-level input current	V _I = 0.4 V				-200	μA
I _{OS}	Short-circuit output current#	V _O = -6 V				-250	mA
		V _O = 0				-150	
		V _O = V _{CC}				250	
		V _O = 8 V				250	
I _{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

¶ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
t _{d(OD)}	Differential-output delay time	C _{L1} = C _{L2} = 100 pF, R _L = 60 Ω, See Figure 3				8	22	ns
	Skew ((t _{d(ODH)} - t _{d(ODL)}))					1	8	ns
t _{t(OD)}	Differential output transition time					8	18	ns
t _{PZH}	Output enable time to high level	C _L = 100 pF,	R _L = 500 Ω,	See Figure 4		50	ns	
t _{PZL}	Output enable time to low level	C _L = 100 pF,	R _L = 500 Ω,	See Figure 5		50	ns	
t _{PHZ}	Output disable time from high level	C _L = 15 pF,	R _L = 500 Ω,	See Figure 4	8	30	ns	
t _{PLZ}	Output disable time from low level	C _L = 15 pF,	R _L = 500 Ω,	See Figure 5	8	30	ns	

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.



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SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7 V, I_O = -0.4 mA$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5 V, I_O = 8 mA$	$-0.2‡$			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	$V_{OC} = 0$		70		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18 mA$			-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200 mV$ or inputs open, $I_{OH} = -400 \mu A$, See Figure 6	2.4			V
V_{OL}	Low-level output voltage	$V_{ID} = -200 mV$, See Figure 6	$I_{OL} = 16 mA$		0.5	V
			$I_{OL} = 8 mA$		0.45	
I_{OZ}	High-impedance-state output current	$V_O = 0.4 V$ to $2.4 V$			± 20	μA
I_I	Line input current	Other input = 0, See Note 5	$V_I = 12 V$		1	mA
			$V_I = -7 V$		-0.8	
I_{IH}	High-level enable-input current	$V_{IH} = 2.7 V$			20	μA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4 V$			-100	μA
r_I	Input resistance			12		k Ω
I_{OS}	Short-circuit output current§	$V_O = 0$	-15		-85	mA
I_{CC}	Supply current	No load	Outputs enabled	23	50	mA
			Outputs disabled	19	35	

† All typical values are at $V_{CC} = 5 V$ and $T_A = 25^\circ C$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Duration of the short circuit should not exceed one second for this test.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.



switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 15 \text{ pF}$

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$,		14	37	ns
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 7		14	37	ns
t_{PZH}	Output enable time to high level	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level			7	20	ns
t_{PHZ}	Output disable time from high level	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level			8	16	ns

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

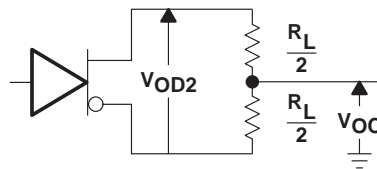


Figure 1. Driver V_{OD} and V_{OC}

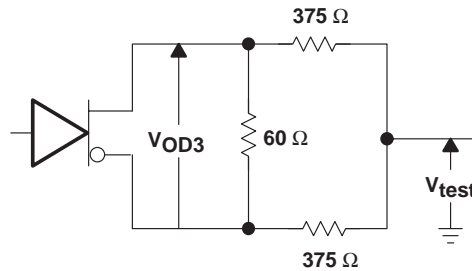
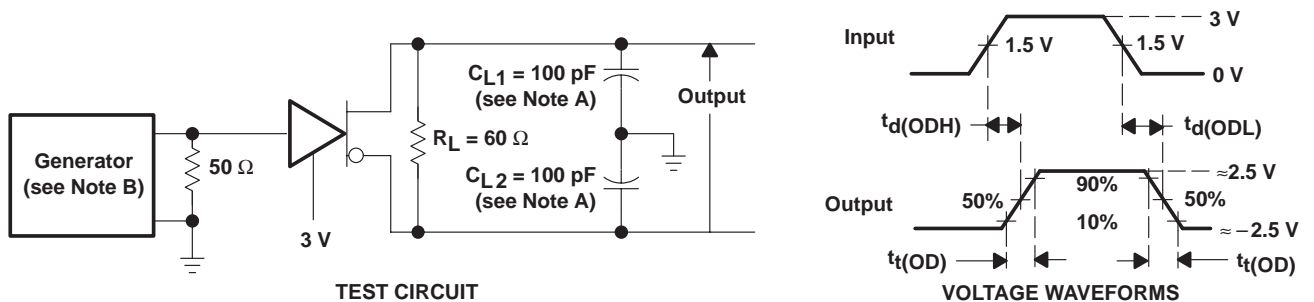


Figure 2. Driver V_{OD3}



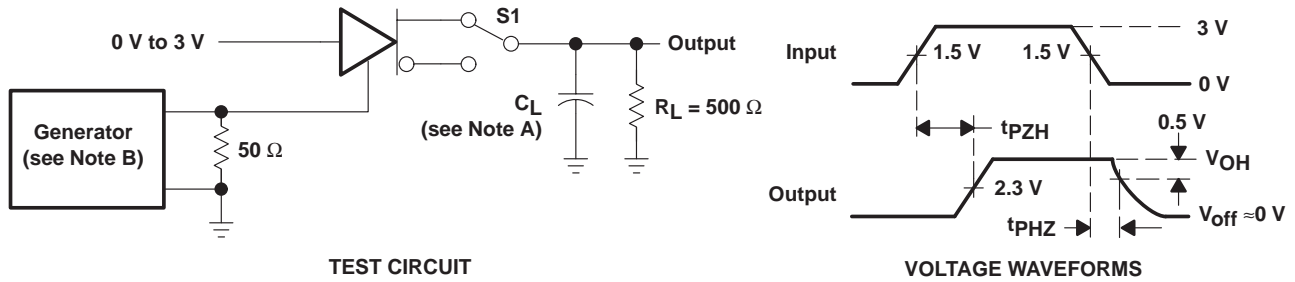
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

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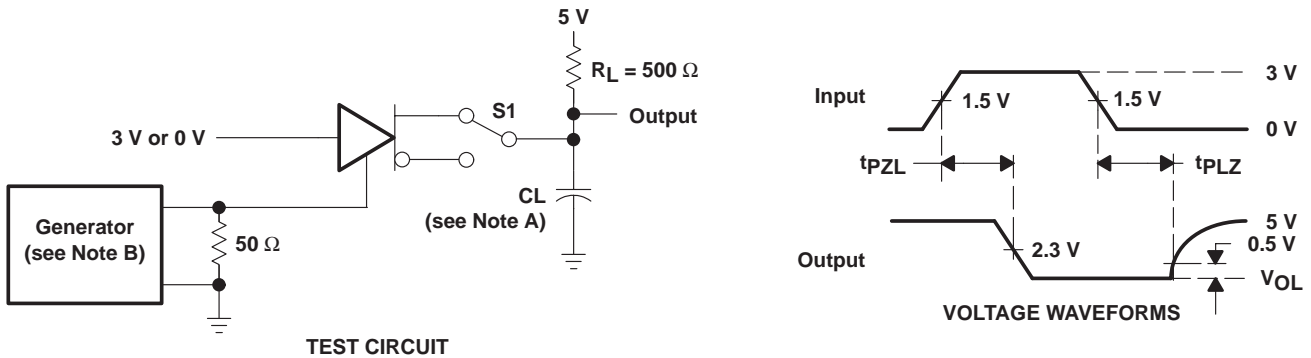
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $Z_O = 50 \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $Z_O = 50 \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

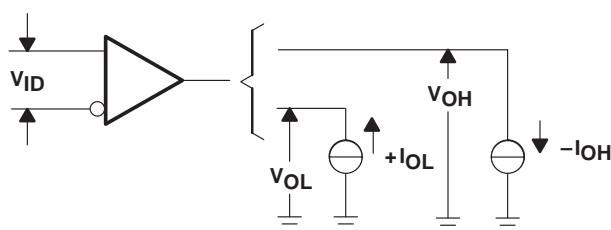
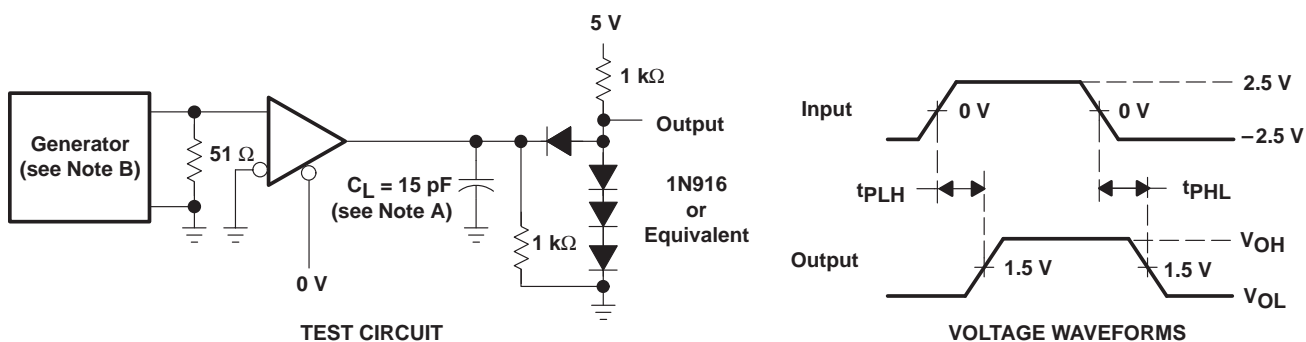


Figure 6. Receiver V_{OH} and V_{OL}



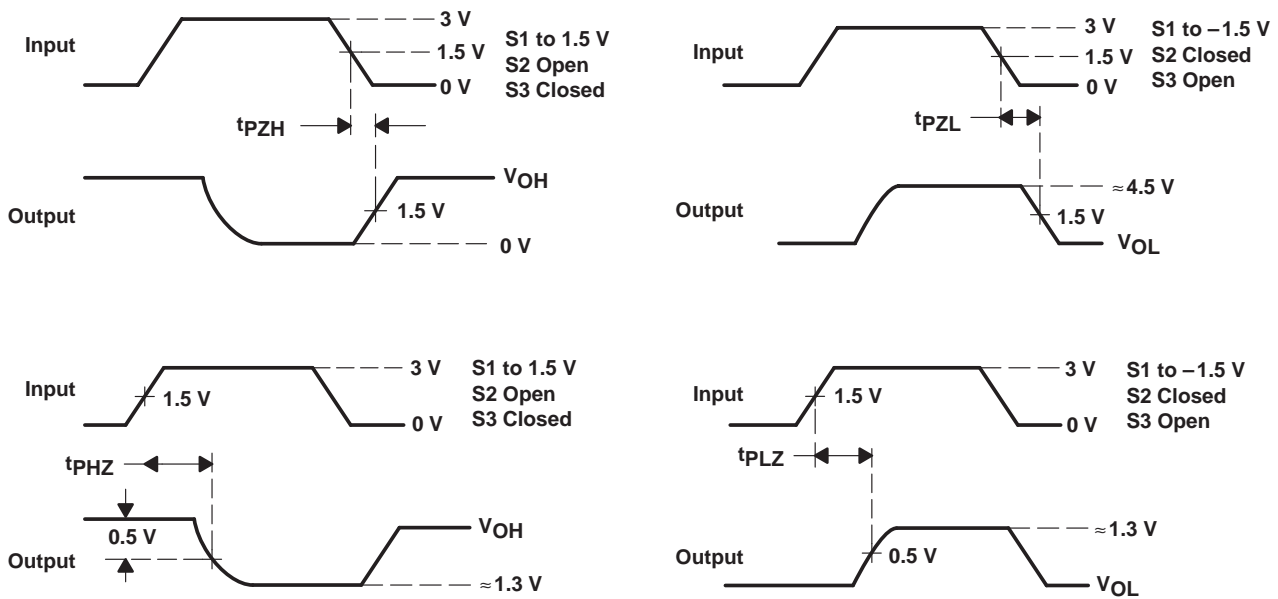
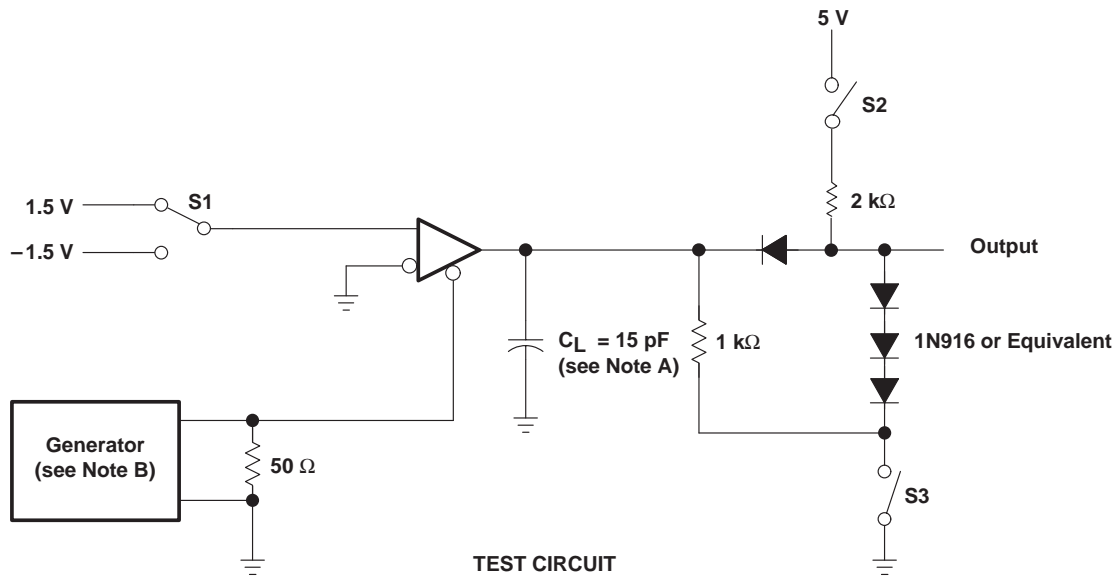
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

Figure 7. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, $Z_O = 50 \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

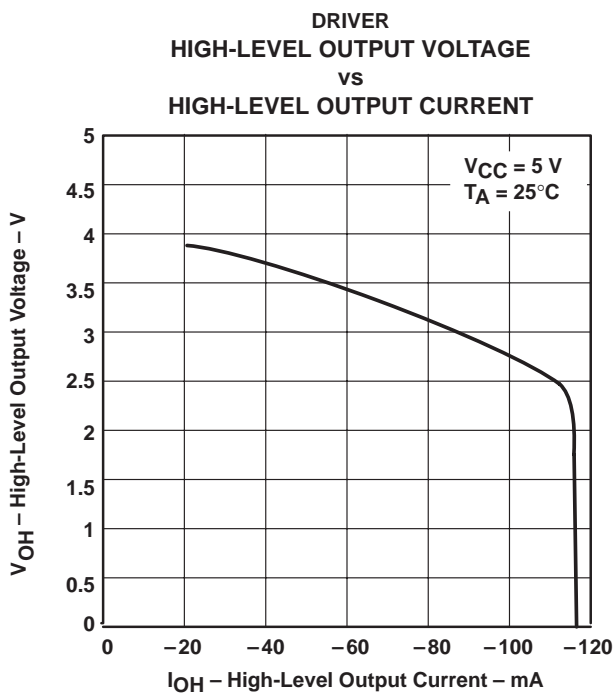


Figure 9

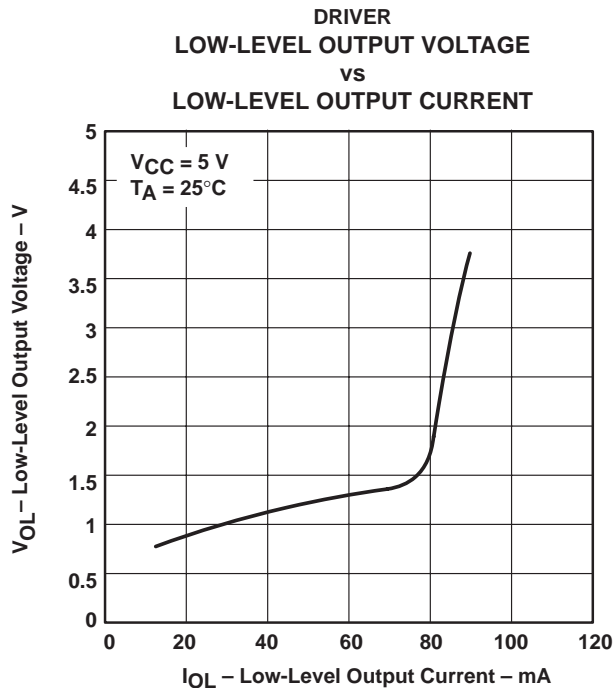


Figure 10

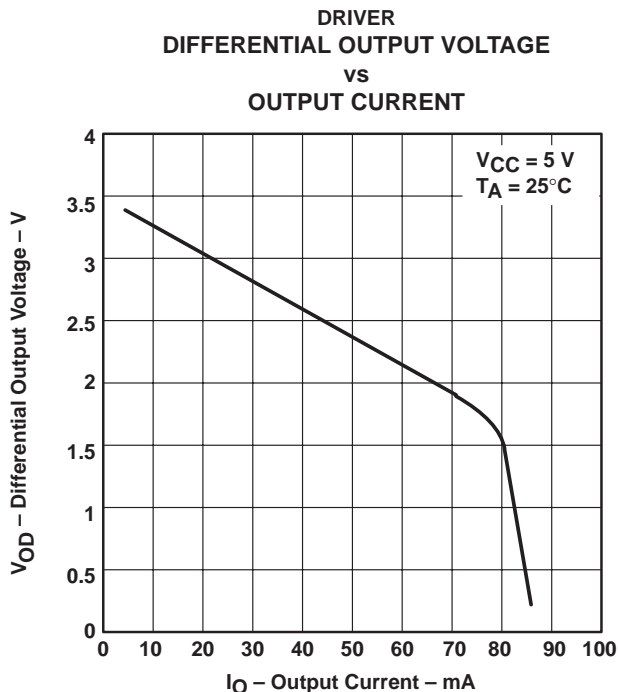


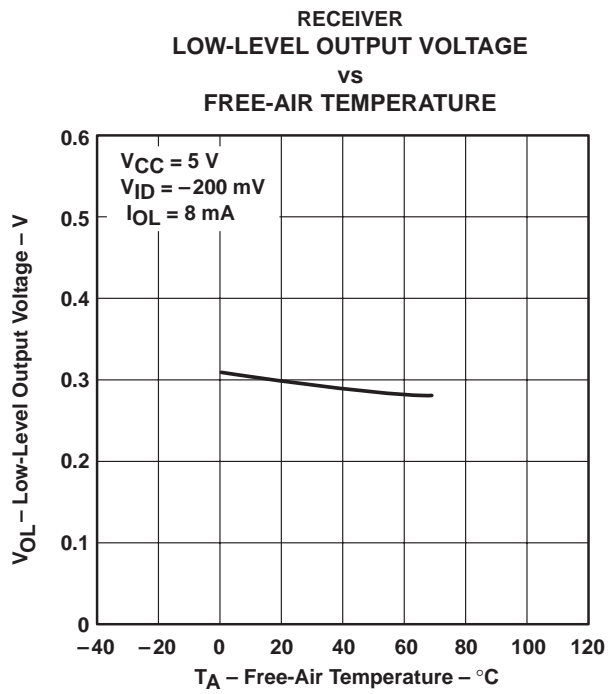
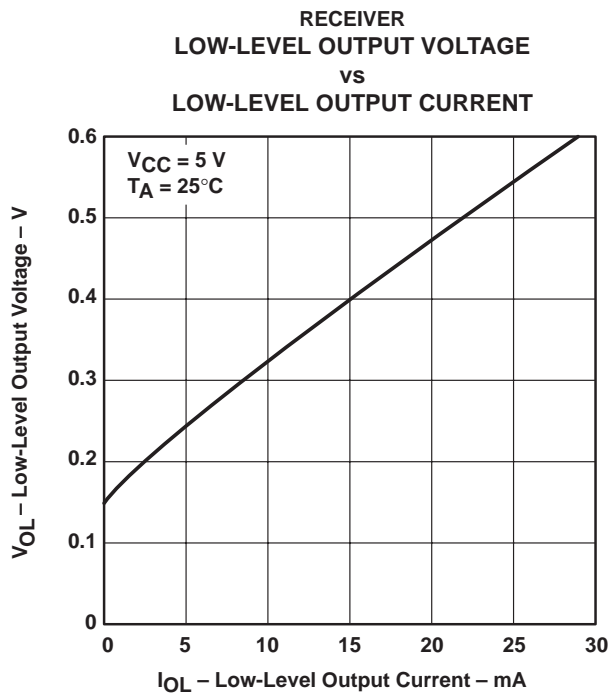
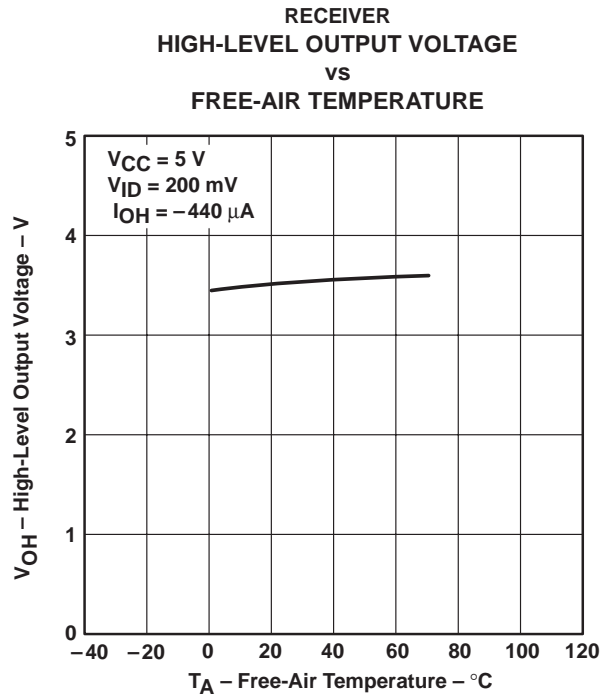
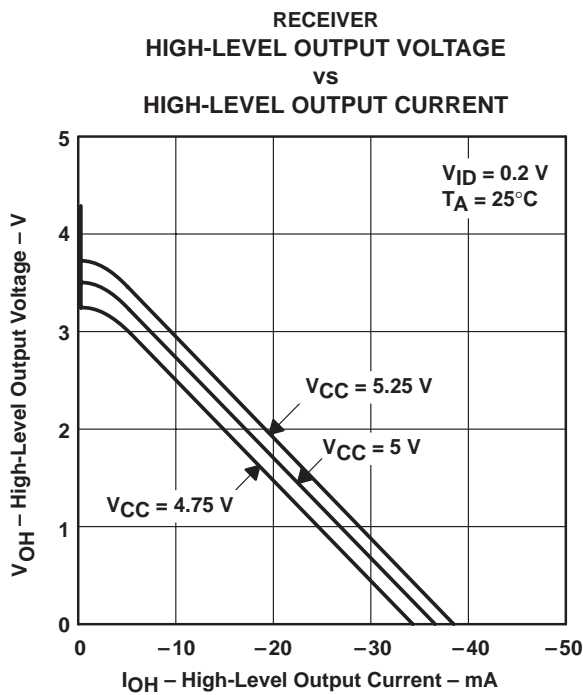
Figure 11

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

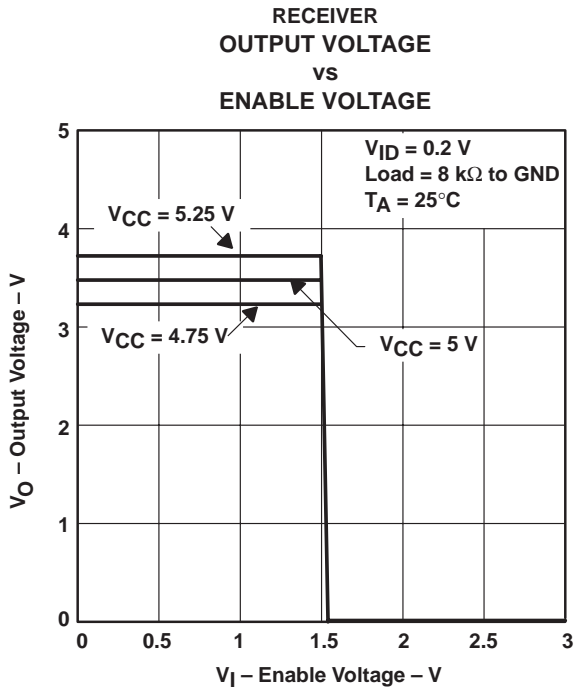


Figure 16

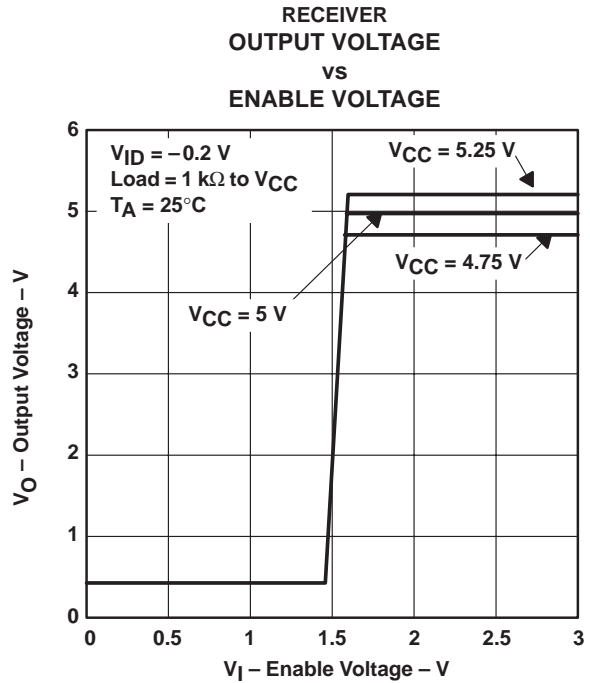
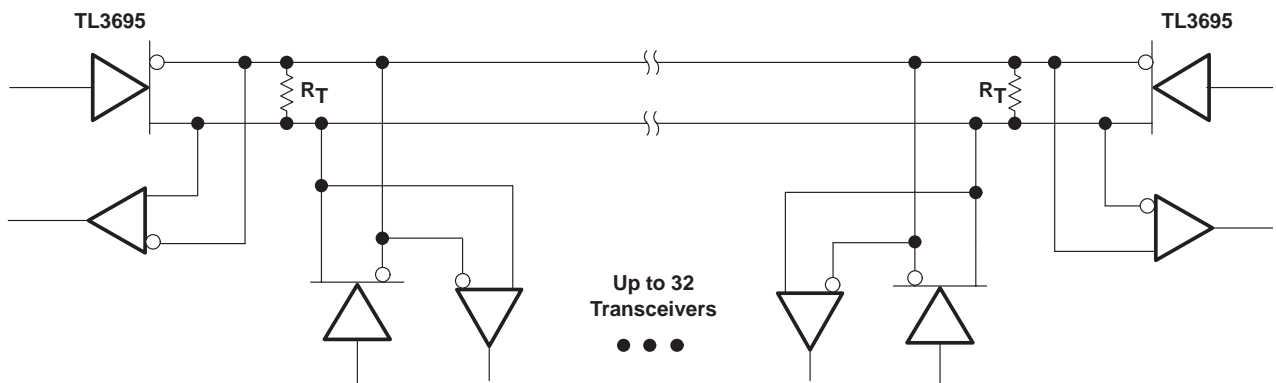


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

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