- Single-Chip TIA/EIA-232-F Interface for IBM ${ }^{\text {M }}$ PC/AT ${ }^{\text {™ }}$ Serial Port
- Designed to Transmit and Receive 4- $\mu \mathrm{s}$ Pulses (Equivalent to 256 kbit/s)
- Less Than 21-mW Power Consumption
- Wide Supply-Voltage Range, 4.75 V to 15 V
- Driver Output Slew Rates Are Internally Controlled to $30 \mathrm{~V} / \mu \mathrm{s}$ Max
- Receiver Input Hysteresis, 1000 mV Typ
- TIA/EIA-232-F Bus-Pin ESD Protection Exceeds:
- 15-kV, Human-Body Model
- IEC1000-4-2 Level-4 Compliant
- Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU V. 28
- Complements the SN75LP196
- Designed to Replace the Industry-Standard SN75185 and SN75C185 With the Same Flow-Through Pinout
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Dual-In-Line (N) Packages


## description

The SN75LP1185 is a low-power bipolar device containing three drivers and five receivers with 15 kV of ESD protection on the bus pins with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75185 and SN75C185. The flow-through pinout of the SN75LP1185 allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatibles. The SN75LP1185 provides a rugged, low-cost solution for this function with the combination of the bipolar processing and 15 kV of ESD protection.
The SN75LP1185 has internal slew-rate control to provide a maximum rate of change in the output signal of $30 \mathrm{~V} / \mu \mathrm{s}$. The driver output swing is nominally clamped at $\pm 6 \mathrm{~V}$ to enable the higher data rates associated with this device and to reduce EMI emissions. Even though the driver outputs are clamped, they can handle voltages up to $\pm 15 \mathrm{~V}$ without damage. All the logic inputs can accept $3.3-\mathrm{V}$ or $5-\mathrm{V}$ input signals.

The SN75LP1185 complies with the requirements of TIA/EIA-232-F and ITU V.28. These standards are for data interchange between a host computer and peripheral at signaling rates up to $20 \mathrm{kbit/} / \mathrm{s}$. The switching speeds of the SN75LP1185 support rates up to 256 kbit/s.

The SN75LP1185 is characterized for operation from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.

## Function Tables

| DRIVER |  |
| :---: | :---: |
| INPUT <br> DA | OUTPUT <br> DY |
| H | L |
| L | H |
| Open | L |


| RECEIVER |
| :---: |
| INPUT <br> RA |
| OUTPUT <br> RY |
| H |
| L |
| Open |

logic diagram (positive logic)


# absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\dagger$ 


$V_{D D}$ -0.5 V to 15 V
Negative supply-voltage range, $\mathrm{V}_{\mathrm{SS}}$ (see Note 1) .............................................. 0.5 V to -15 V

Driver (DA) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.4 \mathrm{~V}$
Output-voltage range, $\mathrm{V}_{\mathrm{O}}$ : Receiver (RY) ......................................................... -0.5 V to 6 V
Driver (DY) ........................................................... -15 V to 15 V
Electrostatic discharge: Bus pins (human-body model) (see Note 2) ........................ Class 3: 15 kV
Bus pins (machine model) ......................................................... 500 V
Bus pins (IEC1000-4-2, contact) .................................................... 8 kV
All pins (human-body model) (see Note 2) ............................. . . Class 3: 5 kV
All pins (machine model) ......................................................... . 400 V
Package thermal impedance, $\theta_{\mathrm{JA}}$ (see Note 3): DB package ..................................... $115^{\circ} \mathrm{C} / \mathrm{W}$
DW package ...................................... $97^{\circ} \mathrm{C} / \mathrm{W}$
N package ............................................ $67^{\circ} \mathrm{C} / \mathrm{W}$
PW package ........................................ $128^{\circ} \mathrm{C} / \mathrm{W}$
Storage temperature range, $\mathrm{T}_{\text {stg }}$ $65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$
Lead temperature $1,6 \mathrm{~mm}(1 / 16 \mathrm{inch})$ from case for 10 seconds ..................................... $260^{\circ} \mathrm{C}$
$\dagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to network ground terminal, unless otherwise noted.
2. Per MIL-STD-883, Method 3015.7
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.
recommended operating conditions

|  |  |  | MIN | NOM |
| :--- | :--- | ---: | ---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Mupply voltage (see Note 4) | MAX | UNIT |  |
| $\mathrm{V}_{\mathrm{DD}}$ | Supply voltage (see Note 5) | 4.75 | 5 | 5.25 |
| $\mathrm{~V}_{\mathrm{SS}}$ | Supply voltage (see Note 5) | V |  |  |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  | 12 | 15 |
| $\mathrm{~V}_{\mathrm{IL}}$ | Low-level input voltage | -9 | -12 | -15 |
| $\mathrm{~V}_{\mathrm{I}}$ | Receiver input voltage | DA | V |  |
| $\mathrm{I}_{\mathrm{OH}}$ | High-level output current | DA |  | V |
| $\mathrm{I}_{\mathrm{OL}}$ | Low-level output current | RA | -25 | 0.8 |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating free-air temperature | RY | V |  |

NOTES: 4. $\mathrm{V}_{\mathrm{CC}}$ cannot be greater than $\mathrm{V}_{\mathrm{DD}}$.
5. The device operates down to $\mathrm{V}_{\mathrm{DD}}=\mathrm{V}_{\mathrm{CC}}$ and $\left|\mathrm{V}_{\mathrm{SS}}\right|=\mathrm{V}_{\mathrm{CC}}$, but supply currents increase and other parameters may vary slightly from the data sheet limits.

## supply currents over the recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply current for $\mathrm{V}_{\mathrm{CC}}$, ICC | No load, <br> All inputs at minimum $\mathrm{V}_{\mathrm{OH}}$ or maximum $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{V}_{\mathrm{DD}}=9 \mathrm{~V}$, | $\mathrm{V}_{S S}=-9 \mathrm{~V}$ |  |  | 1000 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}$, | $\mathrm{V}_{\text {SS }}=-12 \mathrm{~V}$ |  |  | 1000 |  |
| Supply current for VDD, IDD |  | $\mathrm{V}_{\mathrm{DD}}=9 \mathrm{~V}$, | $\mathrm{V}_{S S}=-9 \mathrm{~V}$ |  |  | 800 |  |
|  |  | $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}$, | $\mathrm{V}_{S S}=-12 \mathrm{~V}$ |  |  | 800 |  |
| Supply current for VSS, ISS |  | $\mathrm{V}_{\mathrm{DD}}=9 \mathrm{~V}$, | $V_{S S}=-9 \mathrm{~V}$ |  |  | -625 |  |
|  |  | $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}$, | $\mathrm{V}_{\text {SS }}=-12 \mathrm{~V}$ |  |  | -625 |  |

driver electrical characterisitics over the recommended operating conditions (unless otherwise noted)

|  | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VOH | High-level output voltage | $\begin{array}{\|l\|} \hline \mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \\ \mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega, \\ \text { See Figure } 1 \\ \hline \end{array}$ | $\mathrm{V}_{\mathrm{DD}}=9 \mathrm{~V}$, | $\mathrm{V}_{S S}=-9 \mathrm{~V}$ | 5 | 5.8 | 6.6 | V |
|  |  |  | $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}$, | VSS $=-12 \mathrm{~V}$, See Note 6 | 5 | 5.8 | 6.6 |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega, \end{aligned}$$\text { See Figure } 1$ | $V_{D D}=9 \mathrm{~V}$, | $\mathrm{V}_{S S}=-9 \mathrm{~V}$ | -5 | -5.8 | -6.9 | V |
|  |  |  | $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}$, | $\mathrm{V}_{\text {SS }}=-12 \mathrm{~V}, \quad$ See Note 6 | -5 | -5.9 | -6.9 |  |
| ${ }_{\text {IIH }}$ | High-level input current | $V_{\text {I }}$ at $V_{\text {CC }}$ |  |  |  |  | 1 | $\mu \mathrm{A}$ |
| IIL | Low-level input current | $V_{1}$ at GND |  |  |  |  | -1 | $\mu \mathrm{A}$ |
| ${ }^{\text {IOS(H) }}$ | Short-circuit high-level output current | $\mathrm{V}_{\mathrm{O}}=\mathrm{GND}$ or $\mathrm{V}_{\text {SS }}$, |  | See Figure 2 and Note 7 |  | -30 | -55 | mA |
| IOS(L) | Short-circuit low-level output current | $\mathrm{V}_{\mathrm{O}}=\mathrm{GND}$ or $\mathrm{V}_{\mathrm{DD}}$, |  | See Figure 2 and Note 7 |  | 30 | 55 | mA |
| ro | Output resistance | $\mathrm{V}_{\mathrm{DD}}=\mathrm{V}_{S S}=\mathrm{V}_{\mathrm{CC}}=0$, |  | $\mathrm{V}_{\mathrm{O}}=2 \mathrm{~V}$ | 300 |  |  | $\Omega$ |

NOTES: 6. Maximum output swing is nominally clamped at $\pm 6 \mathrm{~V}$ to enable the higher data rates associated with this device and to reduce EMI emissions. The driver outputs may slightly exceed the maximum output voltage over the full $\mathrm{V}_{\mathrm{CC}}$ and temperature ranges.
7. Not more than one output should be shorted at one time.
driver switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

|  | PARAMETER |  | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPHL | Propagation delay time, high- to low-level output | $R_{L}=3 \mathrm{k} \Omega$ to $7 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, See Figure 1 |  | 300 | 800 | 1600 | ns |
| tPLH | Propagation delay time, low- to high-level output | $R_{L}=3 \mathrm{k} \Omega$ to $7 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, See Figure 1 |  | 300 | 800 | 1600 | ns |
| ${ }^{\text {t }}$ LH | Transition time, low- to high-level output | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$, <br> $V_{D D}=12 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{SS}}=-12 \mathrm{~V}$, <br> $R_{\mathrm{L}}=3 \mathrm{k} \Omega$ to $7 \mathrm{k} \Omega$, <br> See Figure 1 and <br> Note 9 | Using $\mathrm{V}_{\mathrm{TR}}=10 \%$-to- $90 \%$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, See Note 8 | 375 |  | 2240 | ns |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 3 \mathrm{~V}$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | 200 |  | 1500 |  |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 2 \mathrm{~V}$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | 133 |  | 1000 |  |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 3 \mathrm{~V}$ transition region, Driver speed $=125 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=2500 \mathrm{pF}$ |  |  | 2750 |  |
| ${ }^{\text {t }}$ HL | Transition time, high- to low-level output | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$, <br> $V_{D D}=12 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{SS}}=-12 \mathrm{~V}$, <br> $R_{L}=3 \mathrm{k} \Omega$ to $7 \mathrm{k} \Omega$, <br> See Figure 1 and <br> Note 9 | Using $\mathrm{V}_{\mathrm{TR}}=10 \%$-to- $90 \%$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$, See Note 8 | 375 |  | 2240 | ns |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 3 \mathrm{~V}$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | 200 |  | 1500 |  |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 2 \mathrm{~V}$ transition region, Driver speed $=250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | 133 |  | 1000 |  |
|  |  |  | Using $\mathrm{V}_{\mathrm{TR}}= \pm 3 \mathrm{~V}$ transition region, Driver speed $=125 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=2500 \mathrm{pF}$ |  |  | 2750 |  |
| SR | Output slew rate | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{DD}}=12 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{SS}}=-12 \mathrm{~V} \end{aligned}$ | Using $\mathrm{V}_{\mathrm{TR}}= \pm 3 \mathrm{~V}$ transition region, Driver speed $=0$ to $250 \mathrm{kbit} / \mathrm{s}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ | 4 | 20 | 30 | V/us |

NOTES: 8. Equivalent to the SN75C185. The SN75LP1185 output-voltage swing is clamped to about $70 \%$ of the typical SN75C185 output-voltage swing, and the specified limits reflect the reduced output swing.
9. Maximum output swing is limited to $\pm 6 \mathrm{~V}$ to enable the higher data rates associated with this device and to reduce EMI emissions.
receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

|  | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{17+}$ | Positive-going input threshold voltage | See Figure 3 | 1.6 | 2 | 2.55 | V |
| $\mathrm{V}_{\text {IT }}$ | Negative-going input threshold voltage | See Figure 3 | 0.6 | 1 | 1.45 | V |
| $\mathrm{V}_{\mathrm{HYS}}$ | Input hysteresis, $\mathrm{V}_{\text {IT+ }} \mathrm{V}_{\text {IT- }}$ | See Figure 3 | 600 | 1000 |  | mV |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{IOH}=-1 \mathrm{~mA}$ | 2.5 | 3.9 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{IOL}=2 \mathrm{~mA}$ |  | 0.33 | 0.5 | V |
| IIH | High-level input current | $\mathrm{V}_{1}=3 \mathrm{~V}$ | 0.43 | 0.6 | 1 | mA |
|  |  | $\mathrm{V}_{\mathrm{I}}=25 \mathrm{~V}$ | 3.6 | 5.1 | 8.3 |  |
| IIL | Low-level input current | $\mathrm{V}_{1}=-3 \mathrm{~V}$ | -0.43 | -0.6 | -1 | mA |
|  |  | $\mathrm{V}_{\mathrm{I}}=-25 \mathrm{~V}$ | -3.6 | -5.1 | -8.3 |  |
| IOS(H) | Short-circuit high-level output current | $\mathrm{V}_{\mathrm{O}}=0, \quad$ See Figure 5 and Note 7 |  |  | -20 | mA |
| Ios(L) | Short-circuit low-level output current | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}, \quad$ See Figure 5 and Note 7 |  |  | 20 | mA |
| RIN | Input resistance | $\mathrm{V}_{\text {I }}= \pm 3 \mathrm{~V}$ to $\pm 25 \mathrm{~V}$ | 3 | 5 | 7 | k $\Omega$ |

NOTE 7: Not more than one output should be shorted at one time.

## LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS335 - JANUARY 1999
receiver switching characteristics over recommended operating free-air temperature range, $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ (unless otherwise noted) (see Figure 4)

|  | PARAMETER | MIN | TYP |
| :---: | :--- | ---: | :---: |
| MPHL | Mropagation delay time, high- to low-level output | UNIT |  |
| tPLH | Propagation delay time, low- to high-level output | 400 | 900 |
| tTLH | Transition time, low- to high-level output | 400 | 900 |
| tTHL | Transition time, high- to low-level output | 200 | 500 |
| tSK(p) | Pulse skew \|tPLH - tpHLl | 200 | 400 |

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:
For $\mathrm{C}_{\mathrm{L}}<1000 \mathrm{pF}: \mathrm{t}_{\mathrm{w}}=4 \mu \mathrm{~s}, \mathrm{PRR}=250 \mathrm{kbit} / \mathrm{s}, \mathrm{Z}_{\mathrm{O}}=50 \Omega$, $\mathrm{t}_{\mathrm{r}}$ and $\mathrm{t}_{\mathrm{f}}<50 \mathrm{~ns}$.
For $C_{L}=2500 \mathrm{pF}: \mathrm{t}_{\mathrm{w}}=8 \mu \mathrm{~s}, \mathrm{PRR}=125 \mathrm{kbit} / \mathrm{s}, \mathrm{Z}_{\mathrm{O}}=50 \Omega, \mathrm{t}_{\mathrm{r}}$ and $\mathrm{t}_{\mathrm{f}}<50 \mathrm{~ns}$.
B. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform


Figure 2. Driver Ios Test

Inputs Outputs


Figure 3. Receiver $\mathrm{V}_{\mathrm{IT}}$ Test

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $\mathrm{t}_{\mathrm{w}}=4 \mu \mathrm{~s}, \mathrm{PRR}=250 \mathrm{kbit} / \mathrm{s}, \mathrm{Z}_{\mathrm{O}}=50 \Omega, \mathrm{t}_{\mathrm{r}}$ and $\mathrm{t}_{\mathrm{f}}<50 \mathrm{~ns}$.
B. $C_{L}$ includes probe and jig capacitance.

Figure 4. Receiver Parameter Test Circuit and Waveform


Figure 5. Receiver Ios Test

## APPLICATION INFORMATION

Diodes placed in series with the $\mathrm{V}_{\mathrm{DD}}$ and $\mathrm{V}_{\text {SS }}$ leads protect the SN75LP1185 in the fault condition when the device outputs are shorted to $\pm 15 \mathrm{~V}$ and the power supplies are at low voltage and provide low-impedance paths to ground (see Figure 6).


Figure 6. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

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