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<ul> <li>Four Independent Drivers and Receivers</li> <li>Loopback Mode Functionally Self Tests</li> </ul>		CKAGE VIEW)
Drivers and Receivers Without Disconnection From Line	3A [] 1	28 2LB
<ul> <li>Driver Slew Rate Controlled by a Single</li> </ul>	3Z [] 2 3LB [] 3	27 2Z 26 2A
Resistor	4A 🛛 4	25 1LB
Internal Thermal-Overload Protection	<u>4Z</u> [] 5	24 🛛 1Z
<ul> <li>RS-423-B Inputs and Outputs Designed to</li> </ul>	4 <u>LB</u> [] 6	23 🛛 1A
Withstand ±25 V	V <sub>SS</sub> [] 7	22 Rws
ESD Protection Exceeds 2000 V Per	GND 8	21 VDD
MIL-STD-833C Method 3015	4B 🛛 9	20 🛛 1Y
● LinBiCMOS <sup>™</sup> Process Technology	4Y 🛛 10	19 🛛 1B
	3B 🛛 11	18 🛛 2Y
description	3Y 🚺 12	17 🛛 2B
description	3C [ 13	16 🛛 2C
The SN75LBC786 is a monolithic quadruple	4C [ 14	15 🛛 1C
RS-423-B driver and receiver with integrated-		

loopback function. The operation of the

SN75LBC786 is closely based on that of the SN75186. In normal operation, the device performs as four independent RS-423-B driver/receiver pairs designed to interface data-terminal equipment (DTE) with data circuit-terminating equipment (DCE). In loopback mode, the signal from each driver output is fed back via special circuitry into its associated receiver input, removing the need to locally disconnect cables and install a loopback connector. The receiver output signal is the same as the driver input signal.

The SN75LBC786 is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE								
LOOPBACK	I	NPUTS	OUT	OUTPUTS				
LB	Α	В	С	Z	Y			
н	L	L	Н	н	Н			
Н	н	L	Н	н	L			
Н	L	Н	L	L	Н			
Н	Н	Н	L	L	L			
Н	L	L	L	?	Н			
Н	н	L	L	?	L			
Н	L	Н	Н	?	Н			
Н	Н	Н	Н	?	L			
L	L	Х	Х	L	L			
L	Н	Х	Х	Н	L			

FUNCTION TABLE

H = high level, L = low level, X = irrelevant, ? = indeterminate



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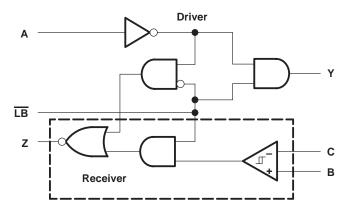
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### logic diagram (positive logic) (each transceiver)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Positive supply voltage, $V_{DD}$ (see Note 1) Negative supply voltage, $V_{SS}$ Receiver input voltage range Driver input voltage range Loopback input voltage range Driver output voltage range (supplies at 0 V) Driver output voltage range (supplies at $\pm 12$ V) Continuous power dissipation at (or below) $T_A = 70^{\circ}C$	
Operating free-air temperature range, T <sub>A</sub> Storage temperature range, T <sub>stg</sub> Case temperature for 10 seconds	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltages are with respect to petwork ground terminal.

NOTE 1: All voltages are with respect to network ground terminal.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub>	10.8	12	13.2	V	
Supply voltage, V <sub>SS</sub>		-10.8	-12	-13.2	V
High-level input voltage, VIH	Driver and loopback	2			V
Low-level input voltage, VIL	Driver and loopback			0.8	V
High-level output current, IOH	Receiver			-4	mA
Low-level output current, IOL	Receiver			4	mA
Slew rate control resistor, RWS		20	82	820	kΩ
Operating free-air temperature, TA		0		70	°C



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### DRIVER SECTION

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
∨он	High-level output voltage	Open circuit or RI =	450 Ω	4	5.5	6	V
VOL	Low-level output voltage	Open circuit or RI =	450 Ω	-6	-5.5	-4	V
ЧΗ	High-level input current	V <sub>I</sub> = 2.4 V – 5.5 V				100	μA
Ι <sub>Ι</sub>	Low-level input current	V <sub>I</sub> = 0 V - 0.8 V		-100			μA
IIKG	Output leakage current	$V_{DD} = V_{SS} = 0 V,$	$V_{O} = \pm 6 V$	-100		100	μΑ
IOS(H)	High-level short-circuit output current	VI = high,	V0 = 0 V	15		45	mA
IOS(L)	Low-level short-circuit output current	V <sub>I</sub> = low,	V0 = 0 V	-45		-15	mA
	Over the summer of the surface of a state of the	No load,	LB at 2 V		10	12	
IDD	Supply current (loopback off)	$RI = 450 \Omega$ ,	LB at 2 V		60	70	mA
IDD(LB)	Supply current with loopback on	No load,	LB at 0.8 V		13	16	mA
	Owners have seen as the set of the sector of	No load,	LB at 2 V		-10	-12	
ISS	Supply current (loopback off)	$RI = 450 \ \Omega,$	LB at 2 V		-60	-70	mA
IDD	Supply current with loopback on	No load,	LB at 0.8 V		-13	-16	mA
LOOPBA	CK MODE	· · · ·		-			
	Output voltage (input either high or low)	RI = >450 Ω,	$V_{LB} = low$	-6	-5.5	-4	V

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	-	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
				$R_{WS} = 0 \ k\Omega$		1.5		
Transition time, low-to-high level output <sup>t</sup> TLH (see Figure 1)		$R_{WS} = 20 \ k\Omega$	1.5	2.1	2.7			
			$R_{WS} = 82 \ k\Omega$	5	8	11	μs	
	(000 + 19010 +)			R <sub>WS</sub> = 820 kΩ		80		
		$RI = 450 \Omega$ , $C_L = 50 pF$ ,	$R_{WS} = 0 \ k\Omega$		1.5			
	Transition time, high-to-low level output (see Figure 1)	V <sub>WS</sub> = 5 V		$R_{WS} = 20 \ k\Omega$	1.5	2.1	2.7	
t <sub>THL</sub>		v level output		$R_{WS} = 82 \ k\Omega$	5	8	11	μs
		R <sub>WS</sub> = 820 kΩ		80				
SR	Output slew rate	1		R <sub>WS</sub> = 20 kΩ			15	V/µs
t <sub>sk</sub>	Output skew,  t <sub>PHL</sub> - t <sub>PLH</sub>   (see Figure 4)			$R_{WS} = 82 \text{ k}\Omega$			1	μs



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### **RECEIVER SECTION**

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V	Receiver input threshold voltage	$\forall_{IT} = (\forall_{I+} - \forall_{I-})$		-200		200	mV
VIT	(see Figure 5)	$V_{IT} = (V_{I+} - V_{I-})$ with 50	00- $\Omega$ series resistor	-400		400	mv
1.	Input current	V <sub>I</sub> = 10 V	Other input to GND		1.3	3.25	mA
'I	input current	V <sub>I</sub> = -10 V		-3.25	-1.3		
V <sub>hys</sub>	Hysteresis voltage			20	40	150	mV
Val	H High-level output voltage (see Note 2) $\frac{I_{O} = -20 \ \mu A}{I_{O} = -4 \ mA}$		3.5		5	V	
∨он			2.4		5	v	
VOL	Low-level output voltage	$I_{O} = 20 \ \mu A$ to 4 mA				0.4	V
los	RX short circuit current					50	mA
VID	Differential input voltage	Receiver inputs open circuit		1.6	2.1	2.6	V
Vofs	Fail safe output voltage	See Note 3		3.5			V

NOTES: 2. Device has an internal RX supply regulator. Maximum RX logic output voltage under no load is thus defined by an internal voltage value. This is nominally set to 4.5 V with a tolerance of ±5%.

3. One input at ground, other input open circuit,  $I_{O} = -20 \mu A$ , or both open circuit.

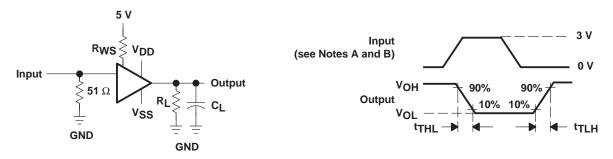
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high (see Figure 2)	С <sub>L</sub> = 50 рF		0.15	4	
<b>t</b> PHL	Propagation delay time, high-to-low (see Figure 2)		0.15	0.15	I	μs
<sup>t</sup> THL	Transition time, high-to-low (see Figure 3)			20	200	
<sup>t</sup> TLH	Transition time, low-to-high (see Figure 3)			20	200	ns



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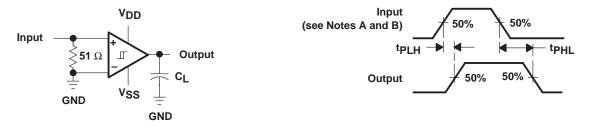
### PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: t<sub>f</sub> ≤ 10 nS, t<sub>f</sub> < 10 nS, Z<sub>0</sub> = 50 Ω, PRR ≥ 5 kHz, duty cycle = 50%, V<sub>max</sub> = 3 V, V<sub>min</sub> = 0 V.

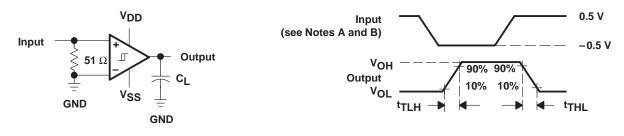
#### **Figure 1. Driver Transition Times**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: t<sub>f</sub> ≤ 10 nS, t<sub>f</sub> < 10 nS, Z<sub>0</sub> = 50 Ω, PRR ≥ 5 kHz, duty cycle = 50%, V<sub>max</sub> = 0.5 V, V<sub>min</sub> = −0.5 V.

#### Figure 2. Receiver Propagation Delay Times



- NOTES: A.  $C_{\mbox{L}}$  includes probe and jig capacitance.
  - B. The input pulse is supplied by a generator having the following characteristics:  $t_f \le 10 \text{ nS}$ ,  $t_f < 10 \text{ nS}$ ,  $Z_0 = 50 \Omega$ , PRR  $\ge 5 \text{ kHz}$ , duty cycle = 50%,  $V_{max} = 0.5 \text{ V}$ ,  $V_{min} = -0.5 \text{ V}$ .

### Figure 3. Receiver Transition Times



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### PARAMETER MEASUREMENT INFORMATION

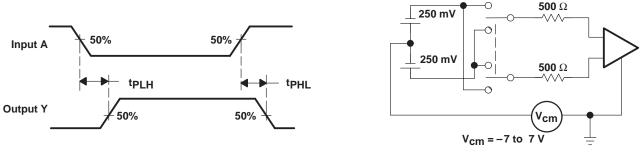


Figure 4. Skew Definition Times

Figure 5. Input Balance Test

### **PRINCIPLES OF OPERATION**

In normal operation, the SN75LBC786 functions as four independent drivers and receivers. The loopback mode is disabled by maintaining a high logic level on the  $\overline{LB}$  input. The receivers consist of differential comparators with hysteresis and resistive attenuation on the inputs. The resistive attenuation improves the input common-mode range and also provides additional protection from ESD and over-voltage stress. The differential and common-mode input impedance are sufficiently high to meet RS-423-B. The balance of the receiver input voltage current characteristics and bias voltage is such that the receiver remains in the intended binary state when a differential voltage of 500 mV is applied to the inputs through 500  $\Omega$  across the entire common-mode range (see Figure 5).

The drivers meet all RS-423-B specifications. In normal operation, the drivers have built-in current limits and thermal overload protection. Slew-rate controlling circuitry is included into the design that is adjusted to suit the application by means of an external resistor. The slew-rate controlling circuitry also has a default mode. If R<sub>WS</sub> is shorted to 5 V externally, the transition time defaults to approximately 1.5  $\mu$ s. The receiver is compatible to the RS-232 with the use of external input resistors to meet the RS-232 input-resistance specification of 3 k $\Omega$  to 7 k $\Omega$ .

Taking an individual  $\overline{LB}$  input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal-loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, -5 V, or the EIA-423-B marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75LBC786 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages. The loopback mode should be entered only when the driver output is low, that is, the marking condition. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.



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