

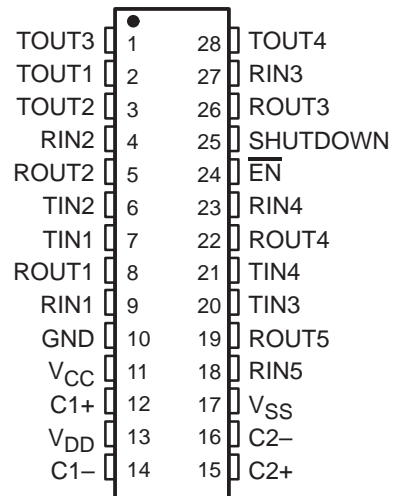
SN75LBC241

LOW-POWER LinBiCMOS™ MULTIPLE DRIVERS AND RECEIVERS

SLLS137E – MAY 1992 – REVISED JANUARY 1999

- Operates With Single 5-V Power Supply
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Improved Performance Replacement for MAX241
- Operates at Data Rates up to 100 kbit/s Over a 3-m Cable
- Low-Power Shutdown Mode . . . $\leq 1 \mu\text{A}$ Typ
- LinBiCMOS™ Process Technology
- Four Drivers and Five Receivers
- $\pm 30\text{-V}$ Input Levels
- 3-State TTL/CMOS Receiver Outputs
- $\pm 9\text{-V}$ Output Swing With a 5-V Supply
- Applications
 - TIA/EIA-232-F Interface
 - Battery-Powered Systems
 - Terminals
 - Modems
 - Computers
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages

DB OR DW PACKAGE
(TOP VIEW)



description

The SN75LBC241† is a low-power LinBiCMOS™ line-interface device containing four independent drivers and five receivers. It is designed as a plug-in replacement for the Maxim MAX241. The SN75LBC241 provides a capacitive-charge-pump voltage generator to produce RS-232 voltage levels from a 5-V supply. The charge-pump oscillator frequency is 20 kHz. Each receiver converts RS-232 inputs to 5-V TTL/CMOS levels. The receivers have a typical threshold of 1.2 V and a typical hysteresis of 0.5 V and can accept $\pm 30\text{-V}$ inputs. Each driver converts TTL/CMOS input levels into RS-232 levels.

The SN75LBC241 includes a receiver, a 3-state control line, and a low-power shutdown control line. When the $\overline{\text{EN}}$ line is high, receiver outputs are placed in the high-impedance state. When $\overline{\text{EN}}$ is low, normal operation is enabled.

The shutdown mode reduces power dissipation to less than 5 μW typically. In this mode, receiver outputs have high impedance, driver outputs are turned off, and the charge-pump circuit is turned off. When SHUTDOWN is high, the shutdown mode is enabled. When SHUTDOWN is low, normal operation is enabled.

This device has been designed to conform to TIA/EIA-232-F and ITU Recommendation V.28.

The SN75LBC241 has been designed using LinBiCMOS technology and cells contained in the Texas Instruments LinASIC™ library. Use of LinBiCMOS circuitry increases latch-up immunity in this device over an all-CMOS design.

The SN75LBC241 is characterized for operation from 0°C to 70°C.



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† Patent pending

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



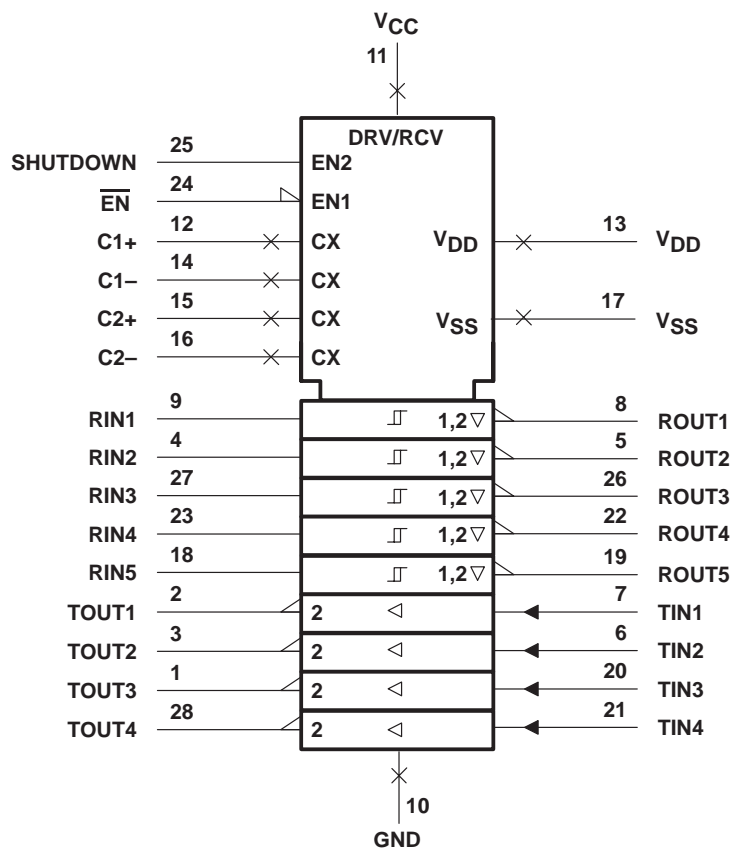
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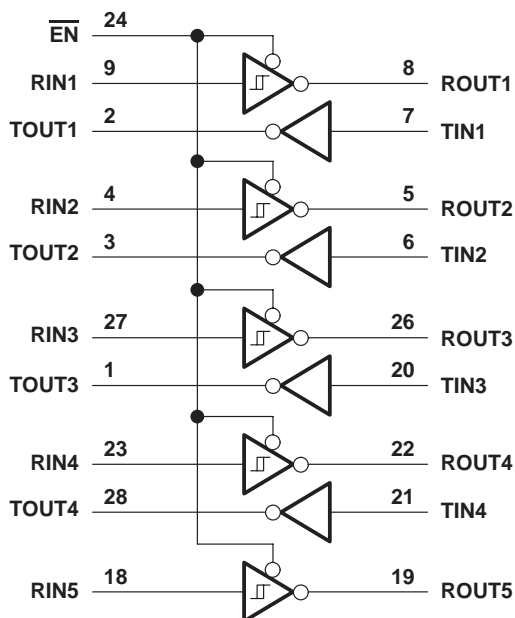
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN75LBC241

LOW-POWER LinBiCMOS™ MULTIPLE DRIVERS AND RECEIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|--------------------------------------|
| Input supply voltage range, V_{CC} (see Note 1) | –0.3 V to 6 V |
| Positive output supply voltage range, V_{DD} | $V_{CC} - 0.3$ V to 15 V |
| Negative output supply voltage range, V_{SS} | 0.3 V to –15 V |
| Input voltage range, V_I : Driver | –0.3 V to $V_{CC} + 0.3$ V |
| Receiver | ±30 V |
| Output voltage range, V_O : TOUT | $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V |
| ROUT | –0.3 V to $V_{CC} + 0.3$ V |
| Short-circuit duration: TOUT | Unlimited |
| Continuous total dissipation | See Dissipation Rating Table |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|--|--|
| DB | 1348 mW | 10.8 mW/°C | 862 mW |
| DW | 1603 mW | 12.8 mW/°C | 1026 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|--|-----|-----|------|
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | V |
| High-level input voltage, V_{IH} | TIN | | 2 | V |
| | $\overline{\text{EN}}$, SHUTDOWN | | 2.4 | |
| Low-level input voltage, V_{IL} | TIN, $\overline{\text{EN}}$, SHUTDOWN | | 0.8 | V |
| External charge-pump capacitor | C1–C4 (see Figure 1) | | 1 | μF |
| External charge-pump capacitor voltage rating | C1, C3 (see Figure 1) | | 6.3 | V |
| | C2, C4 (see Figure 1) | | 16 | |
| Receiver input voltage, V_I | | | ±30 | V |
| Operating free-air temperature, T_A | 0 | | 70 | °C |



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT | |
|------------------|---|-----------------|--|------|-----|------|----|
| V _{OH} | High-level output voltage | TOUT | R _L = 3 kΩ to GND, See Note 2 | 5 | 9 | V | |
| | | ROUT | I _{OH} = -1 mA | 3.5 | | | |
| V _{OL} | Low-level output voltage | TOUT | R _L = 3 kΩ to GND, See Note 3 | -9‡ | -5 | V | |
| | | ROUT | I _{OL} = 3.2 mA | | 0.4 | | |
| V _{IT+} | Receiver positive-going input threshold voltage | RIN | V _{CC} = 5 V, T _A = 25°C | 1.7 | 2.4 | V | |
| V _{IT-} | Receiver negative-going input threshold voltage | RIN | V _{CC} = 5 V, T _A = 25°C | 0.8 | 1.2 | V | |
| V _{hys} | Input hysteresis voltage (V _{IT+} - V _{IT-}) | RIN | V _{CC} = 5 V | 0.5 | 1 | V | |
| r _i | Receiver input resistance | RIN | V _{CC} = 5 V, T _A = 25°C | 3 | 5 | 7 | kΩ |
| r _o | Output resistance | TOUT | V _{DD} = V _{SS} = V _{CC} = 0, V _O = ±2 V | 300 | | | Ω |
| I _{OS} | Short circuit output current§ | TOUT | V _{CC} = 5.5 V, V _O = 0 | ±10 | | | mA |
| I _{IS} | Short circuit input current | TIN | V _I = 0 | | 200 | | μA |
| I _{CC} | Supply current | | V _{CC} = 5.5 V, T _A = 25°C, All outputs open | 4 | 8 | | mA |
| | | | All outputs open, T _A = 25°C, SHUTDOWN high | 1 | 10 | | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at one time.

NOTES: 2. Total I_{OH} drawn from TOUT1, TOUT2, TOUT3, TOUT4, and V_{DD} terminals should not exceed 12 mA.

3. Total I_{OL} drawn from TOUT1, TOUT2, TOUT3, TOUT4, and V_{SS} terminals should not exceed -12 mA.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----|-----|-----|------|
| t _{PLH(R)} | Receiver propagation-delay time, low- to high-level output | See Figure 2 | | 500 | | ns |
| t _{PHL(R)} | Receiver propagation-delay time, high- to low-level output | See Figure 2 | | 500 | | ns |
| t _{PZH} | Receiver output-enable time to high level | See Figure 5 | | 100 | | ns |
| t _{PZL} | Receiver output-enable time to low level | See Figure 5 | | 100 | | ns |
| t _{PHZ} | Receiver output-disable time from high level | See Figure 5 | | 50 | | ns |
| t _{PLZ} | Receiver output-disable time from low level | See Figure 5 | | 50 | | ns |
| SR | Driver slew rate | R _L = 3 kΩ to 7 kΩ, C _L = 2500 pF, See Figure 4 | | | 30 | V/μs |
| SR _(tr) | Driver transition region slew rate | R _L = 3 kΩ to 7 kΩ, C _L = 2500 pF, See Figure 4 | 4 | 6 | | V/μs |



APPLICATION INFORMATION

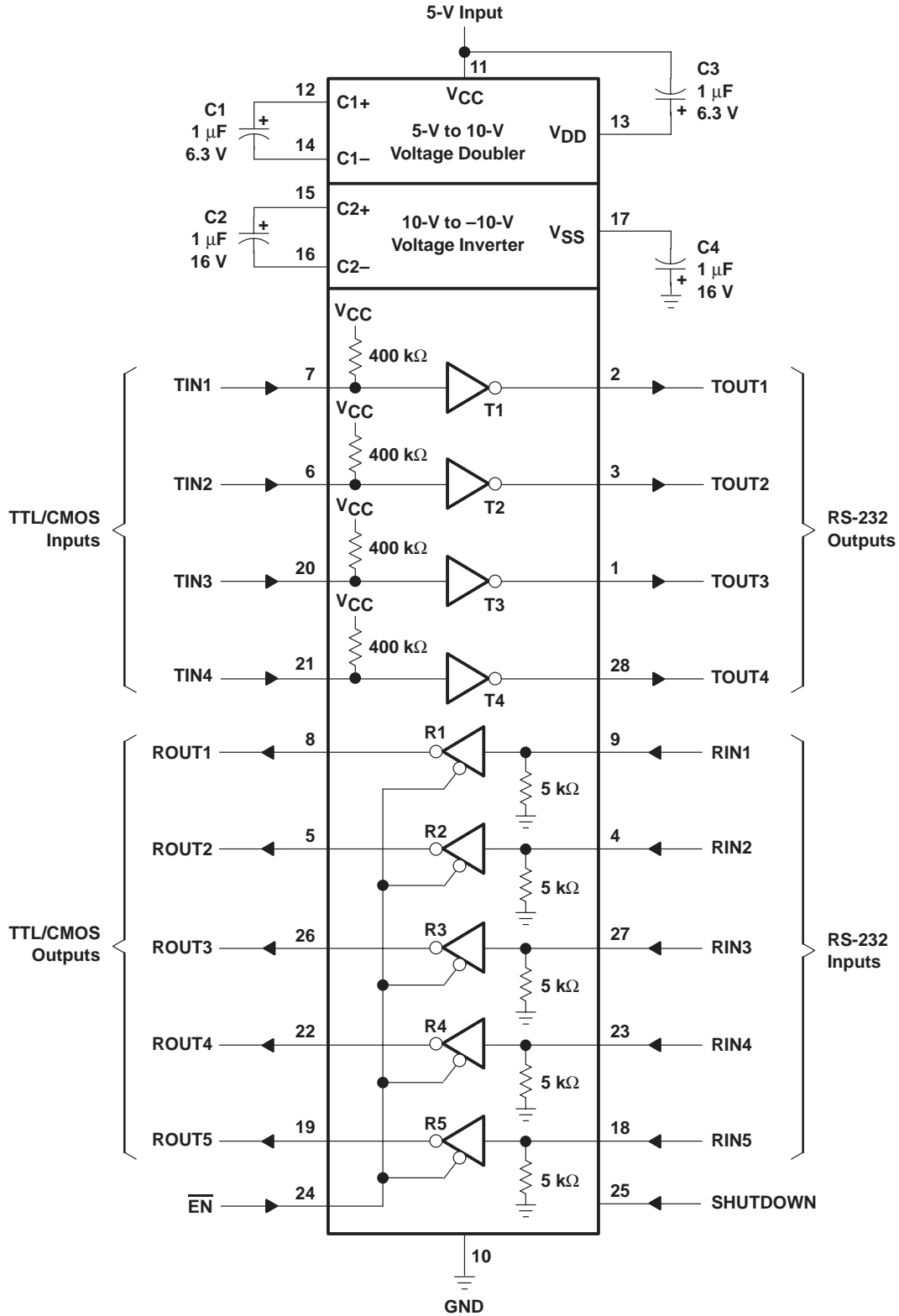
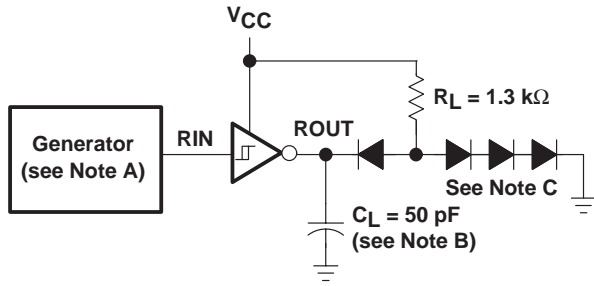
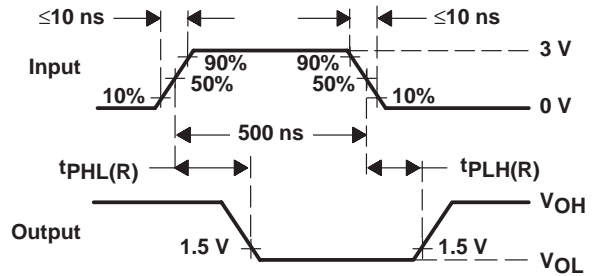


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION



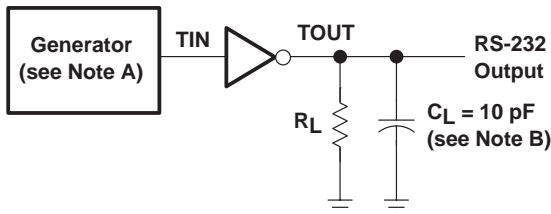
TEST CIRCUIT



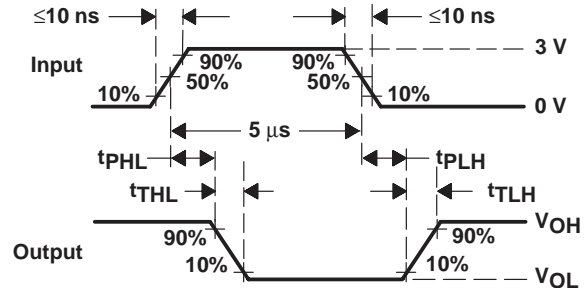
VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\le 50\%$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement



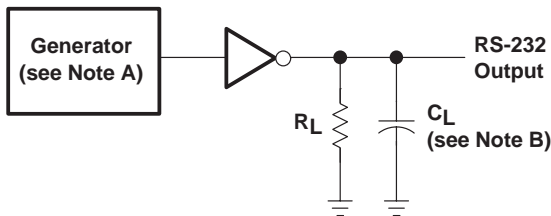
TEST CIRCUIT



VOLTAGE WAVEFORMS

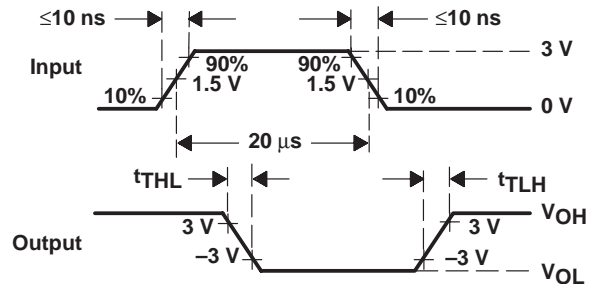
- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\le 50\%$.
 B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5- μs Input)



TEST CIRCUIT

$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

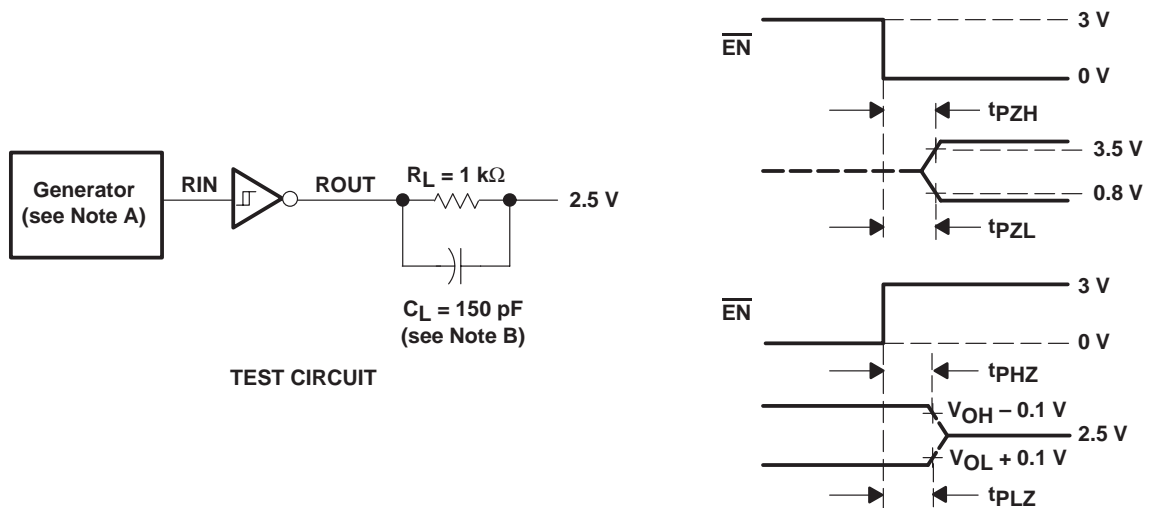


VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\le 50\%$.
 B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20- μs Input)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.
 B. C_L includes probe and jig capacitance.

Figure 5. Receiver Output Enable and Disable Timing

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