SN65LBC172, SN75LBC172
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163B – JULY 1993 – REVISED JANUARY 2000

- **Meet or Exceed EIA Standard RS-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Support Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75172**

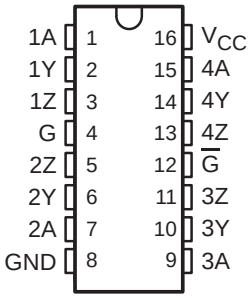
description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

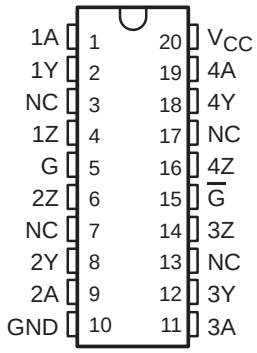
Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of –40°C to 85°C.

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



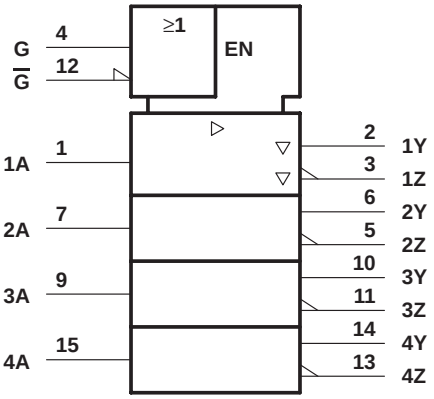
NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

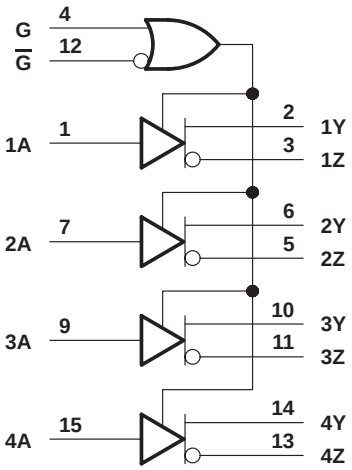
H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic symbol†

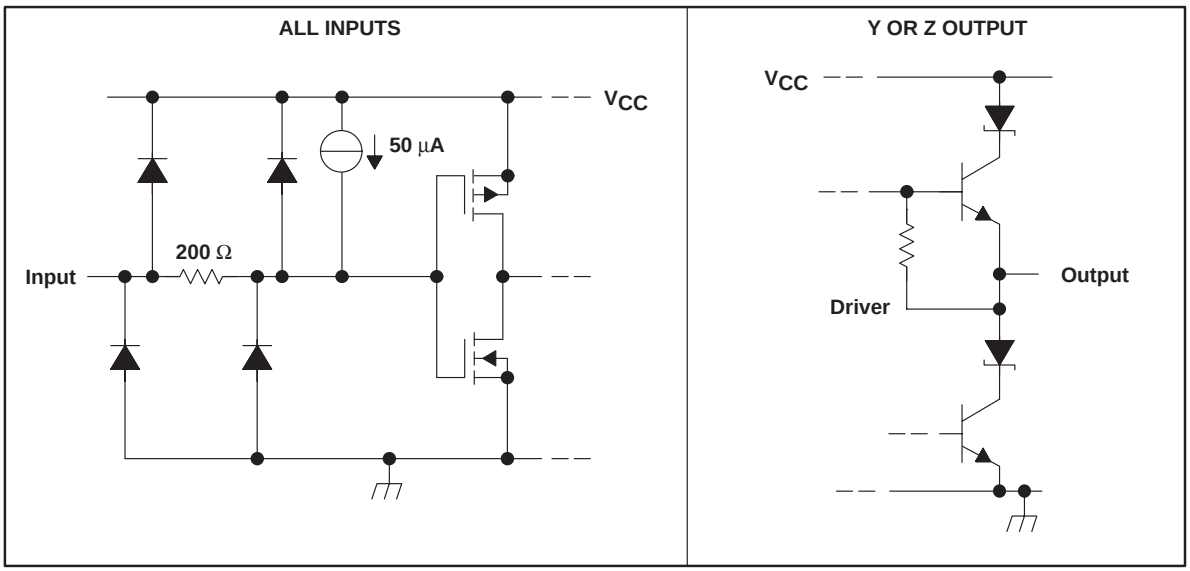


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, V_O . . . . . –10 V to 15 V
Voltage range at A, $\overline{G}$, G . . . . . –0.3 V to V_{CC} + 0.5 V
Continuous power dissipation . . . . . Internally limited‡
Operating free-air temperature range, T_A: SN65LBC172 . . . . . –40°C to 85°C
SN75LBC172 . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				–7	
High-level output current, I_{OH}	Y or Z			–60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC172	–40		85	°C
	SN75LBC172	0		70	

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
$\|V_{OD}\|$	Differential output voltage‡	R_L = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R_L = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = – 7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = – 7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				–100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			10	15	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			30	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			30	ns

PARAMETER MEASUREMENT INFORMATION

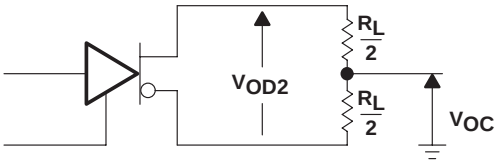
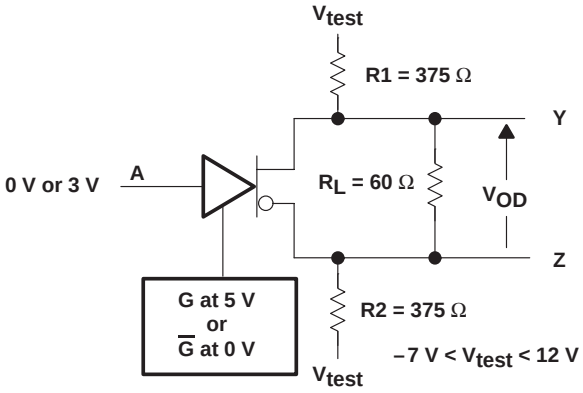
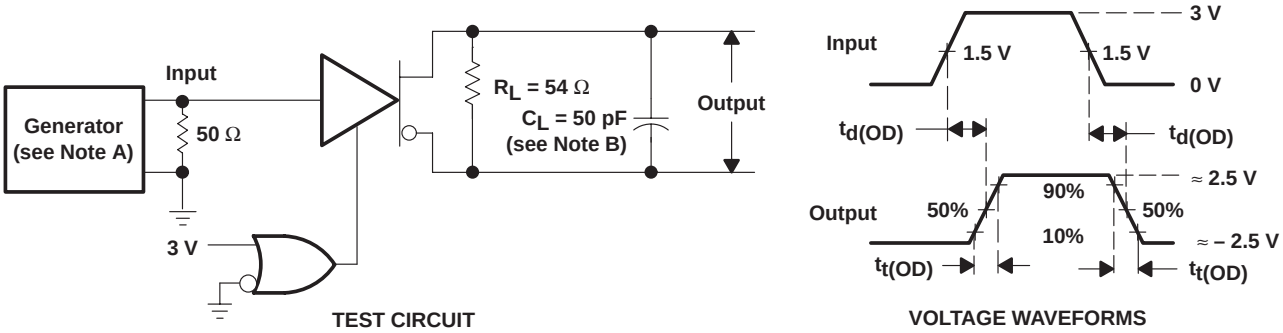


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

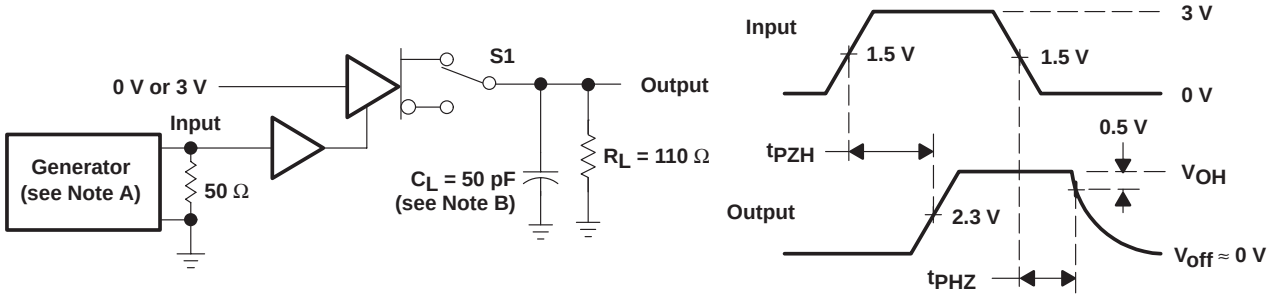
Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

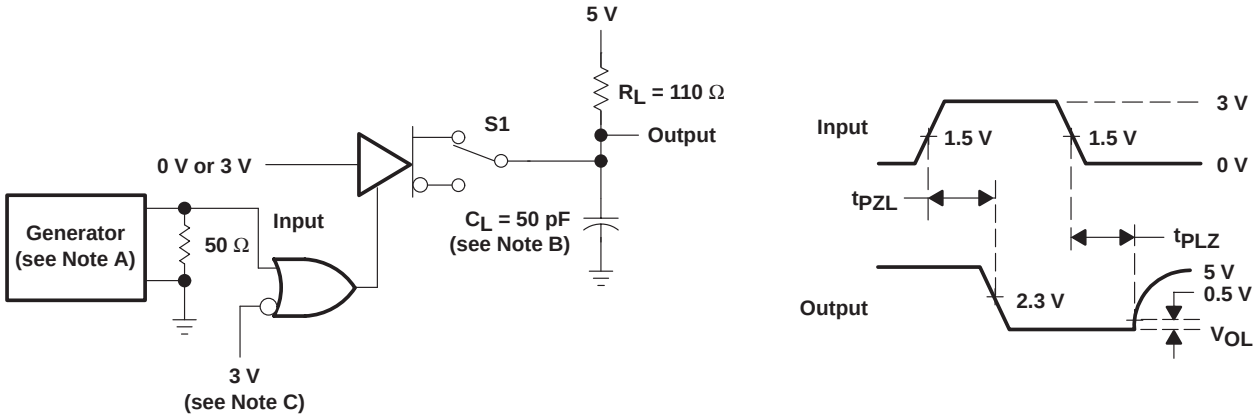
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

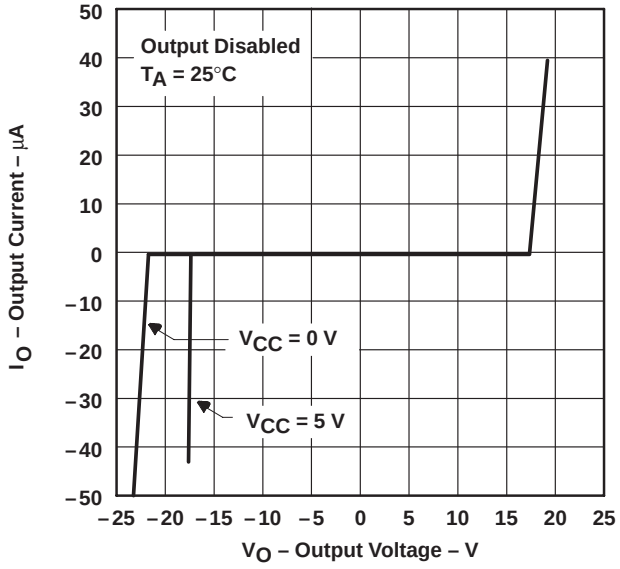


Figure 6

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

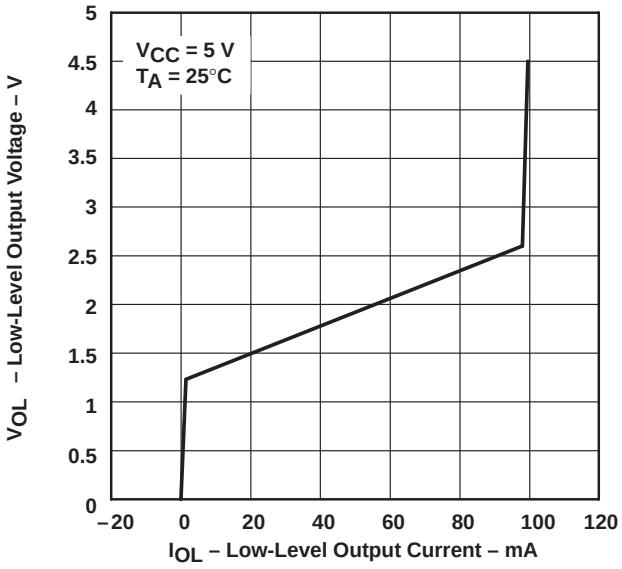


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

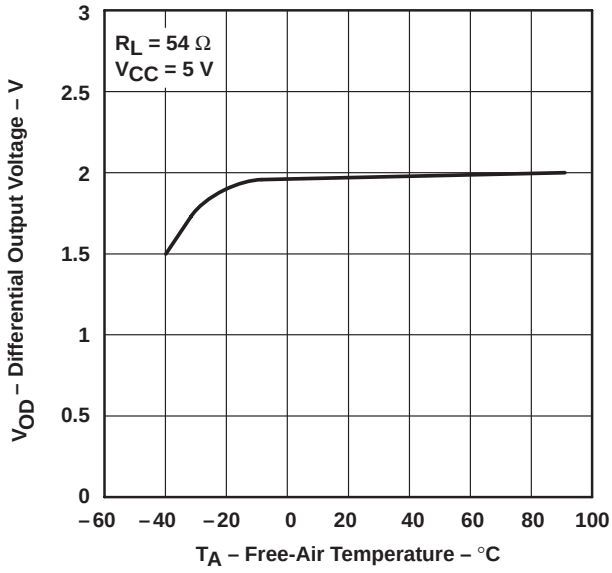


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

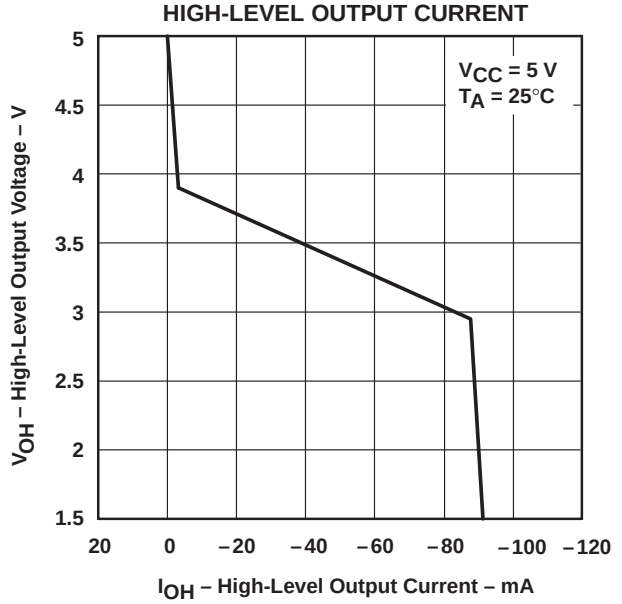


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

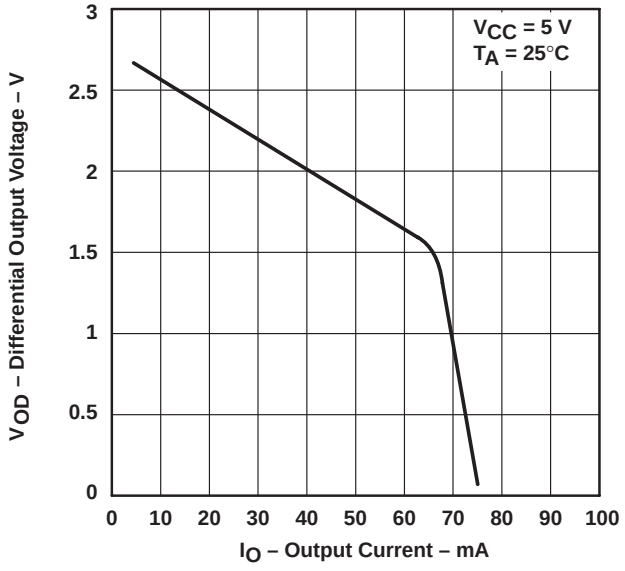


Figure 10

PROPAGATION DELAY TIME, DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

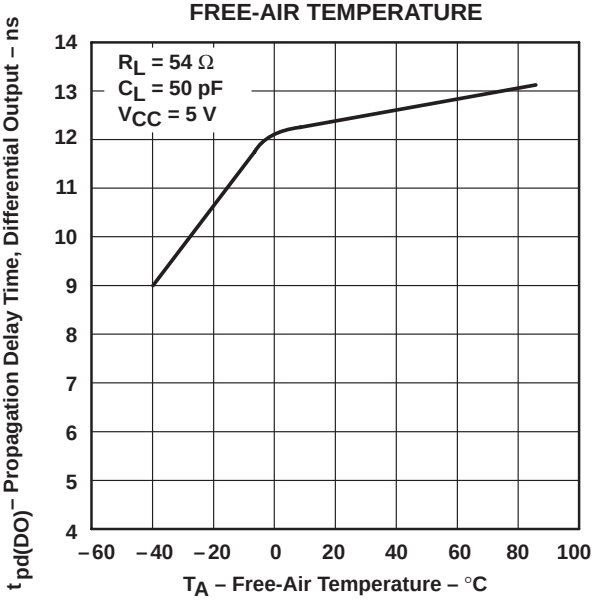
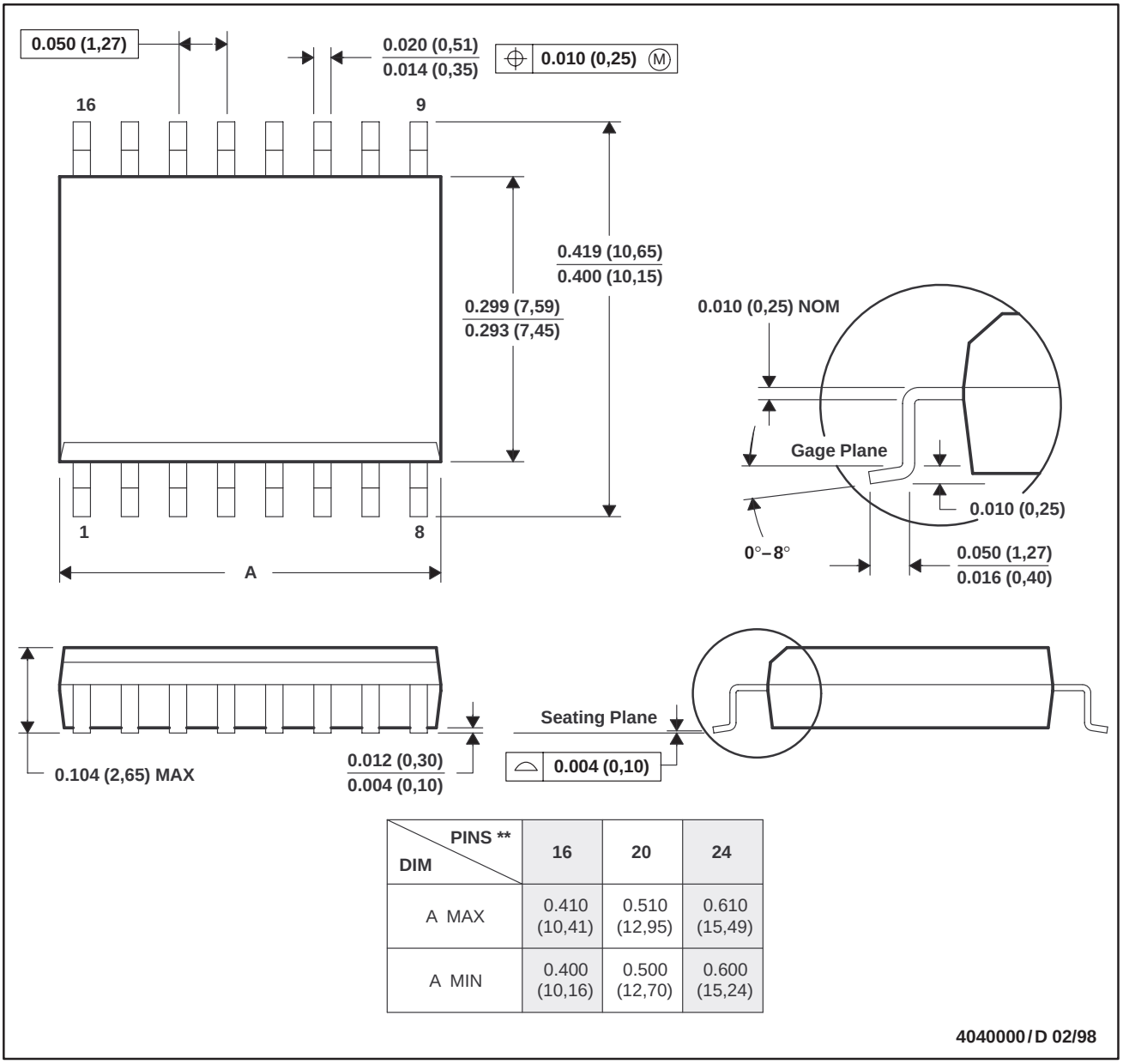


Figure 11

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

4040000/D 02/98

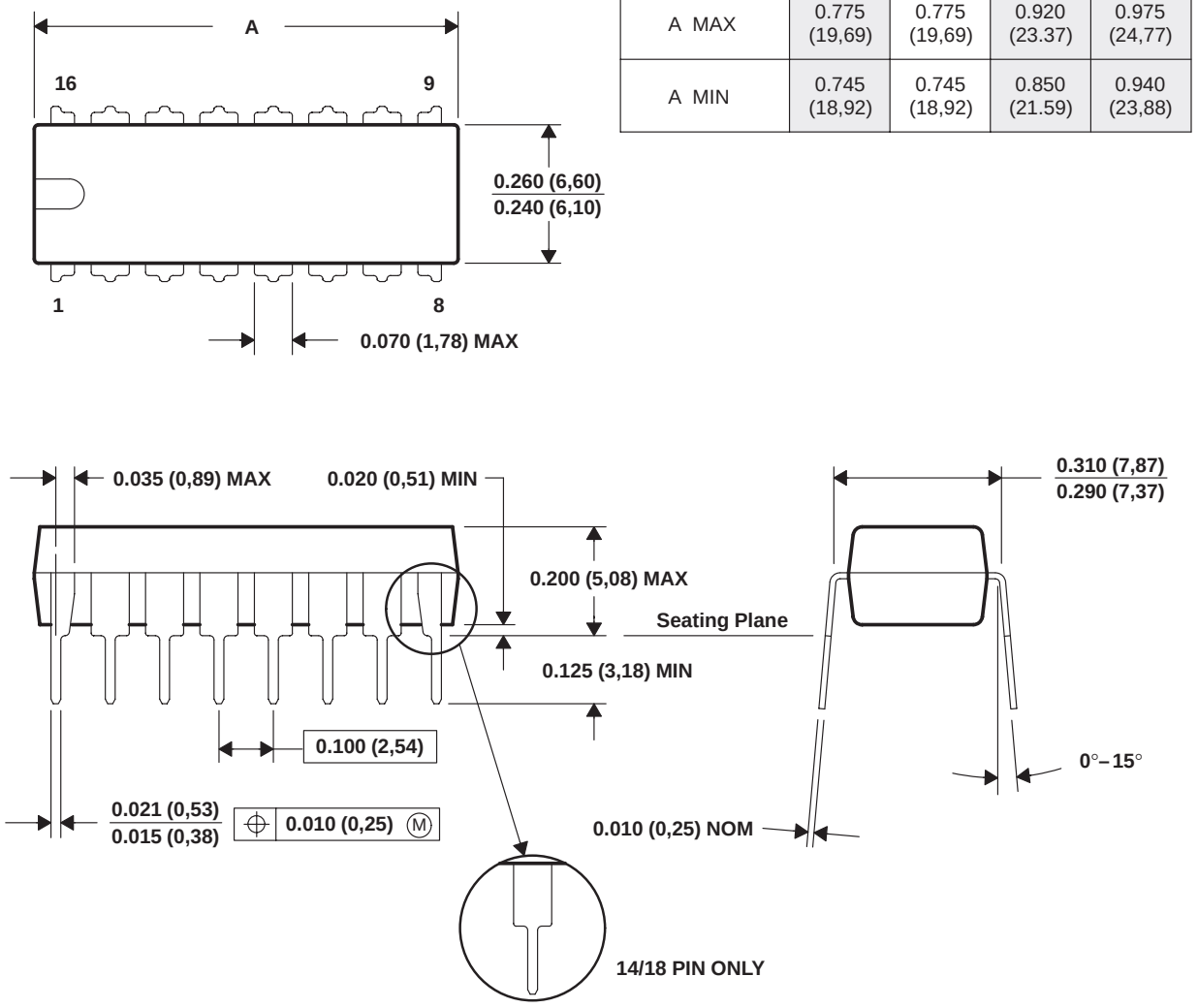
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

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