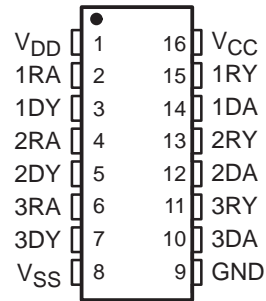


- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Very Low Power Consumption . . . 5 mW Typ**
- **Wide Driver Supply Voltage Range . . .  $\pm 4.5$  V to  $\pm 15$  V**
- **Driver Output Slew Rate Limited to 30 V/ $\mu$ s Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1- $\mu$ s Noise Filter**
- **Functionally Interchangeable With Motorola MC145406 and Texas Instruments TL145406**
- **Package Options Include Plastic Small-Outline (D, DW, NS) Packages and (N) DIPs**

**D, DW, N, OR NS PACKAGE  
(TOP VIEW)**



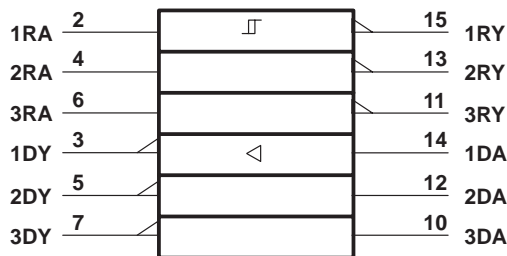
## description

The SN75C1406 is a low-power BiMOS device containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ $\mu$ s, and the receivers have filters that reject input noise pulses shorter than 1  $\mu$ s. Both these features eliminate the need for external components.

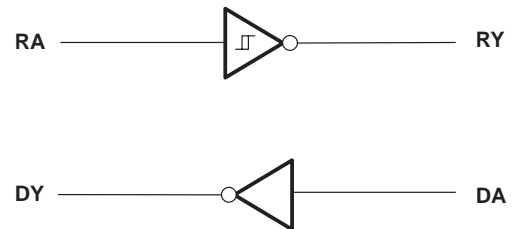
The SN75C1406 is designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C1406 is characterized for operation from 0°C to 70°C.

## logic symbol†



## logic diagram, each driver and receiver



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

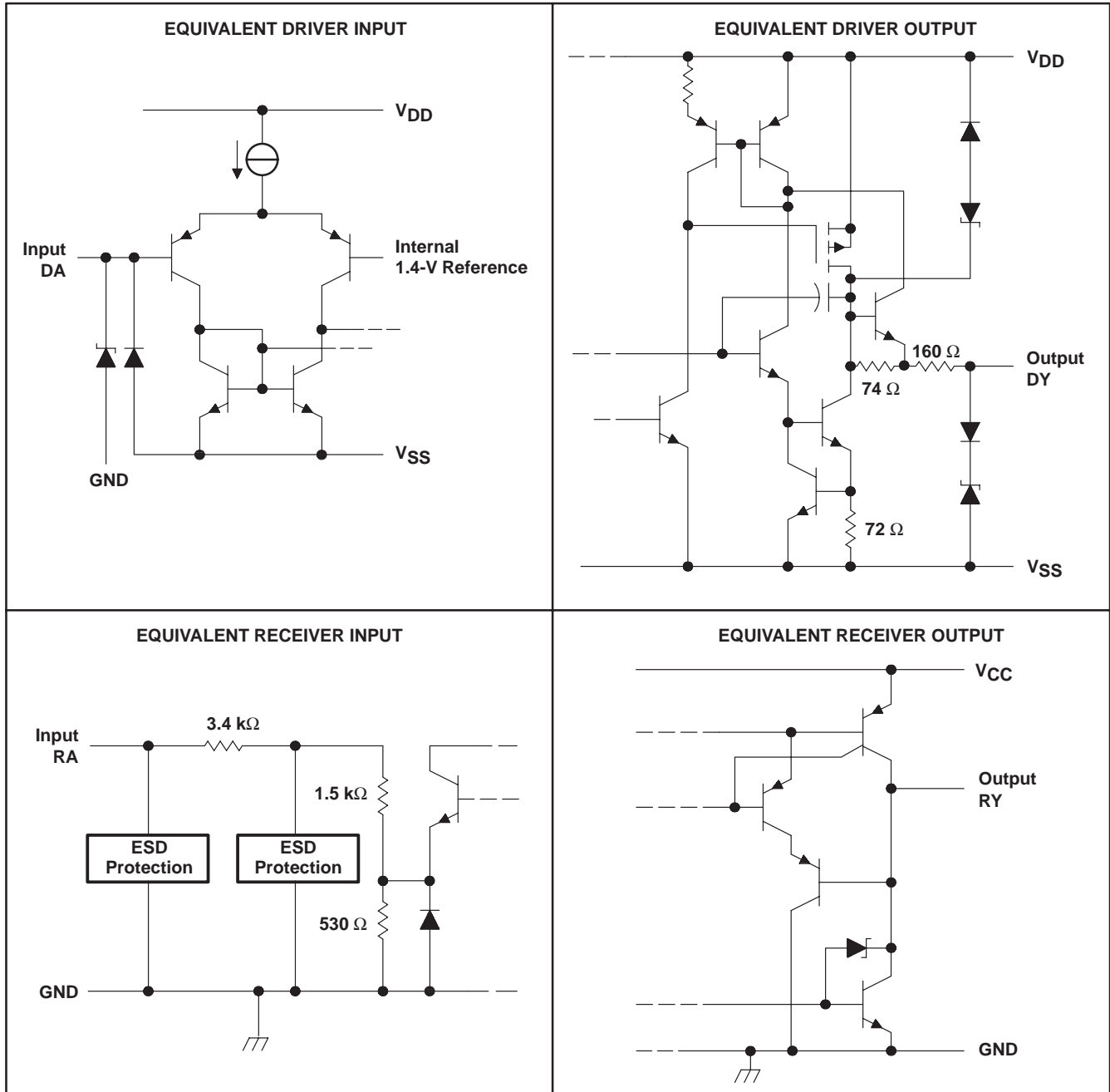


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148D – MAY 1990 – REVISED DECEMBER 1999

## schematics of inputs and outputs



All resistor values shown are nominal.

# SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148D – MAY 1990 – REVISED DECEMBER 1999

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1)	15 V
Supply voltage, $V_{SS}$	-15 V
Supply voltage, $V_{CC}$	7 V
Input voltage range, $V_I$ : Driver	$V_{SS}$ to $V_{DD}$
Receiver	-30 V to 30 V
Output voltage range, $V_O$ : Driver	$(V_{SS} - 6\text{ V})$ to $(V_{DD} + 6\text{ V})$
Receiver	-0.3 V to $(V_{CC} + 0.3\text{ V})$
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DW package	57°C/W
N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150 °C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to the network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$	4.5	12	15	V
Supply voltage, $V_{SS}$	-4.5	-12	-15	V
Supply voltage, $V_{CC}$	4.5	5	6	V
Input voltage, $V_I$	Driver		$V_{SS}+2$	V
	Receiver		$V_{DD}$ $\pm 25$	
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
High-level output current, $I_{OH}$			-1	mA
Low-level output current, $I_{OL}$			3.2	mA
Operating free-air temperature, $T_A$	0		70	°C



# SN75C1406

## TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148D – MAY 1990 – REVISED DECEMBER 1999

### DRIVER SECTION

electrical characteristics over operating free-air temperature range,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 0.8 V, See Figure 1	R <sub>L</sub> = 3 kΩ,	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	4	4.5	V
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	10	10.8	
V <sub>OL</sub>	Low-level output voltage (see Note 3)	V <sub>IH</sub> = 2 V, See Figure 1	R <sub>L</sub> = 3 kΩ,	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	-4.4	-4	V
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	-10.7	-10	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 5 V,	See Figure 2			1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0,	See Figure 2			-1	
I <sub>OS(H)</sub>	High-level short-circuit output current‡	V <sub>I</sub> = 0.8 V, V <sub>O</sub> = 0 or V <sub>SS</sub> ,	See Figure 1	-7.5	-12	-19.5	mA
I <sub>OS(L)</sub>	Low-level short-circuit output current‡	V <sub>I</sub> = 2 V, V <sub>O</sub> = 0 or V <sub>DD</sub> ,	See Figure 1	7.5	12	19.5	mA
I <sub>DD</sub>	Supply current from V <sub>DD</sub>	No load, All inputs at 2 V or 0.8 V		V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	115	250	μA
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	115	250	
I <sub>SS</sub>	Supply current from V <sub>SS</sub>	No load, All inputs at 2 V or 0.8 V		V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	-115	-250	μA
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	-115	-250	
r <sub>O</sub>	Output resistance	V <sub>DD</sub> = V <sub>SS</sub> = V <sub>CC</sub> = 0, See Note 4	V <sub>O</sub> = -2 V to 2 V,	300	400		Ω

† All typical values are at T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time.

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

4. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics at T<sub>A</sub> = 25°C, V<sub>DD</sub> = 12 V, V<sub>SS</sub> = -12 V, V<sub>CC</sub> = 5 V ± 10%

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay time, low- to high-level output§	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 3			1.2	3	μs	
t <sub>PHL</sub>	Propagation delay time, high- to low-level output§				2.5	3.5	μs	
t <sub>TLH</sub>	Transition time, low- to high-level output¶			0.53	2	3.2	μs	
t <sub>THL</sub>	Transition time, high- to low-level output¶			0.53	2	3.2	μs	
t <sub>TLH</sub>	Transition time, low- to high-level output#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 2500 pF, See Figure 3			1	2	μs	
t <sub>THL</sub>	Transition time, high- to low-level output#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 2500 pF, See Figure 3			1	2	μs	
SR	Output slew rate	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 3			4	10	30	V/μs

§ t<sub>PHL</sub> and t<sub>PLH</sub> include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

# Measured between 3-V and -3-V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low



## RECEIVER SECTION

**electrical characteristics over operating free-air temperature range,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	See Figure 5	1.7	2	2.55	V
$V_{IT-}$	Negative-going input threshold voltage	See Figure 5	0.65	1	1.25	V
$V_{hys}$	Input hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		600	1000		mV
$V_{OH}$	High-level output voltage	$V_I = 0.75\text{ V}$ , $I_{OH} = -20\text{ }\mu\text{A}$ , See Figure 5 and Note 5	3.5			V
		$V_I = 0.75\text{ V}$ , $I_{OH} = -1\text{ mA}$ , See Figure 5	$V_{CC} = 4.5\text{ V}$	2.8	4.4	
		$V_{CC} = 5\text{ V}$	3.8	4.9		
		$V_{CC} = 5.5\text{ V}$	4.3	5.4		
$V_{OL}$	Low-level output voltage	$V_I = 3\text{ V}$ , $I_{OL} = 3.2\text{ mA}$ , See Figure 5		0.17	0.4	V
$I_{IH}$	High-level input current	$V_I = 2.5\text{ V}$	3.6	4.6	8.3	mA
		$V_I = 3\text{ V}$	0.43	0.55	1	
$I_{IL}$	Low-level input current	$V_I = -2.5\text{ V}$	-3.6	-5	-8.3	mA
		$V_I = -3\text{ V}$	-0.43	-0.55	-1	
$I_{OS(H)}$	High-level short-circuit output current	$V_I = 0.75\text{ V}$ , $V_O = 0$ , See Figure 4		-8	-15	mA
$I_{OS(L)}$	Low-level short-circuit output current	$V_I = V_{CC}$ , $V_O = V_{CC}$ , See Figure 4		13	25	mA
$I_{CC}$	Supply current from $V_{CC}$	No load, All inputs at 0 or 5 V	$V_{DD} = 5\text{ V}$ , $V_{SS} = -5\text{ V}$	320	450	$\mu\text{A}$
			$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$	320	450	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTE 5: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs remain in the high state.

**switching characteristics at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$ , See Figure 6		3	4	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output			3	4	$\mu\text{s}$
$t_{TLH}$	Transition time, low- to high-level output‡			300	450	ns
$t_{THL}$	Transition time, high- to low-level output‡			100	300	ns
$t_{W(N)}$	Duration of longest pulse rejected as noise§	$C_L = 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$	1		4	$\mu\text{s}$

‡ Measured between 10% and 90% points of output waveform

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of  $t_{W(N)}$  and accepts any positive- or negative-going pulse greater than the maximum of  $t_{W(N)}$ .

PARAMETER MEASUREMENT INFORMATION

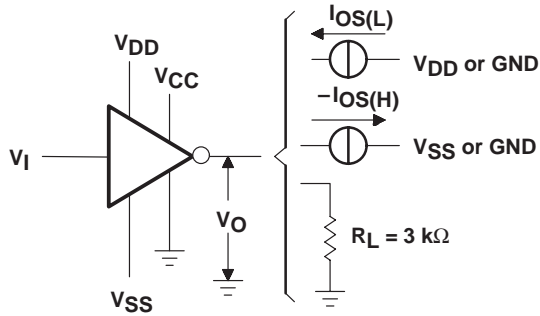


Figure 1. Driver Test Circuit  
 $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(L)}$ ,  $I_{OS(H)}$

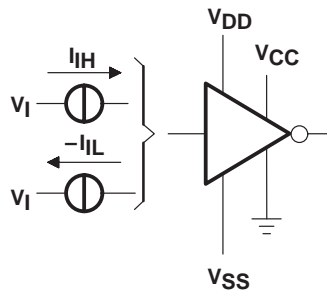
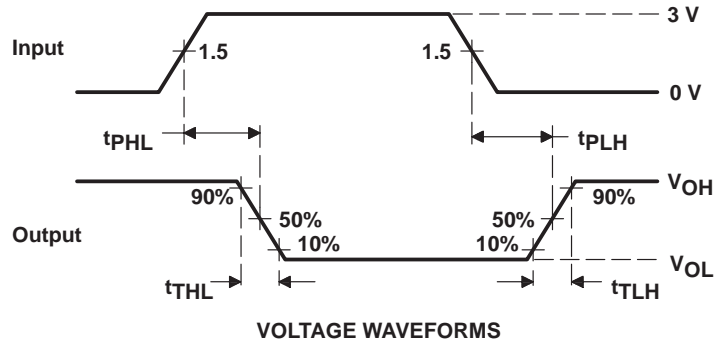
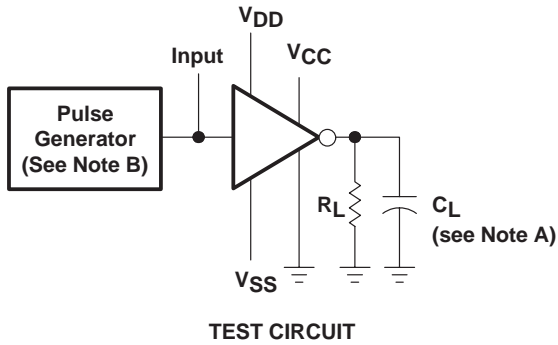


Figure 2. Driver Test Circuit,  $I_{IL}$ ,  $I_{IH}$



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .

Figure 3. Driver Test Circuit and Voltage Waveforms

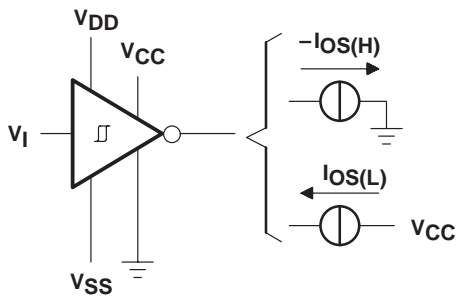


Figure 4. Receiver Test Circuit,  $I_{OS(H)}$ ,  $I_{OS(L)}$

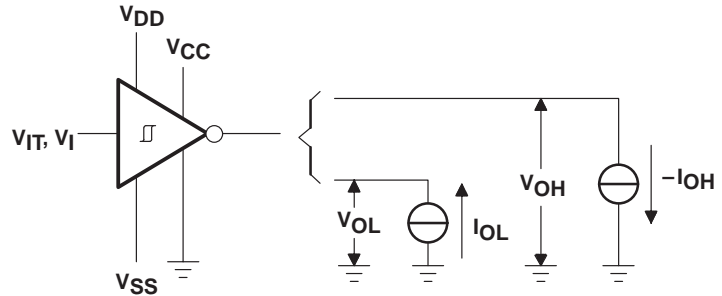
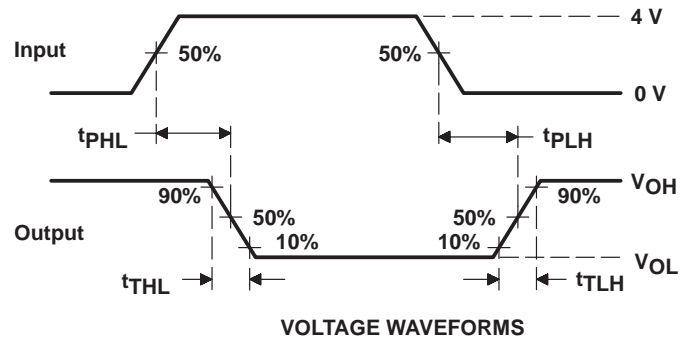
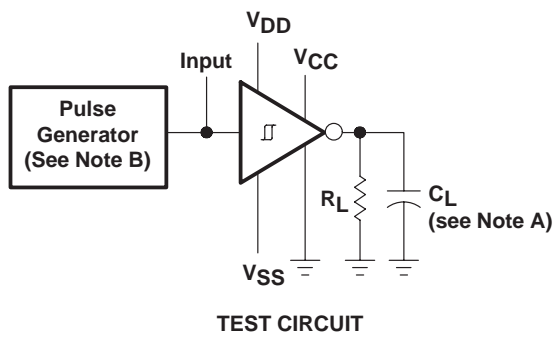


Figure 5. Receiver Test Circuit,  $V_{IT}$ ,  $V_{OL}$ ,  $V_{OH}$

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 ns$ .

Figure 6. Receiver Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

The TIA/EIA-232-F specification is for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. Many TIA/EIA-232-F devices will operate at higher data rates with lower capacitive loads (short cables). For reliable operation at greater than 20 kbit/s, the designer needs to have control of both ends of the cable. By mixing different types of TIA/EIA-232-F devices and cable lengths, errors can occur at higher frequencies (above 20 kbit/s). When operating within the TIA/EIA-232-F requirements of less than 20 kbit/s and with compliant line circuits, interoperability is assured. For applications operating above 20 kbit/s, the design engineer should consider devices and system designs that meet the TIA/EIA-232-F requirements.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.