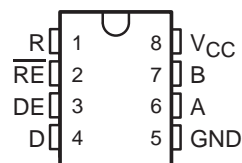


SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Recommended for PROFIBUS Applications
- Operates at Data Rates up to 35 MBaud
- Operating Temperature Range
... -25°C to 85°C
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirement
... 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design
- Package Options Include Plastic Small-Outline (D) Package and (P) DIPs

D† OR P PACKAGE
(TOP VIEW)



† The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65ALS1176DR).

description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS1176 is characterized for operation from -25°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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Function Tables

DRIVERS

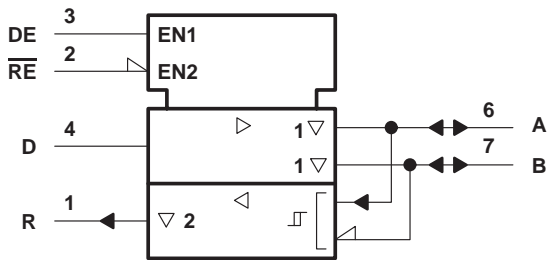
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Inputs open	L	H

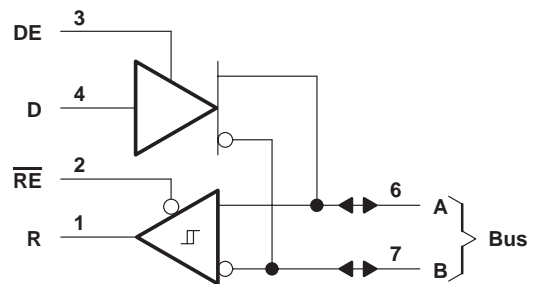
H = high level, L = low level, X = irrelevant,
? = Indeterminate, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

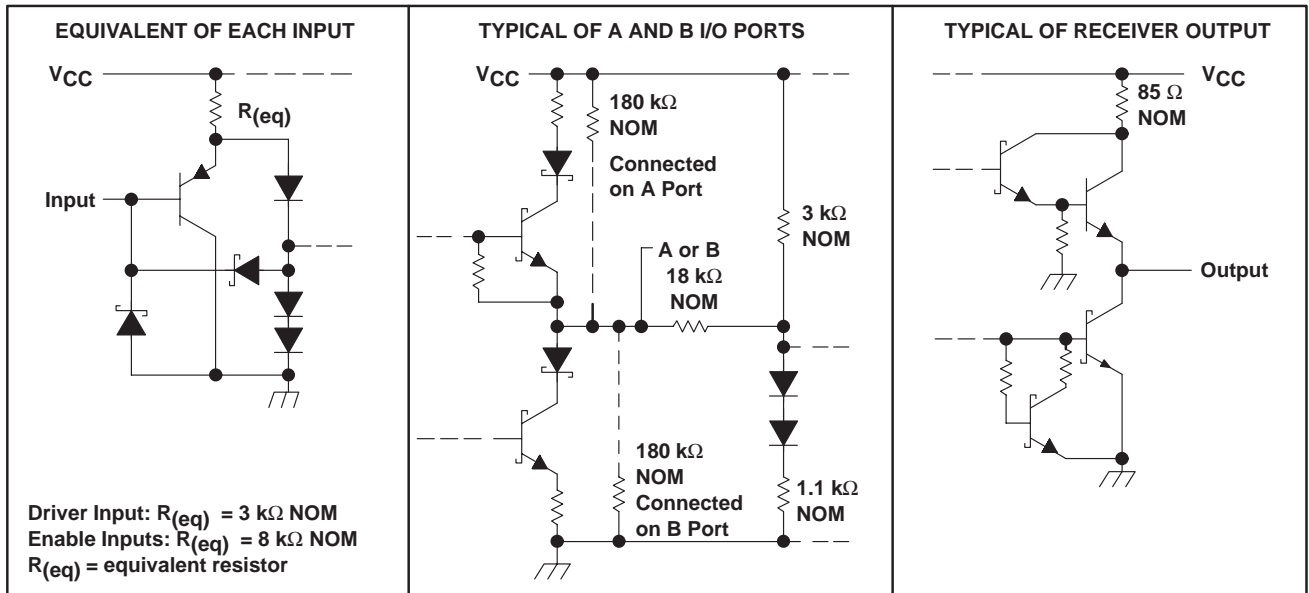
logic diagram (positive logic)



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				-7	V
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}			0.8	V
Differential input voltage, V_{ID} (see Note 3)				± 12	V
High-level output current, I_{OH}	Driver			-60	mA
	Receiver			-400	μ A
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	mA
Operating free-air temperature, T_A		-25		85	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	$1/2 V_{OD1}$ or 2V^{\S}			V
	$R_L = 54 \Omega$, See Figure 1	2.1	2.5	5	V
V_{OD3} Differential output voltage	$V_{\text{test}} = -7 \text{ V to } 12 \text{ V}$, See Figure 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage¶	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage				3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage¶				± 0.2	V
I_O Output current	Outputs disabled, See Note 4	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current#	$V_O = -4 \text{ V}$			-250	mA
	$V_O = 0$			-150	
	$V_O = V_{CC}$			250	
	$V_O = 8 \text{ V}$			250	
I_{CC} Supply current	No load	Outputs enabled	23	30	mA
		Outputs disabled	19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

¶ $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54 \Omega$, See Figure 3	$C_L = 50 \text{ pF}$,			15	ns
$t_{sk(p)}$	Pulse skew‡				0	2	ns
$t_t(OD)$	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level	$R_L = 110 \Omega$, See Figure 4	$C_L = 50 \text{ pF}$,			80	ns
t_{PZL}	Output enable time to low level	$R_L = 110 \Omega$, See Figure 5	$C_L = 50 \text{ pF}$,			30	ns
t_{PHZ}	Output disable time from high level	$R_L = 110 \Omega$, See Figure 4	$C_L = 50 \text{ pF}$,			50	ns
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$, See Figure 5	$C_L = 50 \text{ pF}$,			30	ns

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Pulse skew is defined as the $|t_{pLH} - t_{pHL}|$ of each channel of the same device.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{Os} $	$ V_{Os} $
$\Delta V_{OC} $	$ V_{Os} - \bar{V}_{Os} $	$ V_{Os} - \bar{V}_{Os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}



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DIFFERENTIAL BUS TRANSCEIVER

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5\text{ V}$, $I_O = 8\text{ mA}$	$-0.2\ddagger$			V
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			60		mV
V_{IK} Enable-input clamp voltage	$I_I = -18\text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200\text{ mV}$, See Figure 6	$I_{OH} = -400\text{ }\mu\text{A}$,	2.7		V
V_{OL} Low-level output voltage	$V_{ID} = -200\text{ mV}$, See Figure 6	$I_{OL} = 8\text{ mA}$,		0.45	V
I_{OZ} High-impedance-state output current	$V_O = 0.4\text{ V to } 2.4\text{ V}$			± 20	μA
V_I Line input current	Other input = 0 V, See Note 5	$V_I = 12\text{ V}$		1	mA
		$V_I = -7\text{ V}$		-0.8	
I_{IH} High-level-enable input current	$V_{IH} = 2.7\text{ V}$			20	μA
I_{IL} Low-level-enable input current	$V_{IL} = 0.4\text{ V}$			-100	μA
r_I Input resistance		12	20		k Ω
I_{OS} Short-circuit output current	$V_{ID} = 200\text{ mV}$, $V_O = 0$	-15		-85	mA
I_{CC} Supply current	No load				mA
			Outputs enabled	23 30	
			Outputs disabled	19 26	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
t_{pd} Propagation time	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, $C_L = 15\text{ pF}$, See Figure 7			25	ns	
$t_{sk(p)}$ Pulse skew§			0	2	ns	
t_{PZH} Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 8		11	18	ns	
t_{PZL} Output enable time to low level			11	18	ns	
t_{PHZ} Output disable time from high level					50	ns
t_{PLZ} Output disable time from low level					30	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.



PARAMETER MEASUREMENT INFORMATION

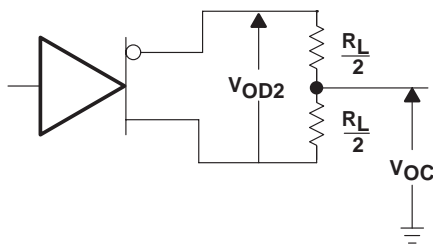


Figure 1. Driver V_{OD2} and V_{OC} Test Circuit

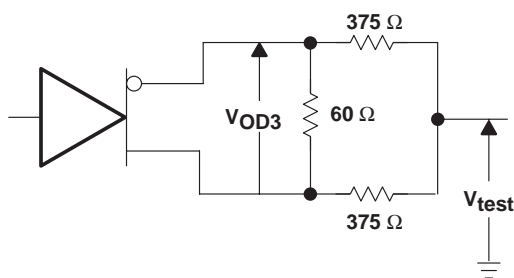
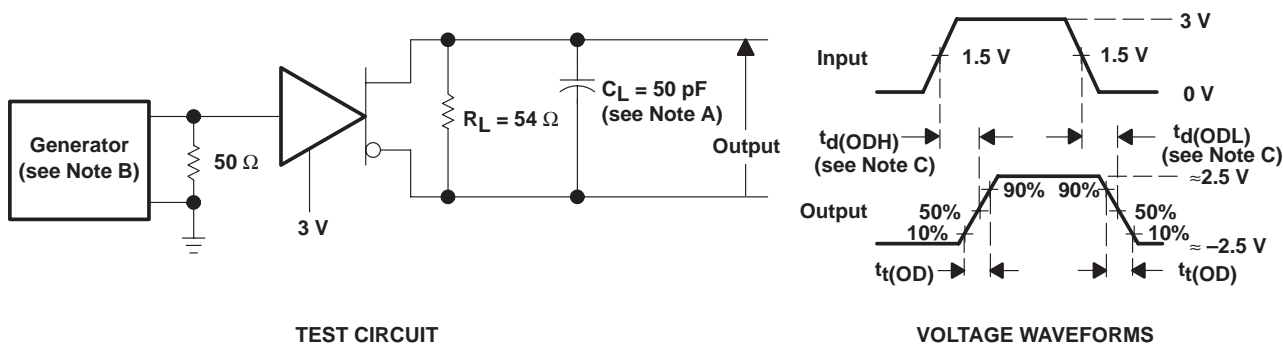


Figure 2. Driver V_{OD3} Test Circuit



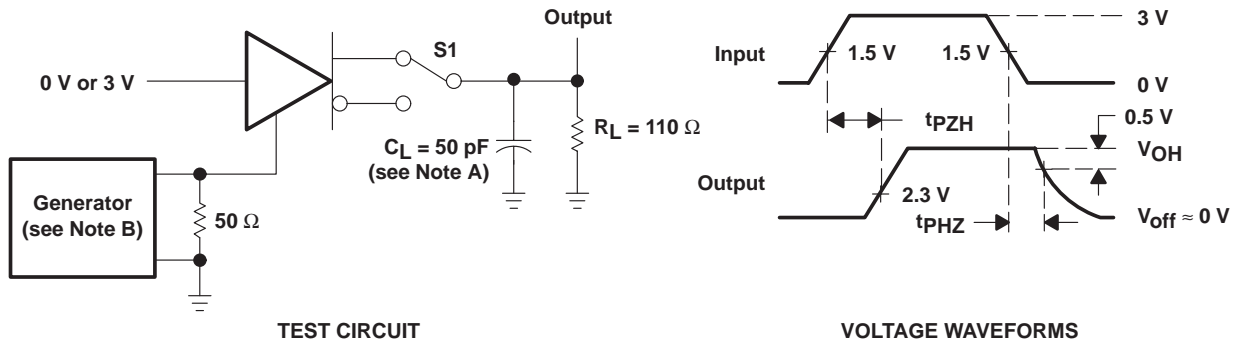
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Differential-Output Delay and Transition Times

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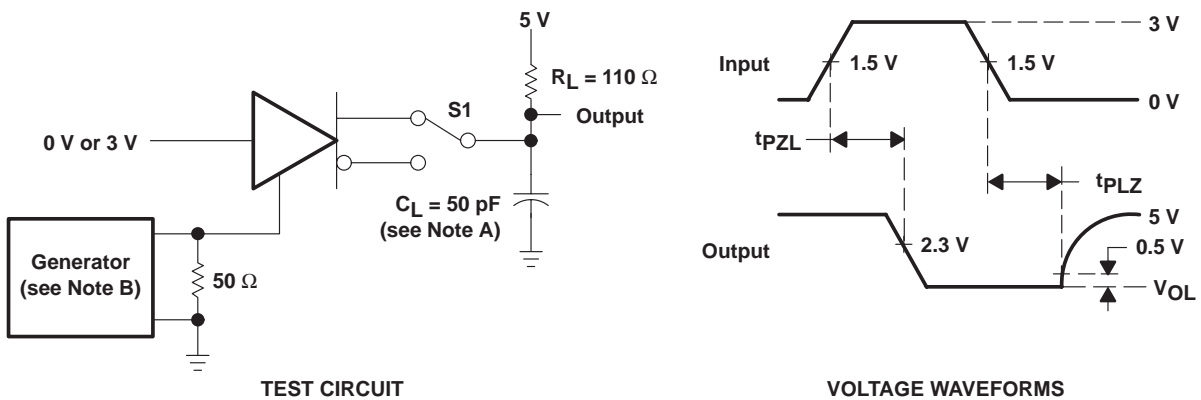
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 4. Driver Enable and Disable Times



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 5. Driver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

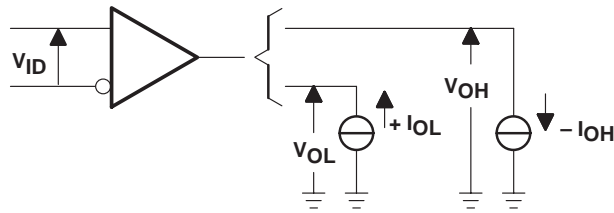
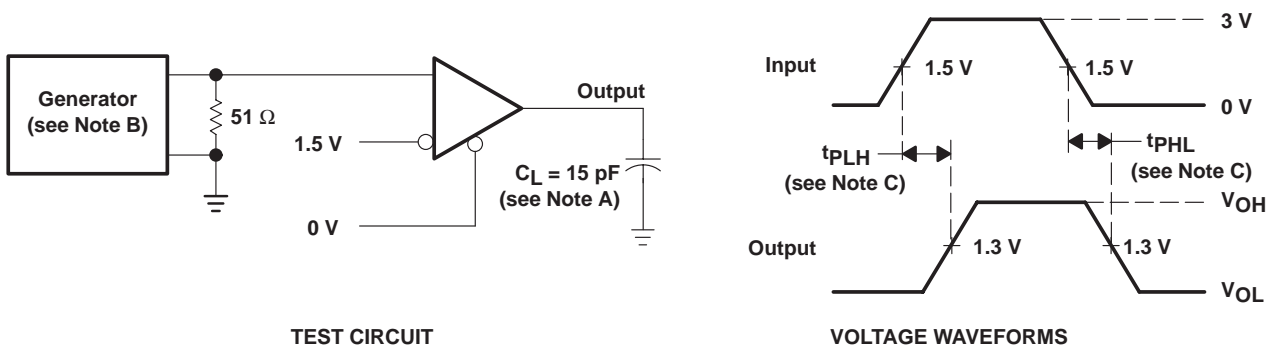


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



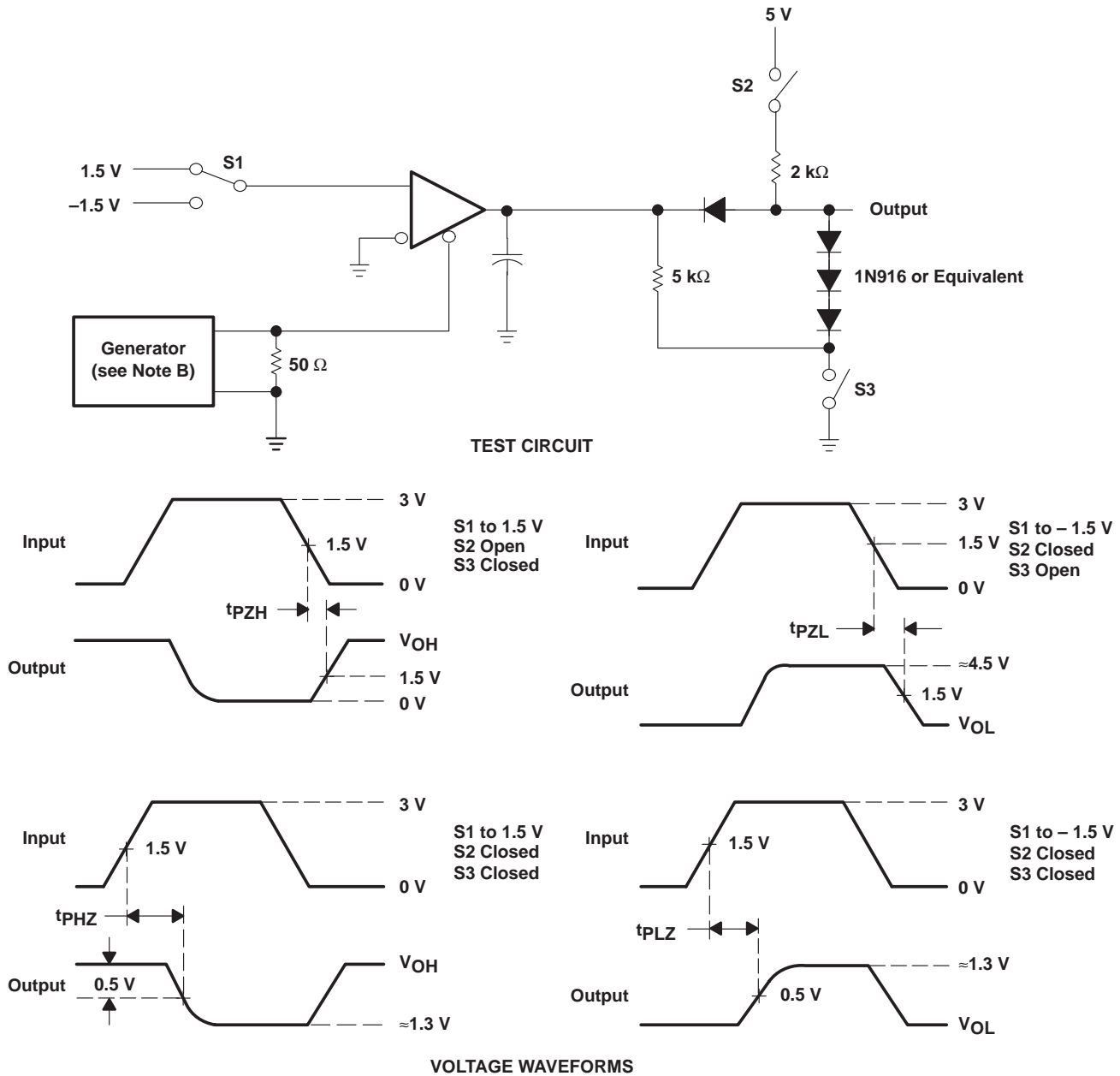
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Propagation-Delay Times

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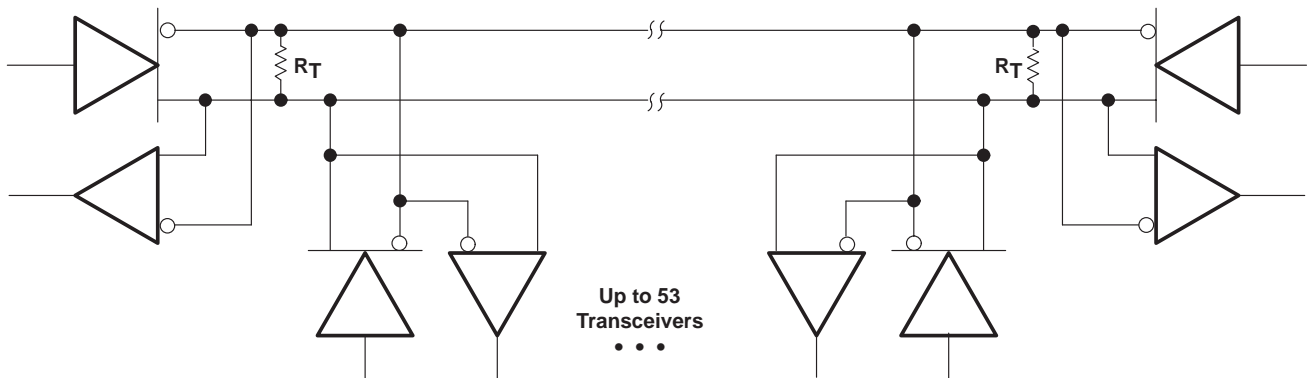
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 8. Receiver Output Enable and Disable Times

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 9. Typical Application Circuit

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