

SN54LV139A, SN74LV139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS396A – APRIL 1998 – REVISED OCTOBER 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

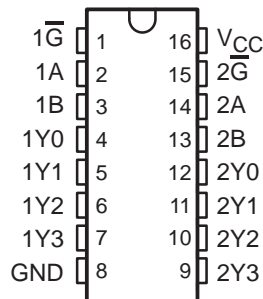
The 'LV139A devices are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V V_{CC} operation.

These devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

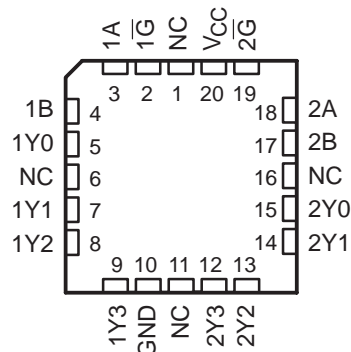
The 'LV139A devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54LV139A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV139A is characterized for operation from -40°C to 85°C .

SN54LV139A . . . J OR W PACKAGE
SN74LV139A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV139A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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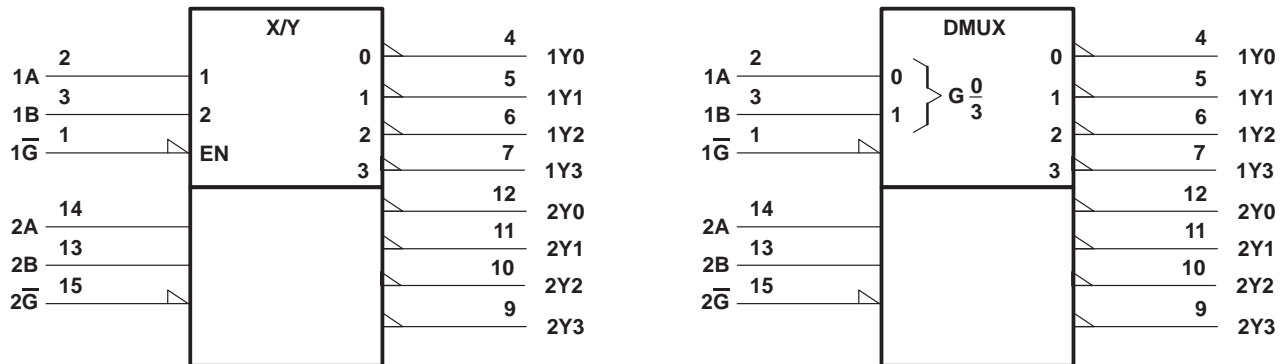
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FUNCTION TABLE

\overline{G}	INPUTS		OUTPUTS			
	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols (alternatives)†

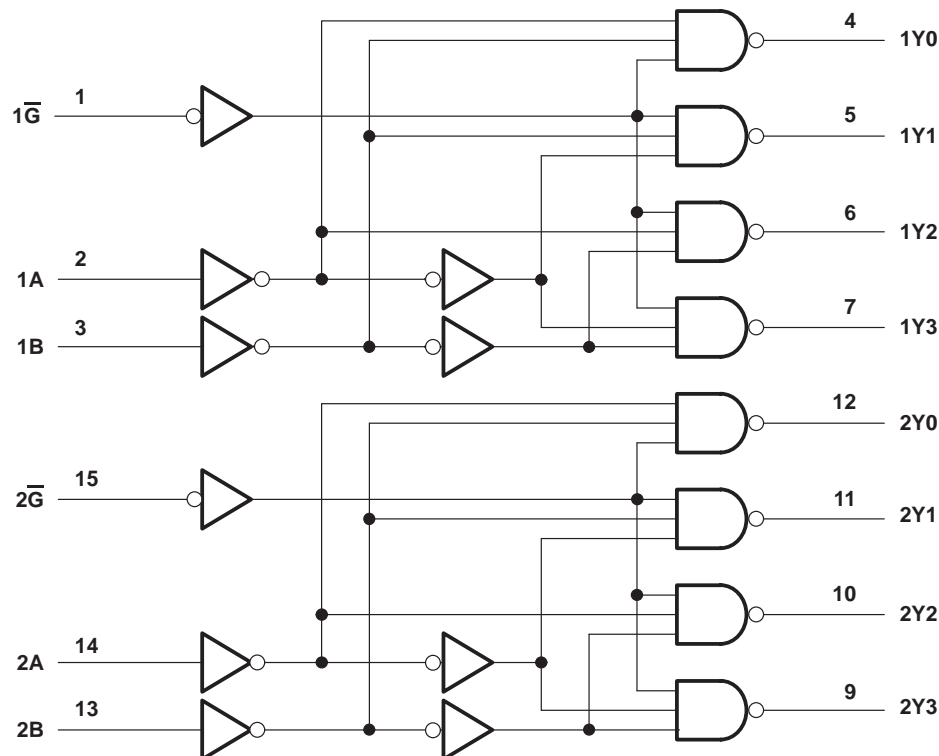


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		SN54LV139A		SN74LV139A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2	5.5	2	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	-50	-50		μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-2	-2		mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-6	-6			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-12	-12			
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	50		μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	2		mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	6	6			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	12	12			
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	200	0	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	100	0	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20	0	20	
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV139A			SN74LV139A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -6\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -12\ \text{mA}$	4.5 V	3.8			3.8			
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V	0.1			0.1			V
	$I_{OL} = 2\ \text{mA}$	2.3 V	0.4			0.4			
	$I_{OL} = 6\ \text{mA}$	3 V	0.44			0.44			
	$I_{OL} = 12\ \text{mA}$	4.5 V	0.55			0.55			
I_I	$V_I = V_{CC}$ or GND	5.5 V	± 1			± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	20			20			μA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0 V	5			5			μA
C_i	$V_I = V_{CC}$ or GND	3.3 V	1.9			1.9			pF

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF	7.7	17.6		1	21	1	21	ns
	\overline{G}	Y		7.4	15.8		1	19	1	19	
t _{pd}	A or B	Y	C _L = 50 pF	10.2	22.5		1	26.5	1	26.5	ns
	\overline{G}	Y		9.9	20.2		1	24	1	24	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF	5.3	11		1	13	1	13	ns
	\overline{G}	Y		5.1	9.2		1	11	1	11	
t _{pd}	A or B	Y	C _L = 50 pF	7.3	14.5		1	16.5	1	16.5	ns
	\overline{G}	Y		7	12.7		1	14.5	1	14.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV139A		SN74LV139A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	Y	C _L = 15 pF	3.7	7.2		1	8.5	1	8.5	ns
	\overline{G}	Y		3.5	6.3		1	7.5	1	7.5	
t _{pd}	A or B	Y	C _L = 50 pF	5.2	9.2		1	10.5	1	10.5	ns
	\overline{G}	Y		4.9	8.3		1	9.5	1	9.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	3.3 V	17.3	pF
			5 V	18.2	

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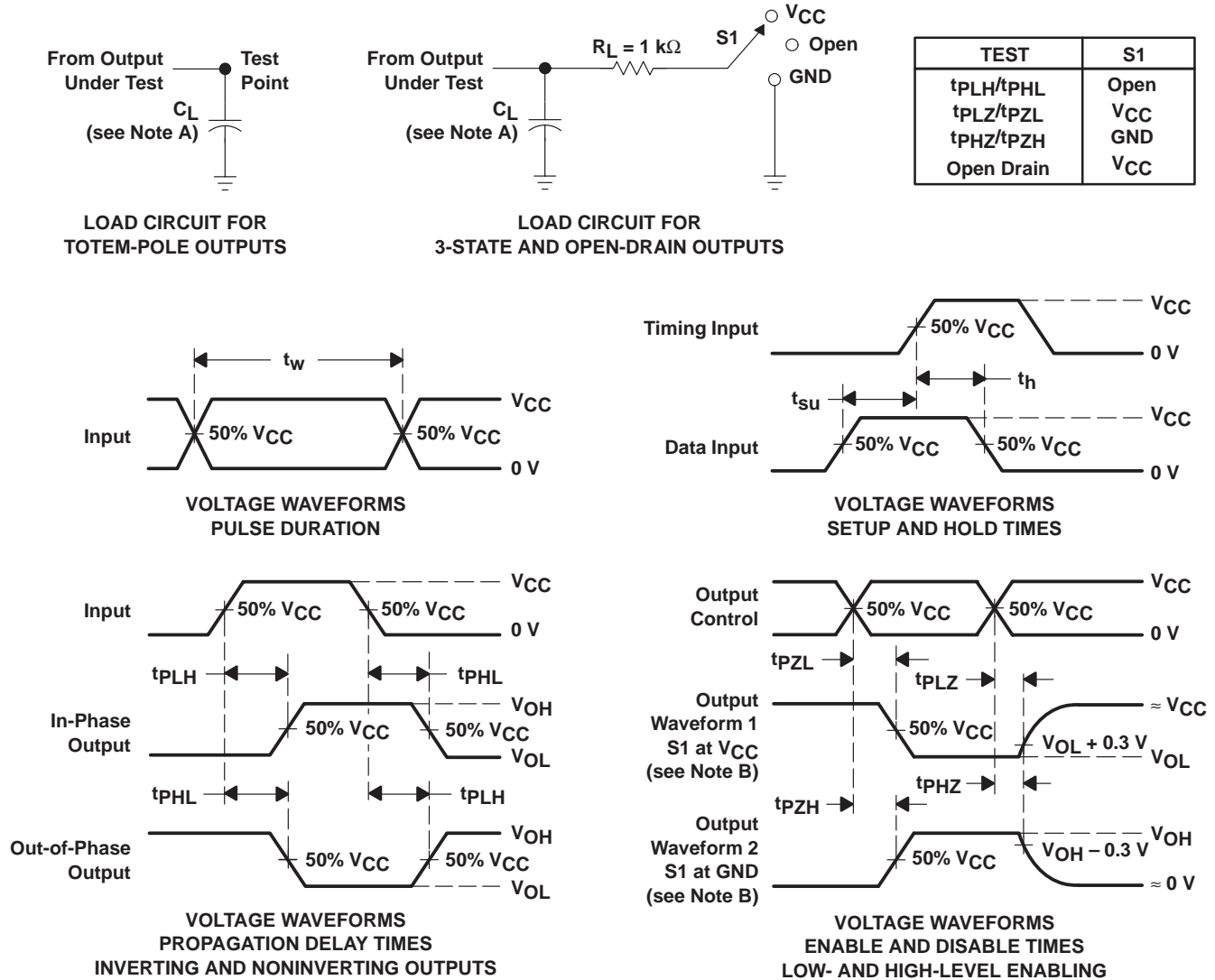


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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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