UNITRODE

18-Line SCSI Terminator (Reverse Disconnect)

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50µA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- –650mA Sourcing Current for Termination
- Trimmed Impedance to 5%

DESCRIPTION

The UCC5617 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5609, the UCC5617 is ideal for high performance 5V SCSI systems, Termpwr 4.0V to 5.25V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5617 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5617 to source full termination current and sink active negation current when all termination lines are actively negated.

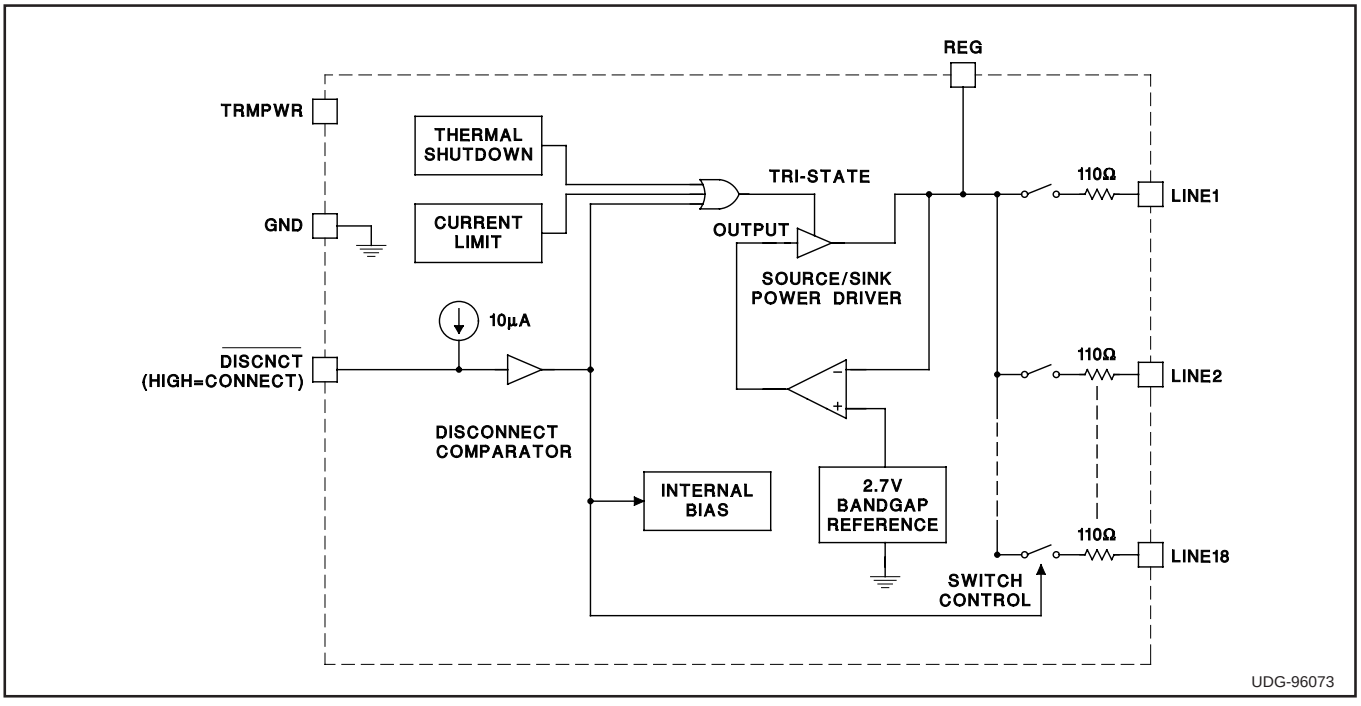
The UCC5617, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, TSSOP and PLCC.

BLOCK DIAGRAM



Circuit Design Patented

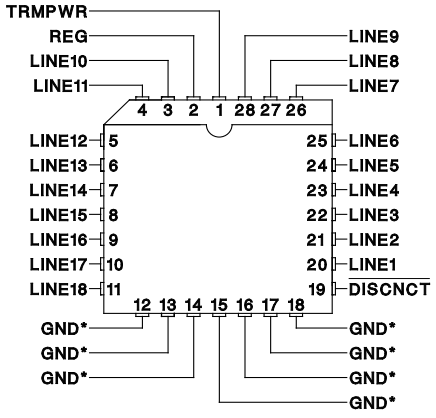
ABSOLUTE MAXIMUM RATINGS

Tempwr . . . . . .+7V
Signal Line Voltage . . . . . .0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . .–65°C to +150°C
Operating Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . .300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

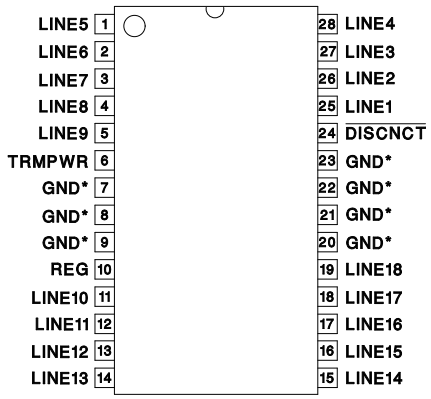
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



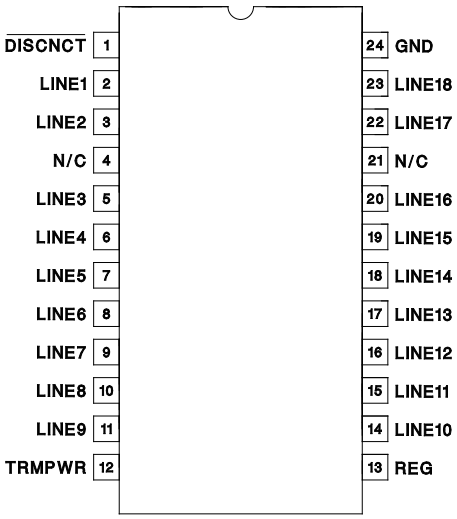
** DWP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



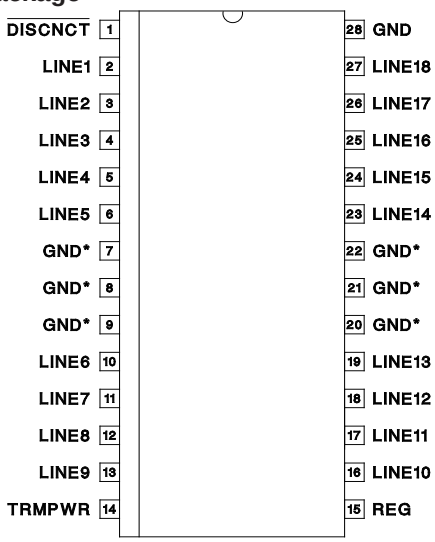
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21, and 22 serve as heatsink ground.*

DIL-24 (Top View)
N Package



** N package for engineering samples only.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*
Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{DISCNCT}$ = 4.75V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		420	450	mA
Power Down Mode	$\overline{DISCNCT}$ = 0V		50	100	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Maximum Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{DISCNCT}$ = 0V, TRMPWR = 0V to 5.25V, REG = 0.2V, V_{LINE} = 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 2.4V (Note 2)		2	3.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–475	–650	–850	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	800	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	$\overline{DISCNCT}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculating:

$$Z = \frac{V_{OUT}\ \text{N.L.} - 0.2V}{I_{OUT}\ \text{at}\ 0.2V}.$$

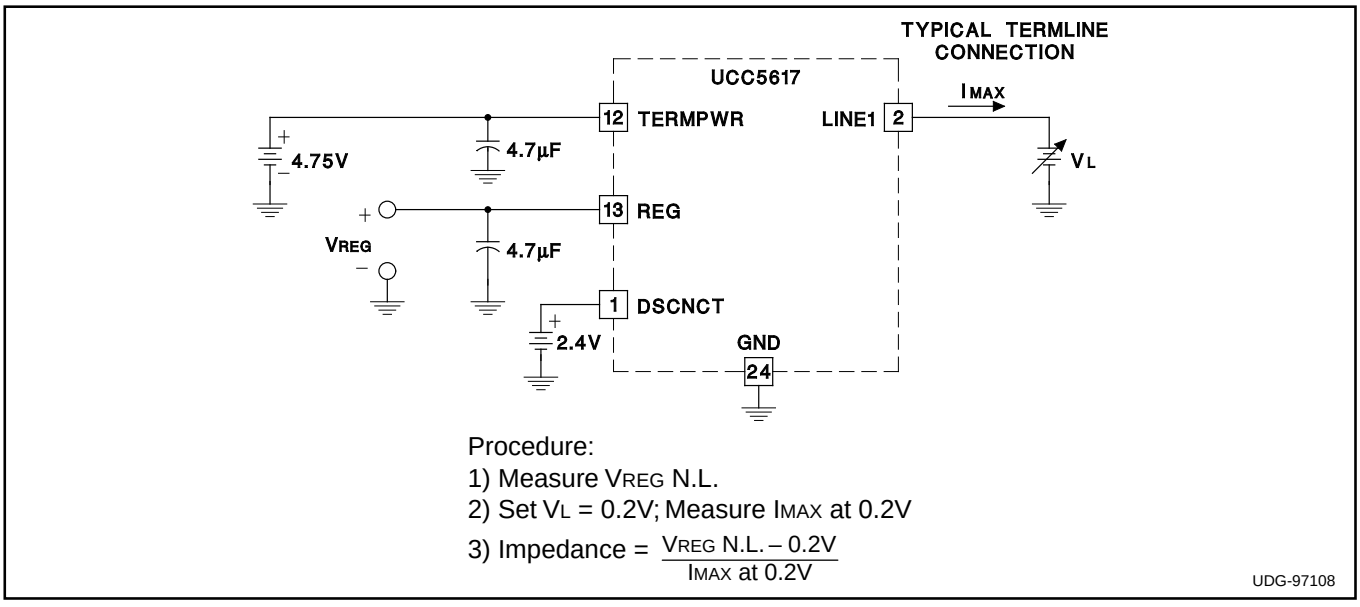


Figure 1. Termline Impedance Measurement Circuit

PIN DESCRIPTIONS

DISCNCT: Taking this pin low causes the 18 channels to become high impedance and the chip to go into low-power mode; a high or open state allows the channels to provide normal termination.

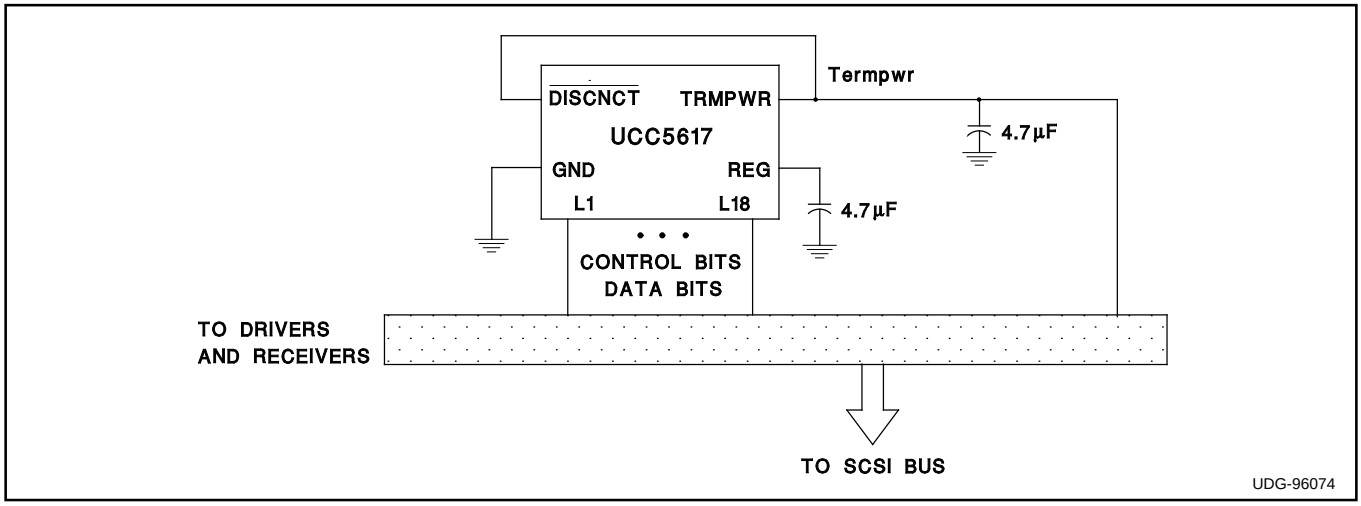
GND: Ground reference for the IC.

LINE 1-18: 110Ω termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

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