UNITRODE

UCC1890
UCC2890
UCC3890

Off-Line Battery Charger Circuit

FEATURES

- Transformerless Off-Line Operation
- Low Voltage Operation to 0.8V
- Ideal for Battery Trickle Charger Applications
- Current Mode Operation With 100mV Shunt
- Voltage Mode Operation With Fixed 1.25V Output or Resistor Adjustable Output
- Efficient BiCMOS Design
- Inherent Short Circuit Protection

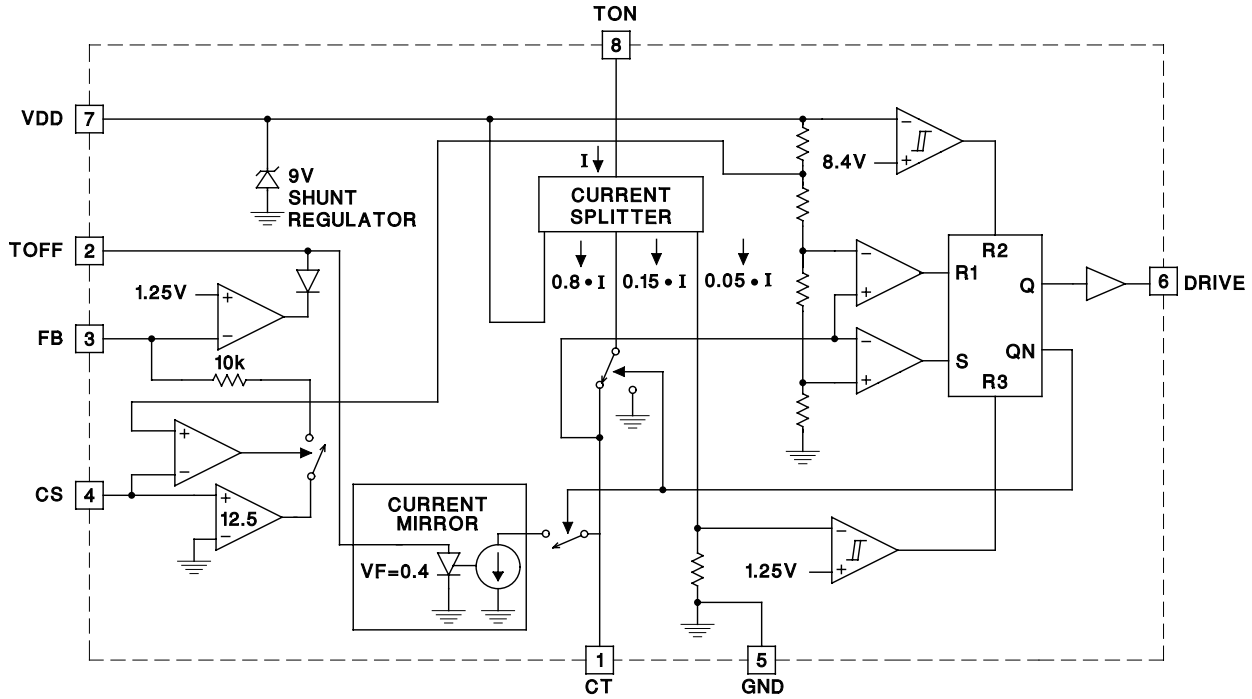
DESCRIPTION

The UCC3890 controller is optimized for use as an off-line, low power, low voltage, regulated current supply, ideally suited for battery trickle charger applications. The unique circuit topology used in this device can be visualized as two cascaded flyback converters; each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to charge low voltage batteries in off-line applications with no transformer, and low internal losses.

The control algorithm used by the UCC3890 forces a switch on time inversely proportional to the input line voltage, while the switch off time is inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a large voltage conversion ratio with reasonable switch duty cycle.

While the UCC3890 is ideally suited for control of constant current battery chargers, provision is also made to operate as a fixed 1.25V regulated supply, or to use a resistor voltage divider to obtain output voltages higher than 1.25V.

BLOCK DIAGRAM



Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-96052

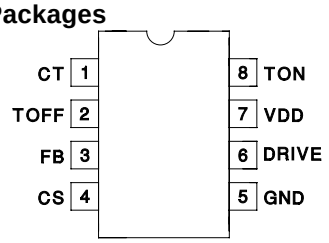
ABSOLUTE MAXIMUM RATINGS

I_{DD} 7.5mA
Current into TON 7.5mA
Voltage on V_{OUT} 20V
Current into TOFF 250µA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1890, –40°C to 85°C for the UCC2890, and 0°C to 70°C for the UCC3890. No load at DRIVE pin (C_{LOAD} = 0), T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VDD Zener Voltage	I_{DD} = 4.75mA, I_{TON} = 0mA	8.3	9.0	9.4	V
Minimum Operating Current I_{TON}	I_{DD} = –1mA, F = 150kHz		1.65	2.0	mA
Undervoltage Lockout					
Minimum Voltage to Start	FB = 0	7.8	8.6	9.2	V
Minimum Voltage after Start	FB = 0	5.75	6.3	6.65	V
Hysteresis	FB = 0	1.8	2.3	2.6	V
VDD – V_{START}	FB = 0	0.2	0.4	0.7	V
Oscillator					
Amplitude	I_{TON} = 3mA; I_{TOFF} = 50µA; V_{FB} = 0V CT = 100pF	3.1	3.4	3.7	V
CT to DRIVE High Delay	Overdrive = 200mV		80	200	ns
CT to DRIVE Low Delay	Overdrive = 200mV		50	100	ns
Charge Coefficient I_{CT}/I_{TON}	I_{TON} = 3mA; V_{CT} = 3.0V	0.135	0.15	0.165	µA/µA
Discharge Coefficent I_{CT}/I_{TOFF}	I_{TOFF} = 50µA; V_{CT} = 3.0V	0.95	1.00	1.05	µA/µA
Driver					
V_{OL}	I = 100mA (Note 1)		0.7	1.8	V
V_{OH}	I = –100mA referred to VDD (Note 1)	–2.9	–1.5		V
Rise Time	C_L = 1nF		35	70	ns
Fall Time	C_L = 1nF		30	60	ns
Line Voltage Detection					
Minimum I_{TON} for Fault		1.0	1.5	2.0	mA
I_{TON} Detector Hysteresis			110		µA
On Time During Fault			0.5		µs
V_{OUT} Error Amplifier					
Reference Level	I_{TOFF} = 50µA, I_{CT} = 25µA, T_J = 25°C	1.20	1.25	1.30	V
	I_{TOFF} = 50µA, I_{CT} = 25µA, Over Temperature	1.15	1.25	1.35	V
Voltage at TOFF	I_{TOFF} = 50µA	0.3	0.4	0.5	V
Regulation gm	I_{TOFF} = 50µA (Note 2)	2.0	4.0	7.7	mA/V
Current Sense Amplifier					
Gain	V_{CS} = 90 – 110mV	11.8	12.5	13.0	V/V
Input Offset Voltage	V_{CS} = 90 – 110mV	–5	0	5	mV
Input Voltage for CS Amplifier Enabled	I_{TON} = 3mA, Referred to VDD	–1.5	–0.8		V
Input Voltage for CS Amplifier Disabled	I_{TON} = 3mA, Referred to VDD		–0.8	–0.3	V

Note 1: VDD forced to 100mV below VDD Zener Voltage

Note 2: gm is defined as $\frac{\Delta ICT}{\Delta VFB}$ *for the values of V_{FB} where the error amp is in regulation. The two points used to calculate gm are for I_{CT} at 65% amd 35% of its maximum value.*

PIN DESCRIPTIONS

CS: The high side of the current sense shunt is connected to this pin. Short CS to VDD for voltage feedback operation.

CT: Oscillator timing capacitor is connected to this pin.

DRIVE: Gate drive to external power switch.

FB: Output of current sense amplifier. This pin can be used for direct output voltage feedback if the current sense amp input pin CS is shorted to the VDD pin.

GND: Ground pin.

TOFF: Resistor ROFF connects from voltage output to this pin to provide a maximum capacitor discharge current proportional to output voltage.

TON: Resistor RON connects from line input to this pin to provide capacitor charge current proportional to line voltage. The current in RON also provides power for the 9V shunt regulator at VDD.

VDD: Output of 9V shunt regulator.

APPLICATION INFORMATION

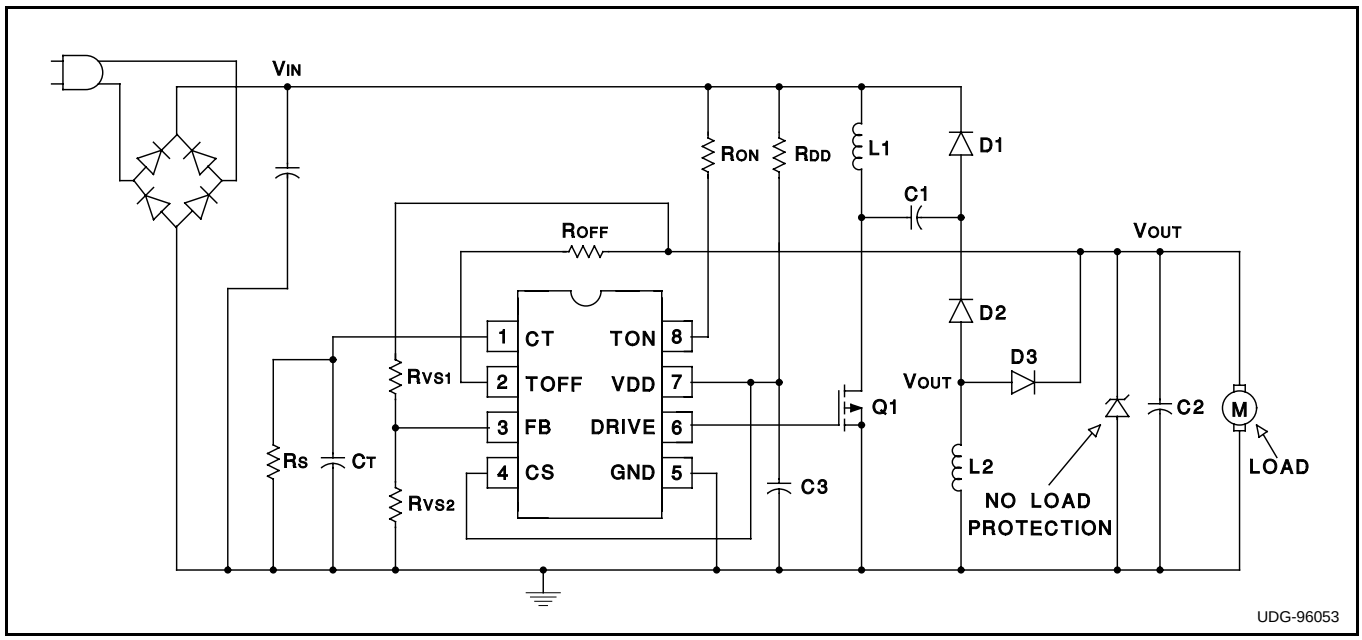


Figure 1. Typical Voltage Mode Application

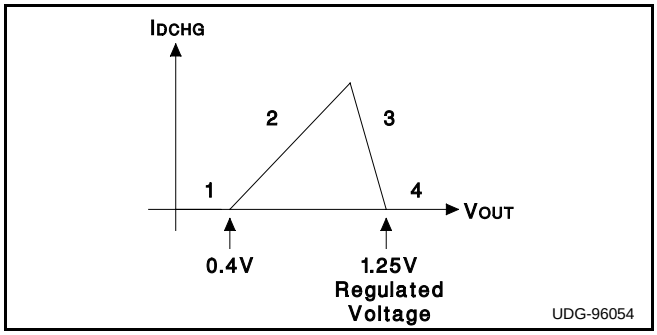
OPERATION (VOLTAGE OUTPUT)

Figure 1 shows a typical voltage mode application. When input voltage is first applied, all of the current through RDD and 80% of the current through RON, charge the external capacitor C3 connected to VDD. As the voltage builds on VDD, undervoltage lockout holds the circuit off and the output DRIVE low until VDD reaches 8.4V. At this time, DRIVE goes high, turning on the external power switch Q1, and 15% of the current into TON is directed to the timing capacitor CT. The voltage at TON is fixed at approximately 11V, so CT charges to a fixed threshold with current

$$I = 0.2 \bullet \frac{V_{IN} - 11V}{R_{ON}}$$

Since the input line is much greater than 11V, the charge current is approximately proportional to the input line voltage. DRIVE is only high while CT is charging, so the power switch on time is inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

At the end of the switch on time, Q1 is turned off, and the 15% of the RON current which was charging CT is diverted to ground. The power switch off time is controlled by discharge of CT, which is determined by the outut voltage as described here:



APPLICATION INFORMATION (cont.)

1. When V_{OUT} = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, R_S, is placed in parallel with C_T to establish a minimum switching frequency.

2. As V_{OUT} rises above approximately 0.4V, I_{DCHG} is set by R_{OFF}, and is defined by

$$I_{DCHG} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

   As V_{OUT} increases, I_{DCHG} increases resulting in the reduction of off time. The frequency of operation increases and V_{OUT} rises quickly to its regulated value.

3. In this region, a transconductance amplifier reduces I_{DCHG} in order to maintain V_{OUT} in regulation. The input to the transconductance amplifier is the pin FB. (In this mode the pin CS should be shorted to VDD.) FB can either be connected directly to V_{OUT} to regulate at nominal V_{OUT} = 1.25V or to be connected to V_{OUT} through a resistor divider R_{VS1}/R_{VS2} to regulate at nominal

$$V_{OUT} = \frac{1.25V \bullet (R_{VS1} + R_{VS2})}{R_{VS2}}$$

4. If V_{OUT} should rise above its regulation range, I_{DCHG} falls to zero and the circuit returns to the minimum frequency established by R_S and C_T.

   The range of switching frequencies is established by R_{ON}, R_{OFF}, R_S, and C_T as follows:

$$\text{Frequency} = \frac{1}{TON + TOFF}$$

$$TON = \frac{CT \bullet 3.4V \bullet 0.15 \bullet R_{ON}}{V_{IN} - 11V}$$

$$TOFF_{(MAX)} = 1.5 \bullet R_S \bullet C_T \text{ (regions1 and 4)}$$

$$TOFF = \frac{C_T \bullet 3.4V \bullet R_{OFF}}{V_{OUT} - 0.4V} \text{ (region 2)}$$

The above equations assume VDD = 9, the voltage at TON = 11V, the voltage at TOFF = 0.4V.

OPERATION (CURRENT OUTPUT)

Figure 2 shows a typical current mode application. In current mode, operation is the same as in voltage mode, except that in region 3 the transconductance amplifier is controlled by the current sense amplifier which senses the voltage across a shunt resistor R_{SH}. The circuit then regulates the current in the shunt to the nominal value

$$I_{SH} = \frac{100mV}{R_{SH}}$$

The circuit shown in this schematic would be suitable for an application which trickle charges a battery at a low current, (e.g. C/10), and has a battery load which draws a high current, (e.g. C), when turned on. In that case, R_{SH1} value is chosen so that

$$\frac{100mV}{R_{SH1}} = \frac{C}{10}$$

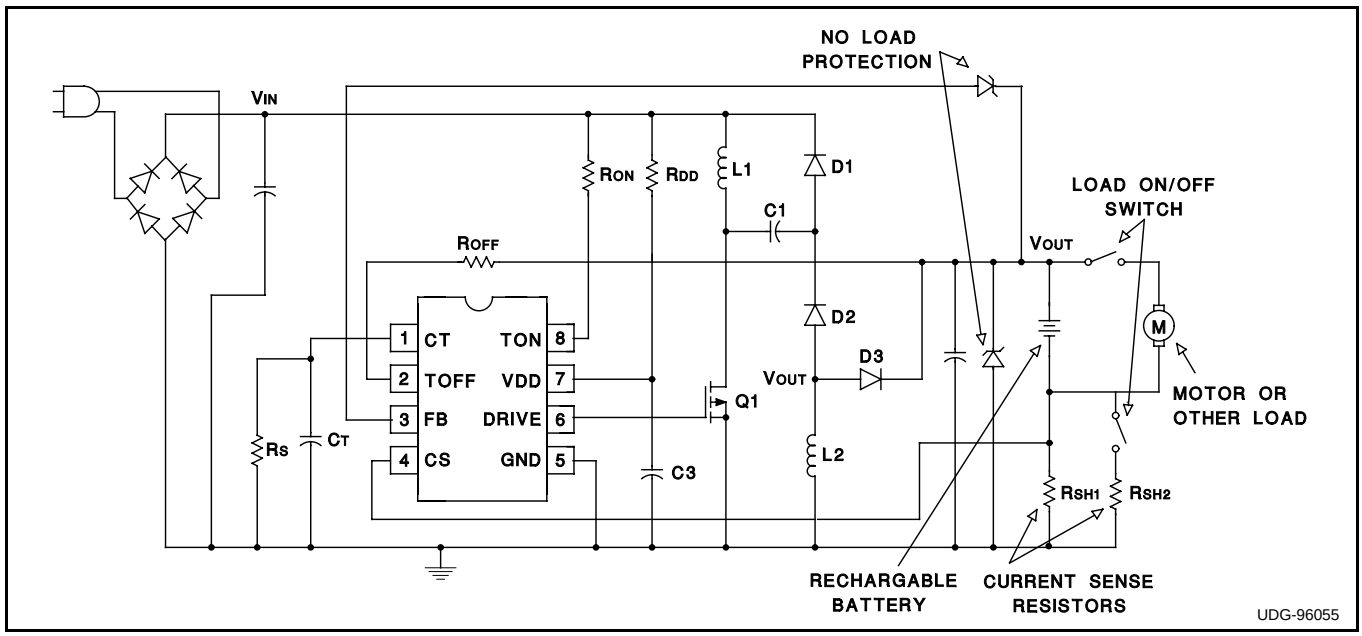


Figure 2. Typical Current Mode Application

APPLICATION INFORMATION (cont.)

If R_{SH2} is chosen so that

$$\frac{100mV}{R_{SH2}} = C$$

then the regulator output will assist the battery, minimizing or eliminating battery output current.

DESIGN EXAMPLE

A typical design has the following requirements:

V_{IN}	=	80 to 132 VAC or 100 to 180 VDC
V_{OUT}	=	1.25V
V_{OUT}'	=	2.0V (assumes 1.25 V_{OUT} with 750mV forward drop in D3)
I_{LOAD}	=	500mADC max
$F_{SWITCHING}$	=	100kHz
η (eff.)	=	50% (excluding efficiency losses in D3 which will be very large due to the low output voltage. Losses in D3 are accounted for by using V_{OUT}' in the calculations).

Component values are indicated in Figure 3. The explanation for the choices in component values follows.

First calculate the maximum duty cycle, d(max). To calculate this assume that at maximum load/minimum line conditions, the converter will be at the continuous conduction boundary and there will be no idle time after the inductors are discharged. For all other load/line conditions, the UCC3890 will stretch the off time, to create an idle time after the inductors are discharged, in order to maintain a constant output voltage. For a single flyback stage at continuous conduction boundary

$$d = \frac{1}{1 + \frac{V_{IN}}{V_{OUT}}}$$

For the cascaded flyback stages of the UCC3890 topology, the corresponding equation is

$$d(max) = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}'}}}$$

in this case

$$d(max) = \frac{1}{1 + \sqrt{\frac{100V}{2V}}} = 0.125$$

Next using the operating frequency and the maximum duty cycle to calculate the maximum on time

$$TON(max) = \frac{d(max)}{F_{SWITCHING}}$$

in this case

$$TON(max) = \frac{0.125}{100kHz} = 1.25\mu s$$

correspondingly

$$TOFF(min) = \frac{1 - 0.125}{100kHz} = 8.75\mu s$$

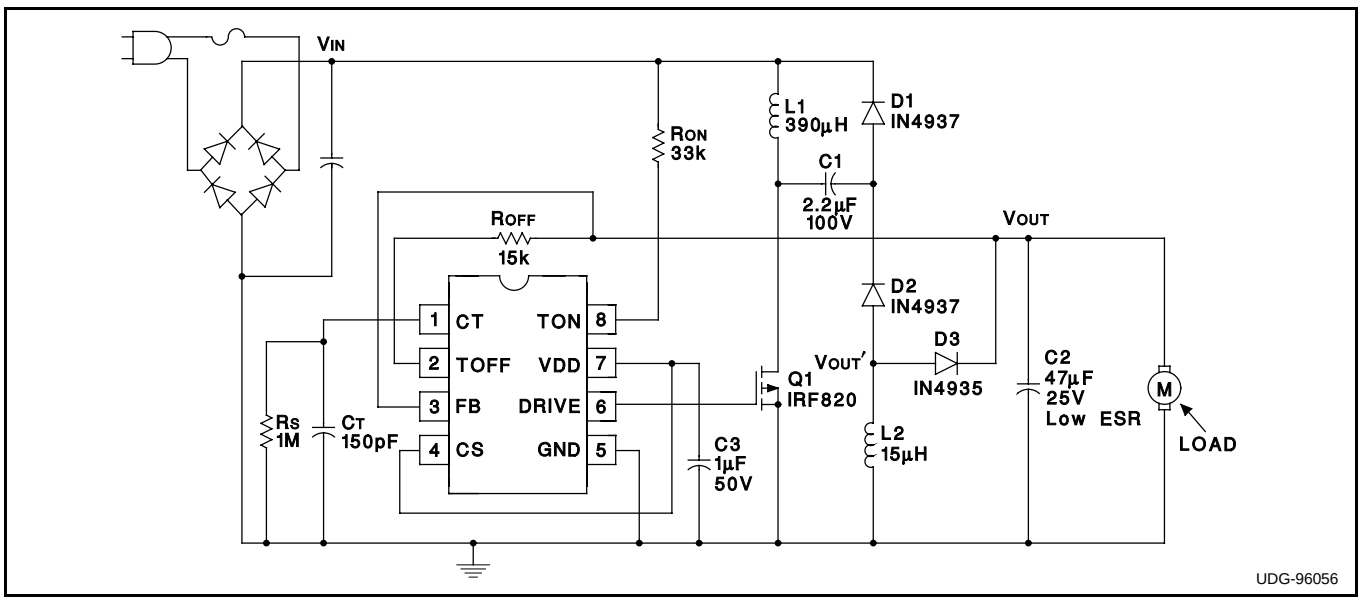


Figure 3. Example Application

APPLICATION INFORMATION (cont.)

The average input current at minimum line and maximum load will be

$$I_{IN} = \frac{I_{OUT}}{\eta} \bullet \frac{V_{OUT}'}{V_{IN}}$$

in this case

$$I_{IN} = \frac{500mA}{0.5} \bullet \frac{2V}{100V} = 20mA$$

Knowing that input current is drawn from the line only during TON, calculate the peak current in L1 to be

$$I_{L1}(pk) = 2 \bullet I_{IN} \bullet \frac{TON + TOFF}{TON}$$

in this case

$$I_{L1}(pk) = 2 \bullet 20mA \bullet \frac{1.25\mu s + 8.75\mu s}{1.25\mu s} = 320mA$$

Now calculate the value for L1

$$L_1 = V_{IN} \bullet \frac{TON}{I_{L1}(pk)}$$

in this case

$$L_1 = 100V \bullet \frac{1.25\mu s}{320mA} = 390\mu H$$

The output voltage of the first flyback stage is

$$V_{C1} = V_{IN} \bullet \frac{TON}{TOFF}$$

in this case

$$V_{C1} = 100V \bullet \frac{1.25\mu s}{8.75\mu s} = 14.3V$$

Knowing that output current is provided to the load only during TOFF, calculate the peak current in L2 to be

$$I_{L2}(pk) = 2 \bullet I_{OUT} \bullet \frac{TON + TOFF}{TOFF}$$

in this case

$$I_{L2}(pk) = 2 \bullet 0.5A \bullet \frac{1.25\mu s + 8.75\mu s}{8.75\mu s} = 1.14A$$

Now calculate the value of L2

$$L_2 = V_{OUT}' \bullet \frac{TOFF}{I_{L2}(pk)}$$

in this case

$$L_2 = 2V \bullet \frac{8.75\mu s}{1.14A} = 15\mu H$$

For all of the calculations so far only the maximum load/minimum line condition have been considered. The entire range of operation must be considered to choose values for the rest of the components.

Under all normal operating conditions the current I_{TON}, (which is the current in R_{ON}), should be greater than 2mA and less than 7.5mA. In this case set R_{ON} to give I_{TON} = 2.8mA at low line. The voltage at TON will be about 11V so

$$R_{ON} = \frac{100V - 11V}{2.8mA} = 33k\Omega$$

With R_{ON} = 33k, I_{TON} at high line will be

$$I_{TON} = \frac{180V - 11V}{33k} = 5.1mA$$

At high line, the power dissipation in R_{ON} will be

$$P(R_{ON}) = (180V - 11V) \bullet 5.1mA = 860mW$$

R_{ON} will need to be at least a 1W resistor. Alternately it could be four 1/4W 8.2kΩ resistors in series.

Once R_{ON} is set, C_T can be chosen. The charge current for C_T is nominally 15% of I_{TON}, and the nominal oscillator amplitude is 3.4V, so

$$TON = \frac{CT \bullet 3.4V}{0.15 \bullet I_{TON}}$$

solving for CT

$$CT = \frac{TON \bullet 0.15 \bullet I_{TON}}{3.4V}$$

I_{TON} at low line is 2.8mA, and the target TON at low line is 1.25µs, so in this case

$$CT = \frac{1.25\mu s \bullet 0.15 \bullet 2.8mA}{3.4V} = 150pF$$

The final component to be chosen is R_{OFF}, which determines the minimum value of TOFF. When the output voltage is below the regulation point, the discharge current for CT is equal to I_{TOFF} (the current in R_{OFF}). Under that condition

$$TOFF = \frac{CT \bullet 3.4V}{I_{TOFF}}$$

since the voltage at the TOFF pin = 0.4V

$$I_{TOFF} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

substituting and solving for R_{OFF}

$$R_{OFF} = \frac{T_{OFF} \bullet (V_{OUT} - 0.4V)}{CT \bullet 3.4V}$$

The largest discharge current, and hence the minimum off time, will occur when the output is about 10mV be-

APPLICATION INFORMATION (cont.)

low the regulation point of 1.25V. The minimum value for TOFF is 8.75µs. So in this case

$$R_{OFF} = \frac{8.75\mu s \bullet (1.24V - 0.4V)}{150pF \bullet 3.4V} = 15k$$

OTHER APPLICATION CONSIDERATIONS

Output Capacitor: For best regulation of the output voltage or current, the output capacitor should be a low ESR type. This is especially true when operating in current sense mode with a non-linear load such as a battery. If a low ESR capacitor cannot be used, excellent regulation can also be achieved by placing a low pass R/C filter between the current shunt and the CS input.

No Load Operation: The UCC3890 is inherently protected for short circuits, but not for open circuits. If the load is removed, the output voltage will quickly rise up to the regulation point. Once the output is above the regulation voltage, the oscillator will drop to the minimum frequency set by RS/CT. With no load on the output, even at this low frequency the output voltage can quickly rise to a dangerous level. To protect against this, it is recommended that a zener or other voltage clamp always be connected across the output. The clamp should be chosen to be above the normal range of output voltage, but low enough to protect the output capacitor. In current sense operation, removal of the load will also break the regulation loop, in which case a simple clamp on the output may not be adequate. In current sense mode it is recommended that a second zener be connected from the output to the FB pin, the breakdown voltage of this clamp chosen to be high enough so that it will not conduct during normal operation, but will conduct at least 2V lower than the breakdown voltage of the other clamp.

Gate Drive for the External FET: The UCC3890 is guaranteed to be able to deliver at least 1mA of steady state current to the gate of the external FET at ITON = 2mA. If ITON is higher than 2mA, 80% of the additional current is available to drive the FET gate. If, as in the design example above, a moderate sized FET such as the IRF820 is used, the operating frequency is 100kHz, and the minimum ITON at low line is 2.8mA, then the available gate drive current may be adequate. The IRF820 needs about 13nC to charge the gate on each cycle. At 100kHz, this is equivalent to 1.3mA steady state; below the minimum 1.64mA available. In some combinations of a larger FET, and/or higher frequency operation, the current available for driving the gate may not be adequate. In that case extra current may be provided by connecting a resistor RDD from the line input to the VDD pin. This resistor should be sized so that under all conditions the current input to VDD is below the 7.5mA absolute maximum limit. RDD will likely need to be a power resistor.

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