TEXAS INSTRUMENTS

CD4555B, CD4556B Types

CMOS
Dual Binary to 1 of 4
Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)
CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

■ CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

■ Expandable with multiple packages
■ Standard, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range):   1 V at V_{DD} = 5 V
   2 V at V_{DD} = 10 V
   2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Decoding   ■ Code conversion
■ Demultiplexing (using Enable input as a data input)
■ Memory chip-enable selection
■ Function selection

CD4555B
FUNCTIONAL DIAGRAM

CD4556B
FUNCTIONAL DIAGRAM

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs
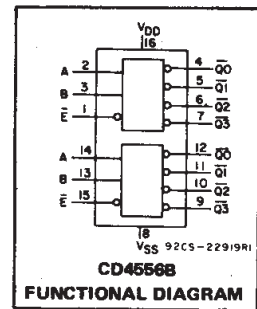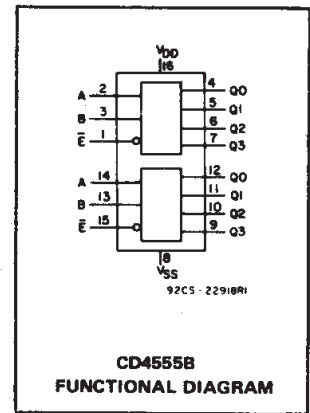
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

TERMINAL ASSIGNMENTS

CD4556B

CD4555B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
   Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
   For T_A = –55°C to +100°C 500mW
   For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
   FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types).......... 100mW
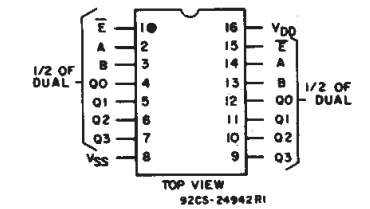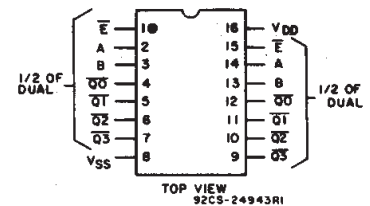OPERATING-TEMPERATURE RANGE (T_A) ....–55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ....–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	µA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, $C_L = 50 pF$, $R_L = 200 K\Omega$

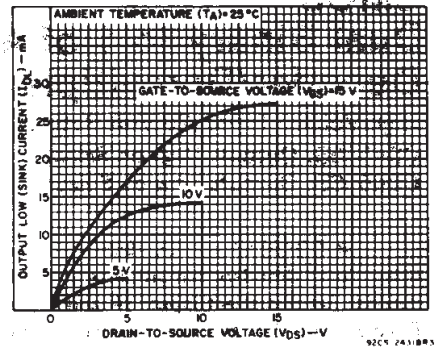| CHARACTERISTIC	TEST CONDITIONS V_{DD} Volts	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} A or B Input to Any Output	5	220	440	ns
	10	95	190	
	15	70	140	
$\overline{E}$ Input to Any Output	5	200	400	ns
	10	85	170	
	15	65	130	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN}	Any Input	5	7.5	pF

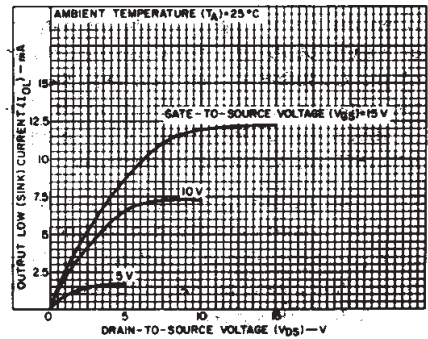Fig. 1 — Typical output low (sink) current characteristics.

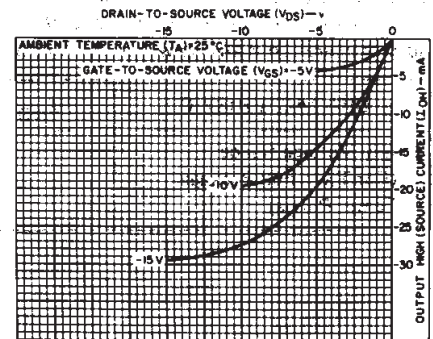Fig. 2 — Minimum output low (sink) current characteristics.

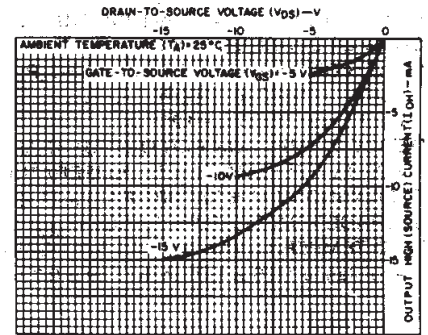Fig. 3 — Typical output high (source) current characteristics.

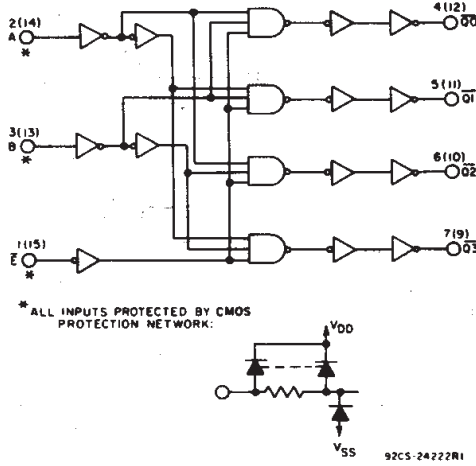Fig. 4 — Minimum output high (source) current characteristics.

*ALL INPUTS PROTECTED BY CMOS
PROTECTION NETWORK:

Fig. 5 — CD4556B logic diagram
(1 of 2 identical circuits).

*ALL INPUTS PROTECTED BY CMOS
PROTECTION NETWORK:
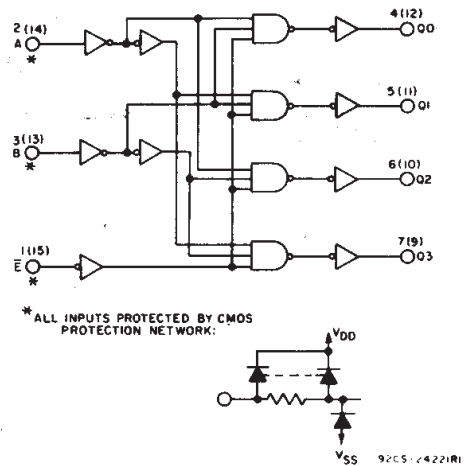
Fig. 6 — CD4555B logic diagram
(1 of 2 identical circuits).

TRUTH TABLE

INPUTS			OUTPUTS CD4555B				OUTPUTS CD4556B			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW
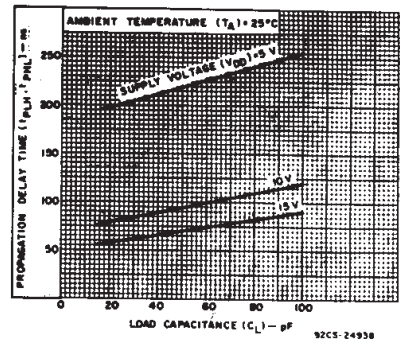
Fig. 7 — Typical propagation delay time vs. load
capacitance (A or B input to any output).
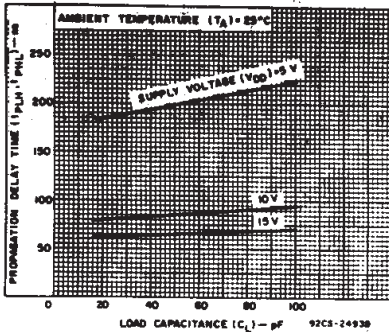
Fig. 8 — Typical propagation delay time vs. load
capacitance (E input to any output).
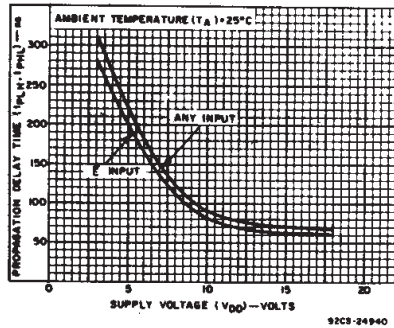
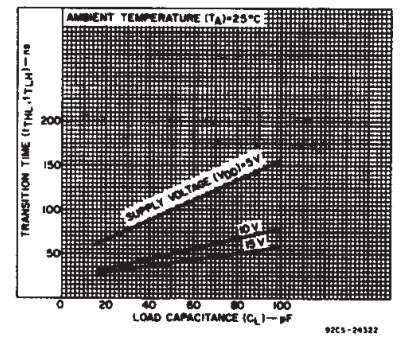Fig. 9 — Typical propagation delay time vs.
supply voltage.

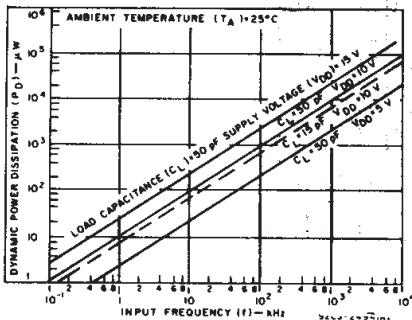Fig. 10 — Typical transition time vs. load
capacitance.

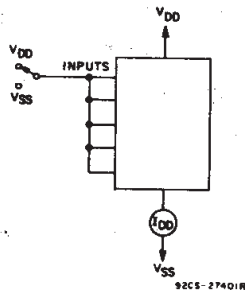Fig. 11 — Typical dynamic power dissipation
vs. frequency.

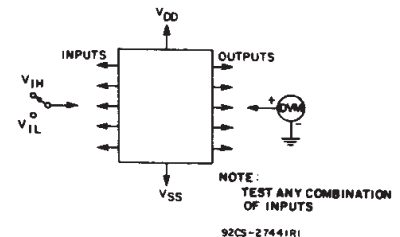Fig. 12 — Quiescent device current test
circuit.

NOTE:
TEST ANY COMBINATION
OF INPUTS

Fig. 13 — Input voltage test circuit.

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs
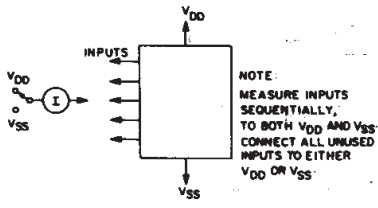
Fig. 14 — Input current test circuit.

NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.
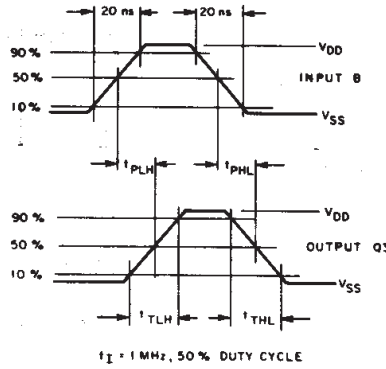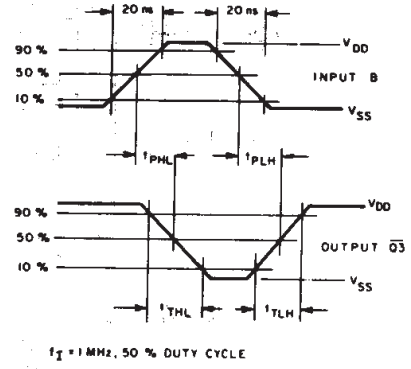

Fig. 15 — CD4555B B input to Q3 output dynamic signal waveforms.

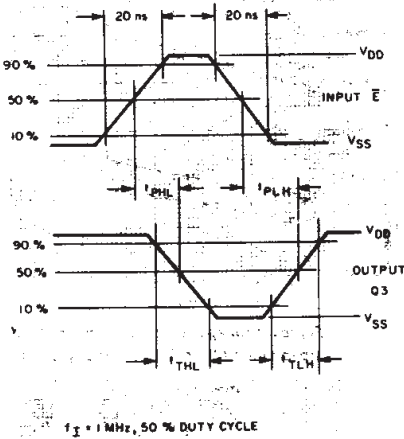Fig. 16 — CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

Fig. 17 — CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.
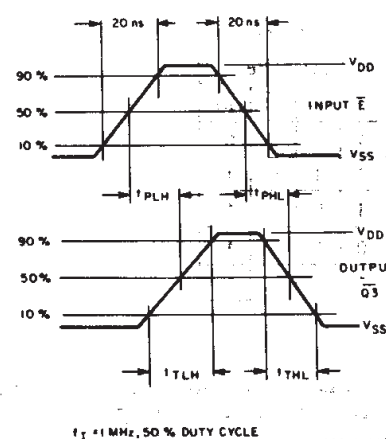
Fig. 18 — CD4556B $\overline{E}$ input to $\overline{Q3}$ output dynamic signal waveforms.

APPLICATIONS
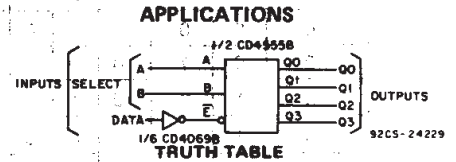
TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Fig. 19 — 1-of-4 line data demultiplexer using CD4555B.
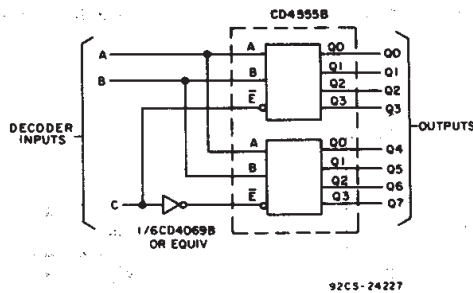
Fig. 20 — 1-of-8 decoder using CD4555B.

TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 21 — 1-of-16 decoder using CD4555B and CD4556B.
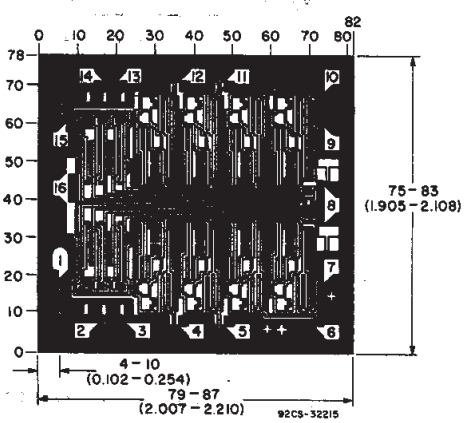
DIMENSIONS AND PAD LAYOUT FOR
CD4555BH.
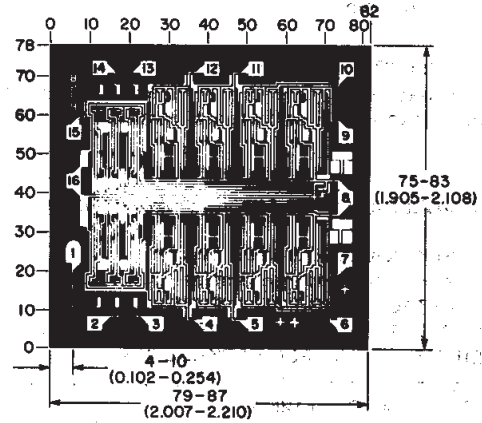
DIMENSIONS AND PAD LAYOUT FOR
CD4556BH.

*Dimensions in parentheses are in millimeters and are
derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10⁻³ inch).*

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated