# SN54AHC138, SN74AHC138
## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V $V_{CC}$
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

**SN54AHC138 . . . J OR W PACKAGE**
**SN74AHC138 . . . D, DB, DGV, N, OR PW PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| A | 1 | 16 | $V_{CC}$ |
| B | 2 | 15 | Y0 |
| C | 3 | 14 | Y1 |
| $\overline{G2A}$ | 4 | 13 | Y2 |
| $\overline{G2B}$ | 5 | 12 | Y3 |
| G1 | 6 | 11 | Y4 |
| Y7 | 7 | 10 | Y5 |
| GND | 8 | 9 | Y6 |

**SN54AHC138 . . . FK PACKAGE**
**(TOP VIEW)**

Top pins: B (3), A (2), NC (1), $V_{CC}$ (20), Y0 (19)

| | | | |
|---|---|---|---|
| C | 4 | 18 | Y1 |
| $\overline{G2A}$ | 5 | 17 | Y2 |
| NC | 6 | 16 | NC |
| $\overline{G2B}$ | 7 | 15 | Y3 |
| G1 | 8 | 14 | Y4 |

Bottom pins: Y7 (9), GND (10), NC (11), Y6 (12), Y5 (13)
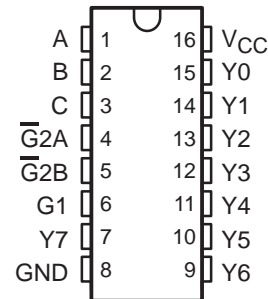
NC – No internal connection

## description

The 'AHC138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.
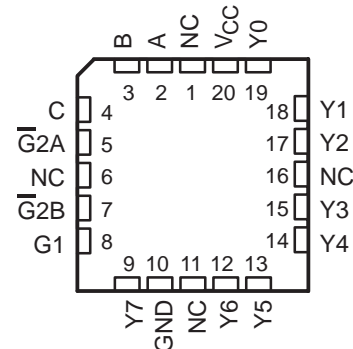
The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC138 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

**TEXAS INSTRUMENTS**

# SN54AHC138, SN74AHC138
## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

**FUNCTION TABLE**

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†
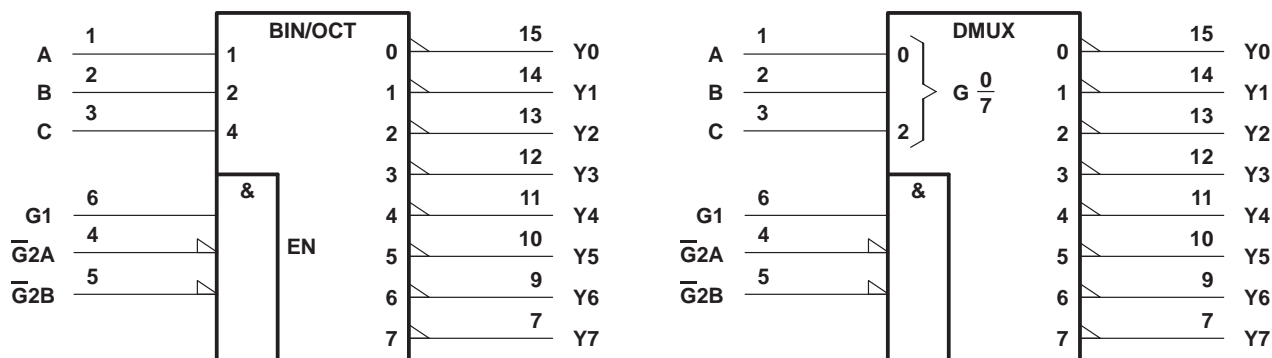


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)
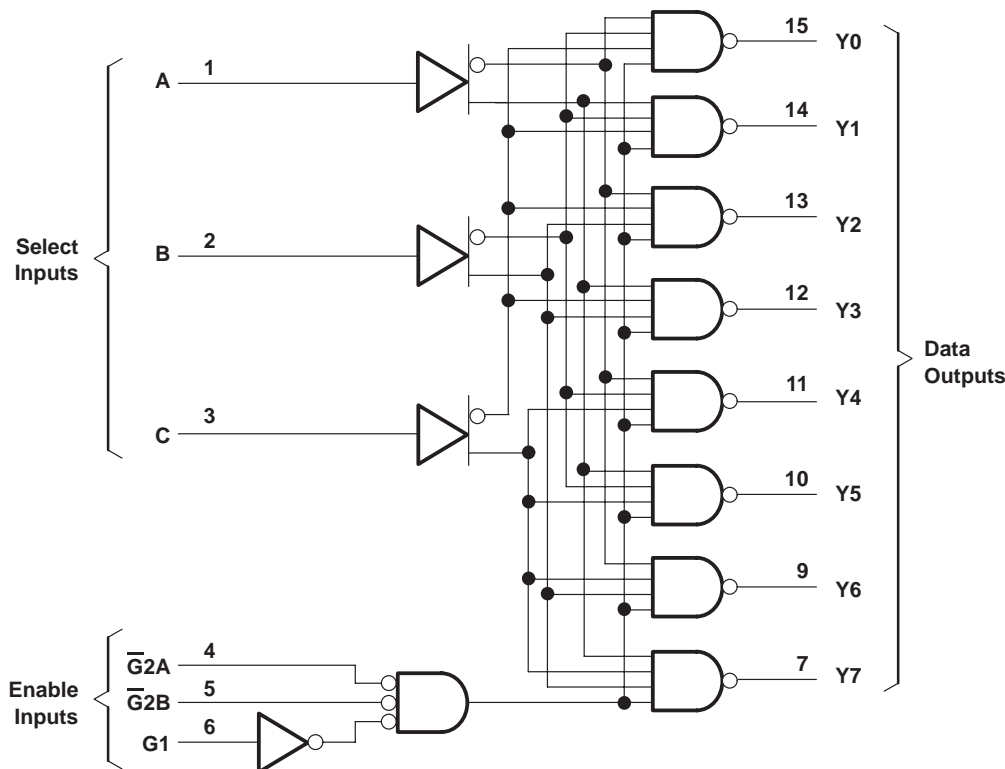
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ............................................................. −0.5 V to 7 V

Input voltage range, $V_I$ (see Note 1) ................................................... −0.5 V to 7 V

Output voltage range, $V_O$ (see Note 1) ....................................... −0.5 V to $V_{CC}$ + 0.5 V

Input clamp current, $I_{IK}$ ($V_I < 0$) ........................................................ −20 mA

Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) ................................................ ±20 mA

Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) ................................................ ±25 mA

Continuous current through $V_{CC}$ or GND ........................................................ ±75 mA

Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .................................... 73°C/W

DB package .................................. 82°C/W

DGV package .............................. 120°C/W

N package .................................. 67°C/W

PW package .............................. 108°C/W

Storage temperature range, $T_{stg}$ ............................................... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54AHC138 MIN | SN54AHC138 MAX | SN74AHC138 MIN | SN74AHC138 MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | | −50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | −4 | | −4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | −8 | | −8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C MIN | $T_A$ = 25°C TYP | $T_A$ = 25°C MAX | SN54AHC138 MIN | SN54AHC138 MAX | SN74AHC138 MIN | SN74AHC138 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = −50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = −4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = −8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.

![Texas Instruments logo]

**switching characteristics over recommended operating free-air temperature range,**
$V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC138 | | SN74AHC138 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 15 pF | | 8.2* | 11.4* | 1* | 13* | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.2* | 11.4* | 1* | 13* | 1 | 13 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 15 pF | | 8.1* | 12.8* | 1* | 15* | 1 | 15 | ns |
| $t_{PHL}$ | | | | | 8.1* | 12.8* | 1* | 15* | 1 | 15 | |
| $t_{PLH}$ | $\overline{G2A}$, $\overline{G2B}$ | Any Y | $C_L$ = 15 pF | | 8.2* | 11.4* | 1* | 13.5* | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 8.2* | 11.4* | 1* | 13.5* | 1 | 13.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 10 | 15.8 | 1 | 18 | 1 | 18 | ns |
| $t_{PHL}$ | | | | | 10 | 15.8 | 1 | 18 | 1 | 18 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 10.6 | 16.3 | 1 | 18.5 | 1 | 18.5 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.3 | 1 | 18.5 | 1 | 18.5 | |
| $t_{PLH}$ | $\overline{G2A}$, $\overline{G2B}$ | Any Y | $C_L$ = 50 pF | | 10.7 | 14.9 | 1 | 17 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 10.7 | 14.9 | 1 | 17 | 1 | 17 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,**
$V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC138 | | SN74AHC138 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 15 pF | | 5.7* | 8.1* | 1* | 9.5* | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.7* | 8.1* | 1* | 9.5* | 1 | 9.5 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 15 pF | | 5.6* | 8.1* | 1* | 9.5* | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.6* | 8.1* | 1* | 9.5* | 1 | 9.5 | |
| $t_{PLH}$ | $\overline{G2A}$, $\overline{G2B}$ | Any Y | $C_L$ = 15 pF | | 5.8* | 8.1* | 1* | 9.5* | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.8* | 8.1* | 1* | 9.5* | 1 | 9.5 | |
| $t_{PLH}$ | A, B, C | Any Y | $C_L$ = 50 pF | | 7.2 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.2 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PLH}$ | G1 | Any Y | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PLH}$ | $\overline{G2A}$, $\overline{G2B}$ | Any Y | $C_L$ = 50 pF | | 7.3 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 10.1 | 1 | 11.5 | 1 | 11.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

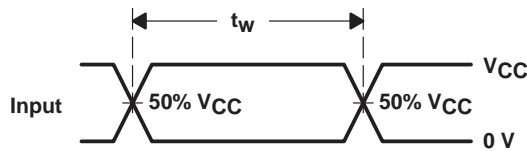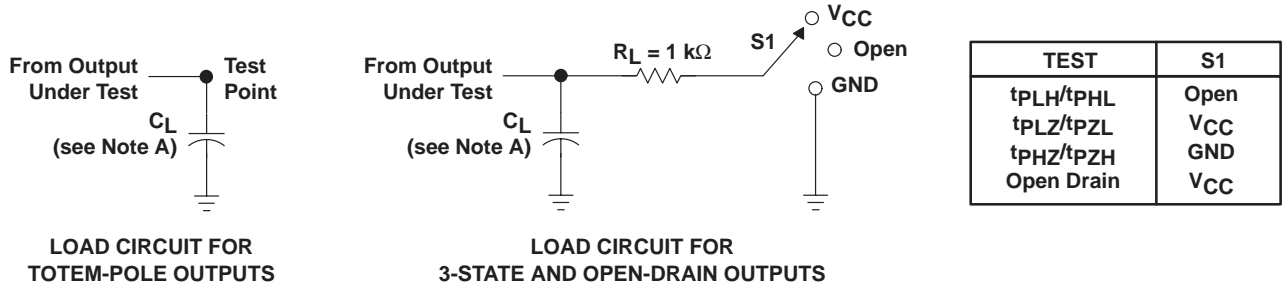**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$  Power dissipation capacitance | No load,  f = 1 MHz | 13 | pF |

TEXAS
INSTRUMENTS

## PARAMETER MEASUREMENT INFORMATION

From Output Under Test — Test Point — $C_L$ (see Note A)

**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

From Output Under Test — $C_L$ (see Note A) — $R_L = 1\ k\Omega$ — S1 — $V_{CC}$ / Open / GND

**LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

Input — $t_w$ — 50% $V_{CC}$ — $V_{CC}$ — 0 V

**VOLTAGE WAVEFORMS
PULSE DURATION**

Timing Input — 50% $V_{CC}$ — $V_{CC}$ — 0 V
$t_{su}$ — $t_h$
Data Input — 50% $V_{CC}$ — 50% $V_{CC}$ — $V_{CC}$ — 0 V
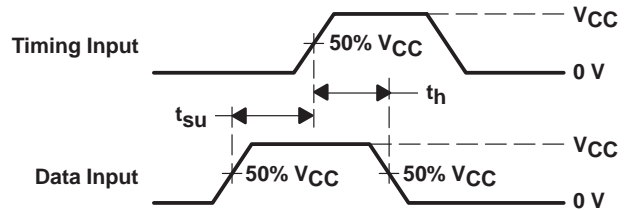
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Input — 50% $V_{CC}$ — 50% $V_{CC}$ — $V_{CC}$ — 0 V
$t_{PLH}$ — $t_{PHL}$
In-Phase Output — 50% $V_{CC}$ — 50% $V_{CC}$ — $V_{OH}$ — $V_{OL}$
$t_{PHL}$ — $t_{PLH}$
Out-of-Phase Output — 50% $V_{CC}$ — 50% $V_{CC}$ — $V_{OH}$ — $V_{OL}$
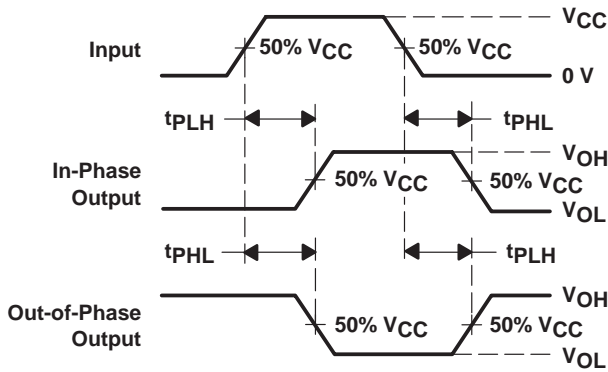
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

Output Control — 50% $V_{CC}$ — 50% $V_{CC}$ — $V_{CC}$ — 0 V
$t_{PZL}$ — $t_{PLZ}$
Output Waveform 1 S1 at $V_{CC}$ (see Note B) — 50% $V_{CC}$ — $\approx V_{CC}$ — $V_{OL} + 0.3\ V$ — $V_{OL}$
$t_{PZH}$ — $t_{PHZ}$
Output Waveform 2 S1 at GND (see Note B) — 50% $V_{CC}$ — $V_{OH}$ — $V_{OH} - 0.3\ V$ — $\approx 0\ V$
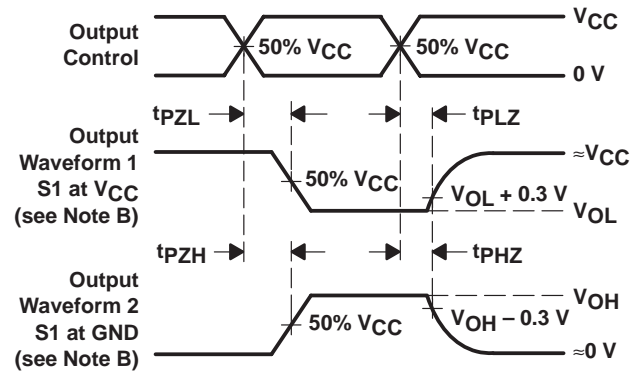
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_O$ = 50 $\Omega$, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## APPLICATION INFORMATION
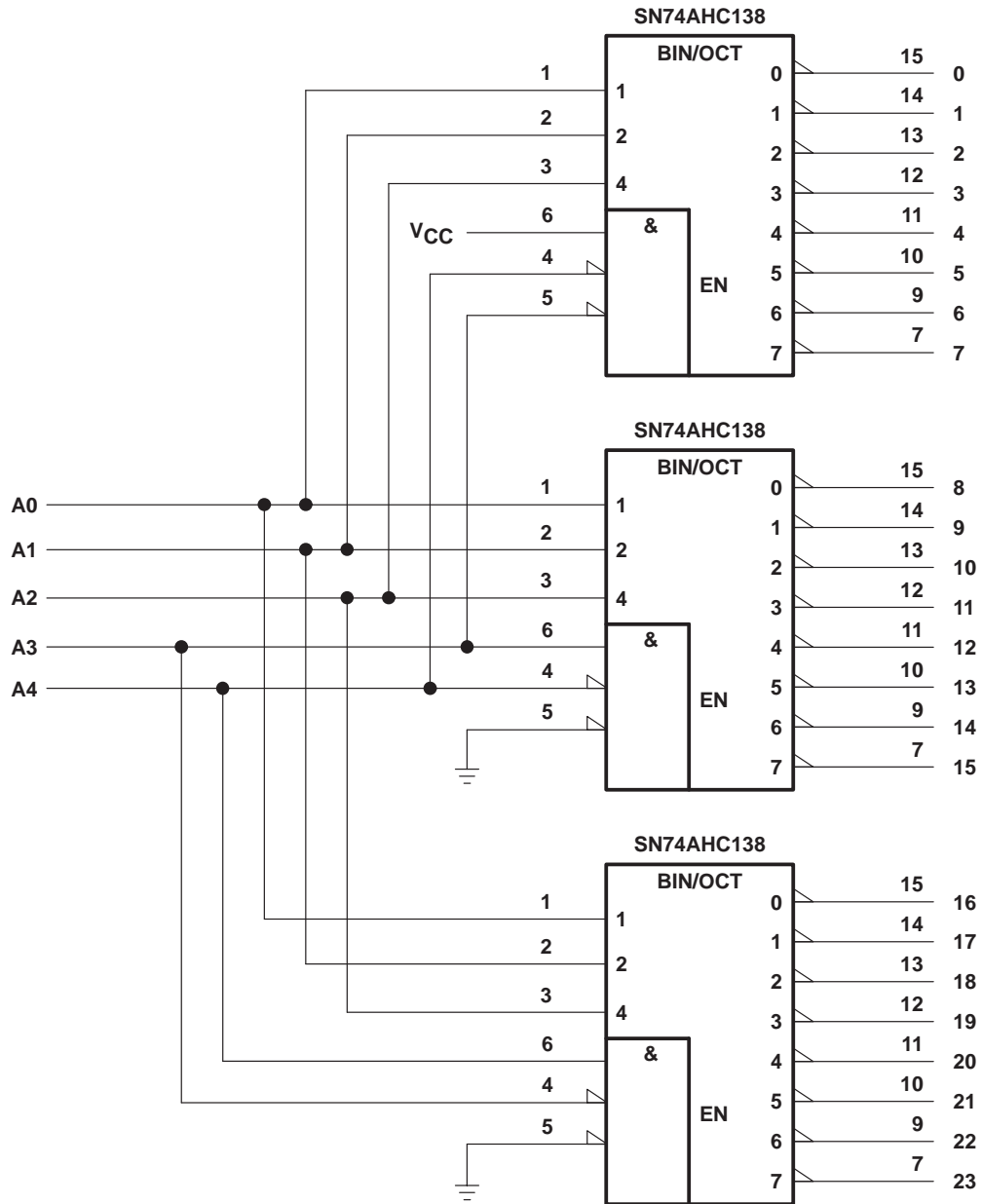


**Figure 2. 24-Bit Decoding Scheme**
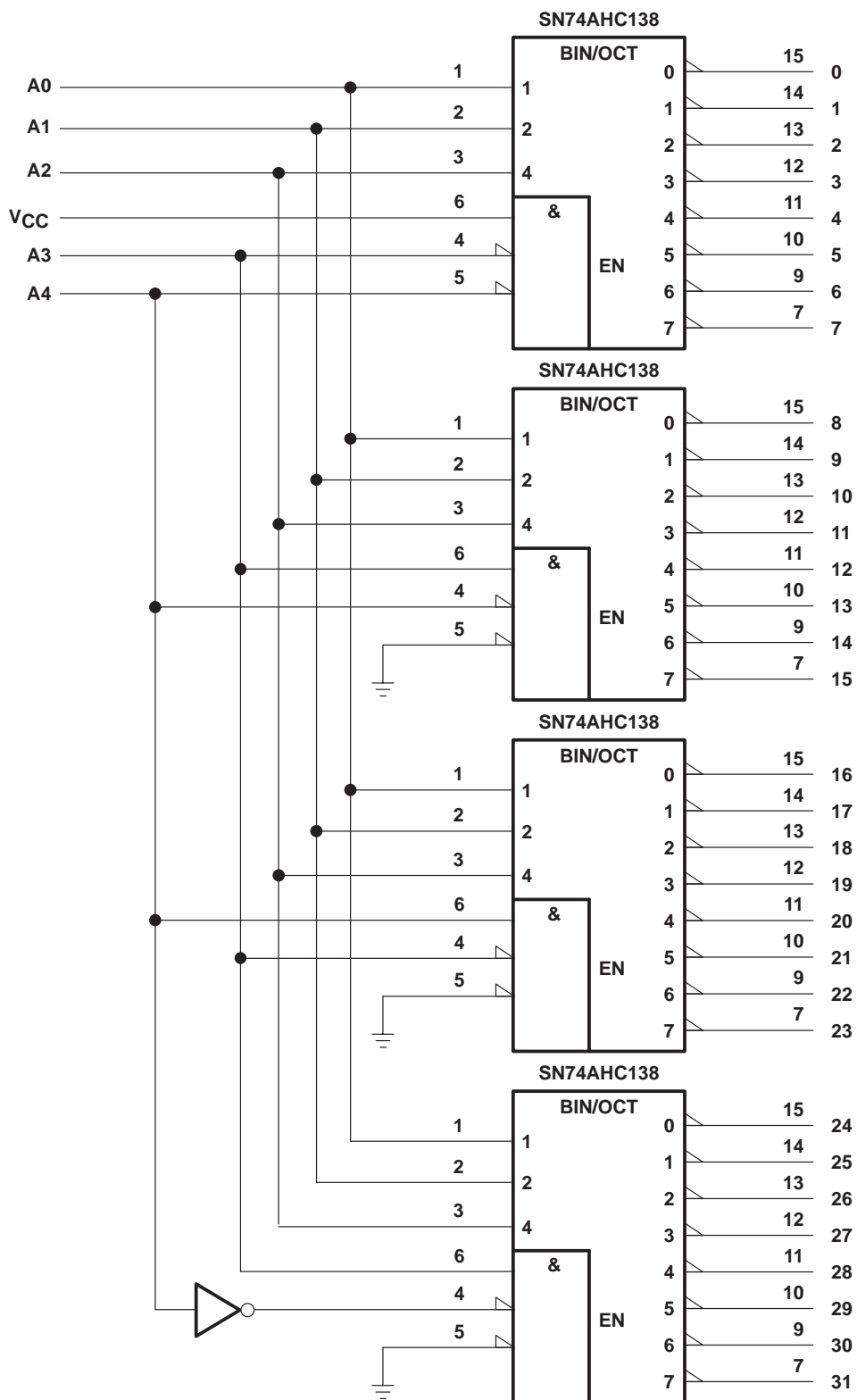
## APPLICATION INFORMATION



**Figure 3. 32-Bit Decoding Scheme**

**IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated