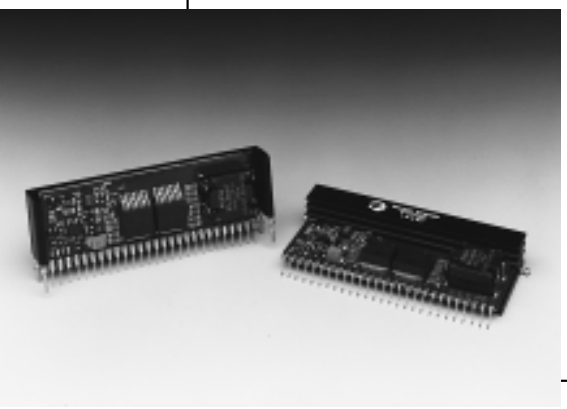
PT7705 Series

18 AMP "BIG-HAMMER" PROGRAMMABLE INTEGRATED SWITCHING REGULATOR

Revised 5/15/98



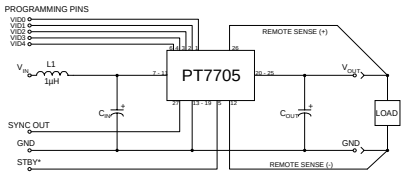
The PT7705 is a new series of high-performance, 18 Amp Integrated Switching Regulators (ISRs) housed in a 27-pin SIP package. The 18A capability allows easy integration of the latest high-speed, low-voltage µPs and bus drivers into existing 5V systems.

The PT7705 series has been designed to work in parallel with one or more of the PT7749 - 18A current boosters for increased I_{out} in increments of 18A.

The output voltage of the PT7705 can be easily programmed from 1.3V to 3.5V with a 5 bit input compatible with Intel's Pentium® II Processor. A differential remote sense is also provided which automatically compensates for any voltage drop from the ISR to the load.

1200µF of output capacitance are required for proper operation.

Standard Application



C_{in} = Required 1200µF electrolytic
C_{out} = Required 1200µF electrolytic
L1 = Optional 1µH input choke

Pin-Out Information

Pin	Function	Pin	Function	Pin	Function
1	VID0	10	V_{in}	19	GND
2	VID1	11	V_{in}	20	V_{out}
3	VID2	12	Remote Sense Gnd	21	V_{out}
4	VID3	13	GND	22	V_{out}
5	STBY* - Stand-by	14	GND	23	V_{out}
6	VID4	15	GND	24	V_{out}
7	V_{in}	16	GND	25	V_{out}
8	V_{in}	17	GND	26	Remote Sense V_{out}
9	V_{in}	18	GND	27	Sync Out

For STBY* pin; open = output enabled; ground = output disabled.

Specifications

Characteristics (T_a = 25°C unless noted)	Symbols	Conditions		PT7705 SERIES Min	Typ	Max	Units
Output Current	I_o	T_a = +60°C, 200 LFM, pkg N T_a = +25°C, natural convection		0.1* 0.1*	— —	18** 15**	A A
Input Voltage Range	V_{in}	0.1A ≤ I_o ≤ 15A		4.5***	—	5.5	V
Output Voltage Tolerance	ΔV_o	V_{in} = +5V, I_o = 15A 0°C ≤ T_a ≤ +65°C		V_o-0.03	—	V_o+0.03	V
Line Regulation	Reg_{line}	4.5V ≤ V_{in} ≤ 5.5V, I_o = 15A		—	±10	—	mV
Load Regulation	Reg_{load}	V_{in} = +5V, 0.1 ≤ I_o ≤ 15A		—	±10	—	mV
V_o Ripple/Noise	V_n	V_{in} = +5V, I_o = 15A		—	50	—	mV
Transient Response with C_{out} = 1200µF	t_{tr} V_{os}	I_o step between 7.5A and 15A V_o over/undershoot		— —	100 200	— —	µSec mV
Efficiency	η	V_{in} = +5V, I_o = 10A	V_o = 3.3V V_o = 2.9V V_o = 2.5V V_o = 1.8V V_o = 1.5V	— — — — —	89 87 85 79 77	— — — — —	% % % % %
Switching Frequency	f_o	4.5V ≤ V_{in} ≤ 5.5V 0.1A ≤ I_o ≤ 15A		650	700	750	kHz
Absolute Maximum Operating Temperature Range	T_a	—		0	—	+85	°C
Recommended Operating Temperature Range	T_a	Forced Air Flow = 200 LFM Over V_{in} and I_o Ranges		0	—	+65****	°C
Storage Temperature	T_s	—		-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, Half Sine, mounted to a fixture		—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2, 20-2000 Hz, Soldered in a PC board		—	10	—	G's
Weight	—	Vertical/Horizontal		—	31/41	—	grams

* ISR-will operate down to no load with reduced specifications. Please note that this product is not short-circuit protected.
**The PT7705 series can be easily paralleled with one or more of the PT7749 Current Boosters to provide increased output current in increments of 18A.
*** The minimum input voltage is 4.5V or V_{out}+1.2V, whichever is greater. ****See SOA curves.

Output Capacitors: *The PT7705 series requires a minimum ouput capacitance of 1200µF for proper operation. Do not use Oscon type capacitors. The maximum allowable output capacitance is 15,000µF. See Capacitor Application Note.*

Input Filter: *An input filter is optional for most applications. The input inductor must be sized to handle 15ADC with a typical value of 1µH. The input capacitance must be rated for a minimum of 1.3Arms of ripple current. For transient or dynamic load applications, additional capacitance may be required.*

Power Trends, Inc. 27715 Diehl Road, Warrenville, IL 60555 **(800) 531-5782** Fax: (630) 393-6902 **http://www.powertrends.com**

Features

- Single-Device: +5V input
- 5-bit Programmable: 1.3V to 3.5V@18A
- High Efficiency
- Input Voltage Range: 4.5V to 5.5V
- Differential Remote Sense
- 27-pin SIP Package
- Parallelable with PT7749 18A "Current Boosters"

Programming Information

VID3	VID2	VID1	VID0	VID4=1 Vout	VID4=0 Vout
1	1	1	1	2.0V	1.30V
1	1	1	0	2.1V	1.35V
1	1	0	1	2.2V	1.40V
1	1	0	0	2.3V	1.45V
1	0	1	1	2.4V	1.50V
1	0	1	0	2.5V	1.55V
1	0	0	1	2.6V	1.60V
1	0	0	0	2.7V	1.65V
0	1	1	1	2.8V	1.70V
0	1	1	0	2.9V	1.75V
0	1	0	1	3.0V	1.80V
0	1	0	0	3.1V	1.85V
0	0	1	1	3.2V	1.90V
0	0	1	0	3.3V	1.95V
0	0	0	1	3.4V	2.00V
0	0	0	0	3.5V	2.05V

Logic 0 = Pin 12 potential (remote sense gnd)
Logic 1 = Open circuit (no pull-up resistors)
VID3 and VID4 may not be changed while the unit is operating.

Ordering Information

PT7705❑ = 1.3 to 3.5 Volts

(For dimensions and PC board layout, see Package Styles 800 and 810.)

PT Series Suffix (PT1234X)

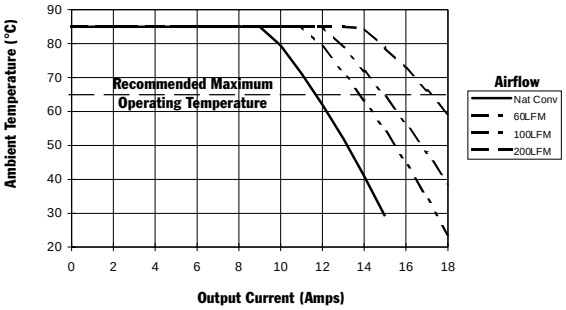
Case/Pin Configuration	
Vertical Through-Hole	**N**
Horizontal Through-Hole	**A**
Horizontal Surface Mount	**C**

CHARACTERISTIC DATA

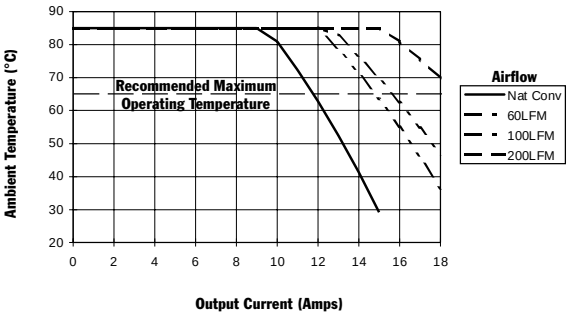
PT7705, V_o = 3.3 VDC (See Note 1)

Safe Operating Area Curves (@V_{in}=+5V)

PKG SUFFIX N

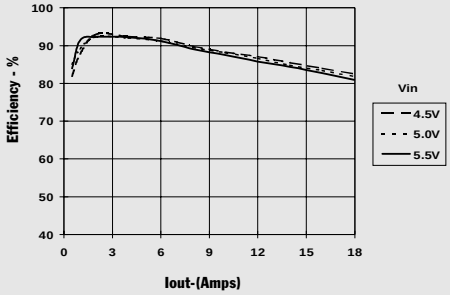


PKG SUFFIX A, C

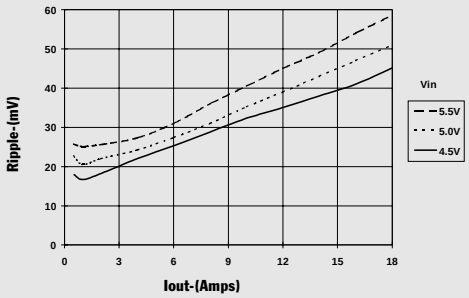


PT7705, V_o = 3.3 VDC (See Note 1)

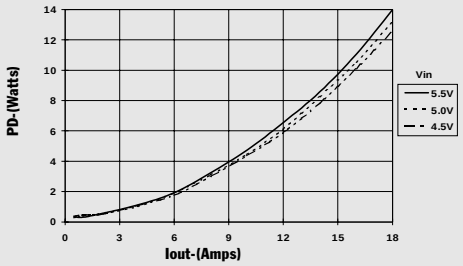
Efficiency vs Output Current



Ripple vs Output Current



Power Dissipation vs Output Current



Note 1: *All data listed in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note 2: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Pin-Coded Output Voltage Adjustment on the "Big Hammer" Series ISRs

The ISRs related to Power Trends' PT7705 incorporate pin-coded voltage control to adjust the ouput voltage. The control pins are identified VID0 - VID4 (pins 1, 2, 3, 4, & 6) respectively. When the control pins are left open-circuit, the ISR output will regulate at its factory trimmed output voltage. Each pin is internally connected to a precision resistor, which when grounded changes the output voltage by a set amount. By selectively grounding VID0 -VID4, the output voltage these ISRs can be programmed in incremental steps over the specified output voltage range. In each case, the program code and output voltage range offered by these ISRs are compatible with the voltage ID specification defined by Intel Corporation for voltage regulator modules (VRMs) used to power Pentium® microprocessors. Refer to Figure 1 below for the connection schematic, and the respective device Data Sheet for the appropriate programming code information.

Notes:

1. The programming convention is as follows:-

   Logic 0: Connect to pin12 (Remote Sense Ground).
   Logic 1: Open circuit/open drain (See notes 2, & 4)

2. Do not connect pull-up resistors to the voltage programming pins.

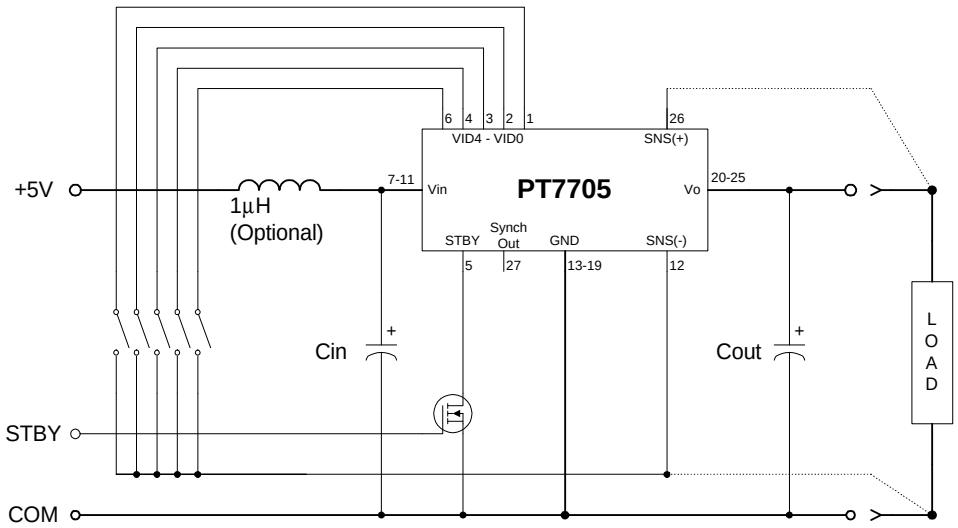
3. To minimize output voltage error, always use pin 12 (Remote Sense Ground) as the logic "0" reference. While the regular ground (pins 13-19) can also be used for programming, doing so will degrade the load reglation of the product.

4. If active devices are used to ground the voltage control pins, low-level open drain MOSFET devices should be used over bipolar transistors. The inherent V_{ce}(sat) in bipolar devices introduces errors in the device's internal divider network. Discrete transistors such as the BSS138, 2N7002, IRLML2402, or the 74C906 hex open-drain buffer are examples of appropriate devices.

Active Voltage Programming:

Special precautions should be taken when making changes to the voltage control progam code while the unit is powered. It is highly recommended that the ISR be either powered down or held in standby. Changes made to the program code while V_{out} is enabled induces high current transients through the device. This is the result of the electrolytic output capacitors being either charged or discharged to the new output voltage set-point. The transient current can be minimized by making only incremental changes to the binary code, i.e. one LSB at a time. A minimum of 100µs settling time between each program state is also recommended. Making non-incremental changes to VID3 and VID4 with the output enabled is discouraged. If they are changed, the transients induced can overstress the device resulting in a permanent drop in efficiency. If the use of active devices prevents the program code being asserted prior to power-up, pull pin 5 (STBY) to the device GND during the period that the input voltage is applied to V_{in}. Releasing pin 5 will then allow the device output to execute a soft-start power-up to the programmed voltage.

Figure 1



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