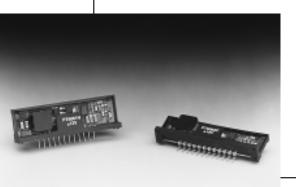
PT5060

Series

+5V to $\pm 12V/15V$ 9W DUAL OUTPUT **INTEGRATED SWITCHING REGULATOR**

> **PT5061**□ = ±12 Volts **PT5062**□ = ±15 Volts

Revised 5/15/98



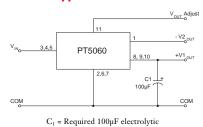
- **Dual Outputs:**
 - +12V @ 0.5A
 - -12V @ 0.25A
 - Wide Input Voltage Range:
- 85% Efficiency
- Adjustable Output Voltage
- Laser-trimmed Output Voltage

The Power Trends' PT5060 Series is a dual output Integrated Switching

Regulator (ISR) designed for use in +5 volt systems that require low power ±12 or ±15 volt rails. They can be used to power such application circuits as D/A and A/D converters, Op Amps, and interface logic. Both output voltages can be easily adjusted with one external resistor. These ISRs are offered in a low profile 12-pin SIP package in either vertical or horizontal through-hole or SMD-configurations.

Please note that this product does not include short-circuit protection.

Standard Application

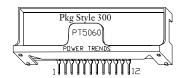


Pin-Out Information Ordering Information

Pin	Function
1	$-V2_{\mathrm{out}}$
2	GND
3	V_{in}
4	V_{in}
5	Vin
6	GND
7	GND
8	$+V1_{out}$
9	$+V1_{out}$
10	$+V1_{out}$
11	V _{out} Adjust
12	Do Not Connect

PT Series Suffix (PT1234X)

Case/Pin Configuration	
Vertical Through-Hole	N
Horizontal Through-Hole	Α
Horizontal Surface Mount	C



Specifications

Characteristics				PT5060	ERIES		
(T _a = 25°C unless noted)	Symbols	Conditions		Min	Тур	Max	Units
Output Current	I_{o}	Over V _{in} range	V _o =+12V V _o =-12V	0.05 0.05*	=	0.50 0.25	A A
			$V_o=+15V$ $V_o=-15V$	0.05 0.05*	=	0.40 0.20	A A
Current Limit**	I_{cl}	$V_{\rm in}$ = +5 V		_	1.5 I _o ma	x** —	A
Inrush Current	$I_{ m ir}$ $t_{ m r}$	V_{in} = +5V @ max I_o On start up		_	5.5 2	_	A mSec
Input Voltage Range	$ m V_{in}$	$I_o = 0.1 \text{ to } I_o \text{max}$		4.75		V_{o} -1 V	V
Output Voltage Tolerance	$\Delta V_{\rm o}$	Over V_{in} and I_o ranges T_A = 0°C to +70°C	$^{+}\mathrm{V_{o}}$ $^{-}\mathrm{V_{o}}$	_	±1.5 ±5	±3.0 ±10	$^{ m \%V_o}_{ m V_o}$
Line Regulation	Reg _{line}	Over V _{in} range, I _o =0.5A,	$V_o = +12V$	_	±0.5	±1.0	$%V_{o}$
Load Regulation	Reg _{load}	$0.1 < I_o < I_o max, V_{in} = +5V$	$V, V_{o} = +12V$	_	±0.5	±1.0	$%V_{o}$
V _o Ripple/Noise	V_n	V_{in} = +5 V , I_o = I_o max	$^{+}\mathrm{V_{o}}$ $^{-}\mathrm{V_{o}}$	_	±1.5 ±2.0	±3 ±3	$\mathrm{^{\%}V_{o}}$ $\mathrm{^{\%}V_{o}}$
Transient Response	$egin{array}{c} egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}$	25% load change V _o over/undershoot		_	100 3.0	5.0	μSec %V _o
Efficiency	η	V_{in} = +5V, I_o =0.25A each of	output	_	85	_	%
Switching Frequency	f_{o}	Over V _{in} and I _o ranges		_	650	_	kHz
Absolute Maximum Operating Temperature Range	T_a	_		0	-	+85	°C
Recommended Operating Temperature Range	T_a	Free Air Convection (40- Over V _{in} and I _o ranges	60LFM)	0	_	+65***	°C
Storage Temperature	T_s			-40		+125	°C
Mechanical Shock		Per Mil-STD-883D, Met 1 msec, Half Sine, mount	hod 2002.3, ed to a fixture	_	500	_	G's
Mechanical Vibration		Per Mil-STD-883D, Met 20-2000 Hz, Soldered in		_	15	_	G's
Weight				_	6.5	_	grams

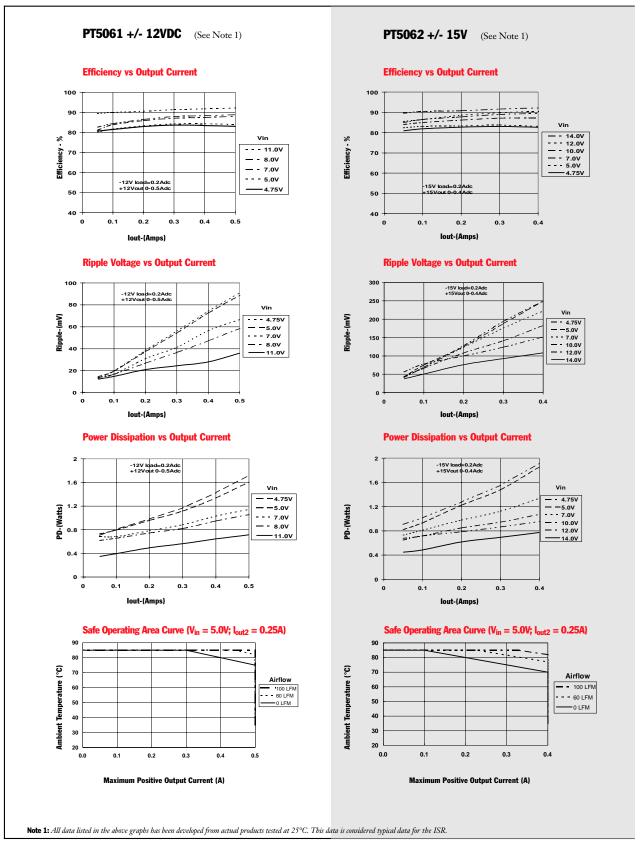
^{*} Do not operate below minimum load. ** Boost topology ISRs are not short circuit protected. *** See SOA Curves.

DATA SHEETS

PT5060

Series

CHARACTERISTIC DATA



More Application Notes

Adjusting the Output Voltage of the PT5060 Dual Output Boost Converter Series

The dual output voltage of the Power Trends PT5060 Series ISRs can be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 accordingly gives the applicable adjustment range for each model in the series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R2, between pin 11 (Vo adjust) and pins 2, 6, or 7 (GND).

Adjust Down: Add a resistor (R1), between pin 11 (V_o adjust) and pins 8, 9 or 10 (V1_{out}).

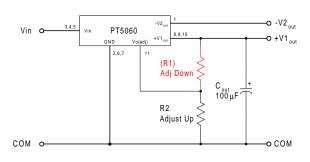
Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R1) or R2 as appropriate.

- 1. Both the positive and negative voltage outputs from the ISR are adjusted simultaneously.
- 2. Use only a single 1% resistor in either the (R1) or R2 location. Place the resistor as close to the ISR as possible.
- Never connect capacitors from V₀ adjust to either GND or V_o . Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
- 4. An increase in the output voltage must be accompanied by a corresponding reduction in the specified maximum current at each output. For V1_{out} and –V2_{out}, the revised maximum output current must be reduced to the equivalent of 6Watts and 3Watts respectively. i.e.

where V_a is the adjusted output voltage.

5. Adjustments to the output voltage will also limit the maximum input voltage that can be applied to the ISR. The maximum input voltage that may be applied is limited to (Vout - 1)Vdc or 14Vdc, whichever is less.

Figure 1



The values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulae.

(R1) =
$$\frac{3.65 (V_a - 2.5)}{(V_o - V_a)} - 0.1$$
 kΩ

R2 =
$$\frac{9.125}{V_2 - V_0}$$
 - 0.1 k Ω

Where: Vo = Original output voltage V_a = Adjusted output voltage

Table 1

PT5060 ADJUSTMENT AND FORMULA PARAMETER				
Series Pt #	PT5061	PT5062		
Vo (nom)	±12.0V	±15.0V		
V _a (min)	± 7.5V	± 7.5V		
Va (max)	±14.0V	±20.0V		

Table 2

Series Pt #	PT5061	PT5062
Current	0.5/0.25Adc	0.4/0.2Adc
V _o (nom)	±12.0Vdc	±15.0Vdc
V _a (req'd)		
7.0		
7.5	(4.0)k Ω	(2.3)k Ω
8.0	(4.9) k Ω	(2.8) k Ω
8.5	(6.2) k $\mathbf{\Omega}$	(3.3) k Ω
9.0	(7.8) k Ω	(3.9)k Ω
9.5	(10.1) k Ω	(4.6) k Ω
10.0	(13.6) k Ω	(5.4) k Ω
10.5	(19.4)k Ω	(6.4) k Ω
11.0	(30.9)k Ω	(7.7) k $\mathbf{\Omega}$
11.5	(65.6) k Ω	(9.3) k Ω
12.0		(11.5)k Ω
12.5	18.2k Ω	(14.5) k $\mathbf{\Omega}$
13.0	9.0k Ω	(19.1)k Ω
13.5	6.0 k $\mathbf{\Omega}$	(26.7) k $\mathbf{\Omega}$
14.0	4.5k Ω	(41.9)k Ω
14.5		(87.5)k Ω
15.0		
15.5		18.2k Ω
16.0		9.0k Ω
16.5		6.0 k Ω
17.0		$4.5k\Omega$
17.5		3.6k Ω
18.0		2.9k Ω
18.5		2.5k Ω
19.0		2.2 k Ω
19.5		1.9k Ω
20.0		$1.7\mathrm{k}\mathbf{\Omega}$
R1 = (Red)	R2 = Black	

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