CD40257B Types

CMOS Quad 2-Line-to-1-Line Data Selector/Multiplexer

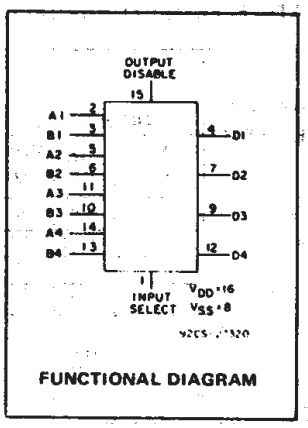
High-Voltage Types (20-Volt Rating)

■ CD40257B is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems.

The CD40257B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 3-state outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Digital Multiplexing
- Shift-right/shift-left registers
- True/complement selection

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITION
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

TRUTH TABLE

INPUTS				OUTPUT
3-STATE OUTPUT DISABLE	SELECT	A	B	D
1	X	X	X	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

X = DON'T CARE LOGIC 1 = HIGH
LOGIC 0 = LOW Z = HIGH IMPEDANCE

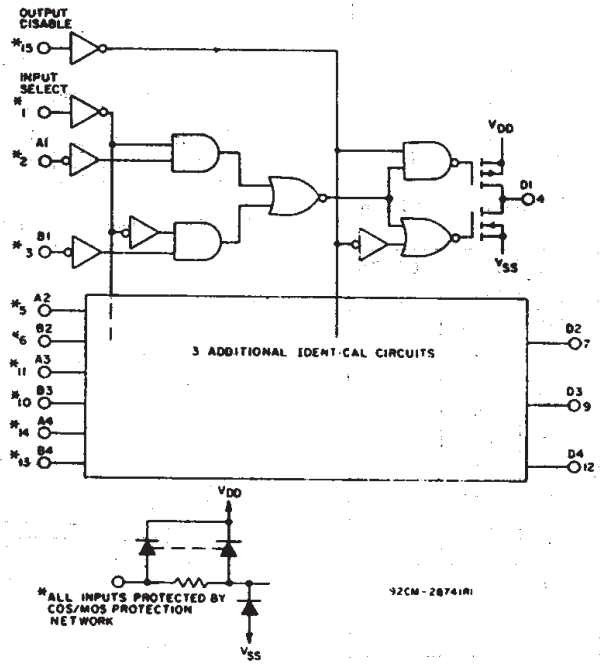


Fig. 1 - Logic diagram for CD40257B.

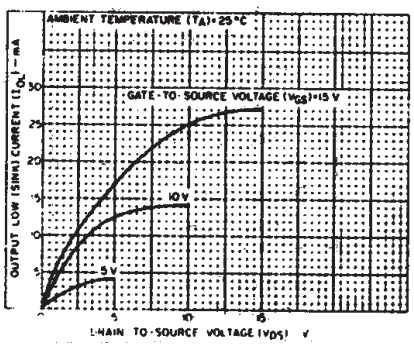


Fig. 2 – Typical output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD}(V)	Typ.	Max.	
Propagation Delay Time: Data Input to Output, t_{PHL}, t_{PLH}	5	150	300	ns
	10	70	140	
	15	50	100	
Select to Output, t_{PHL}, t_{PLH}	5	190	380	ns
	10	85	170	
	15	65	130	
Output Disable to Output, t_{PHL}, t_{PLH}	5	95	190	ns
	10	50	100	
	15	40	80	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

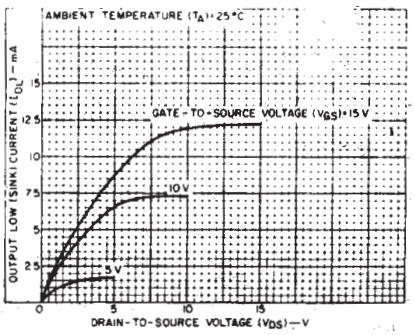


Fig.3 – Minimum output low (sink) current characteristics.

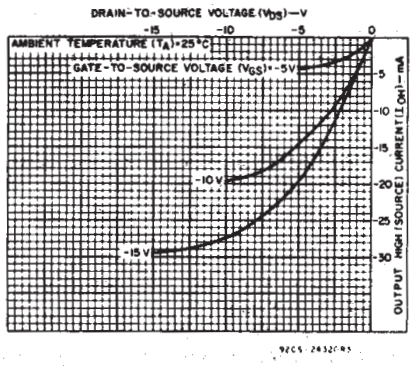


Fig.4 – Typical output high (source) current characteristics.

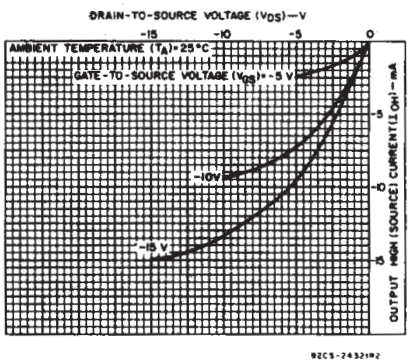


Fig.5 – Minimum output high (source) current characteristics.

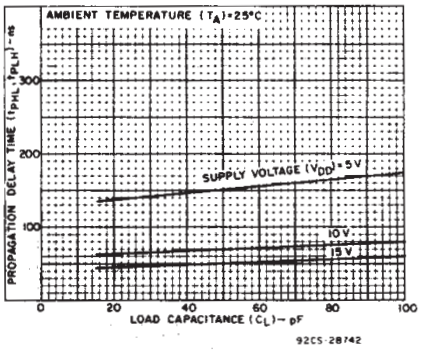


Fig.6 – Typical propagation delay time as a function of load capacitance (DATA INPUT to OUTPUT).

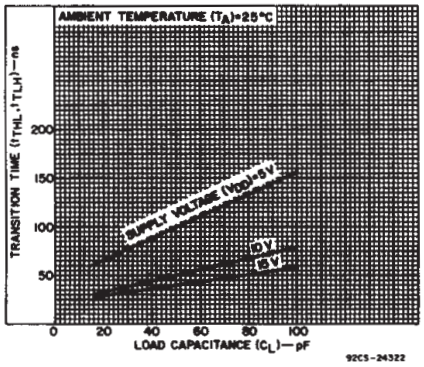


Fig.7 – Typical transition time as a function of load capacitance.

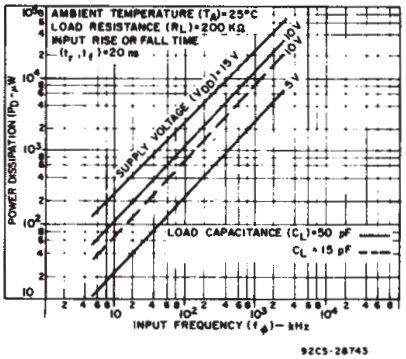


Fig.8 – Typical dynamic power dissipation as a function of input frequency (one INPUT to one OUTPUT).

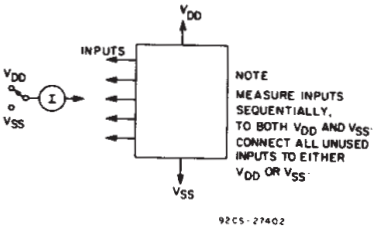


Fig.9 – Input current test circuit.

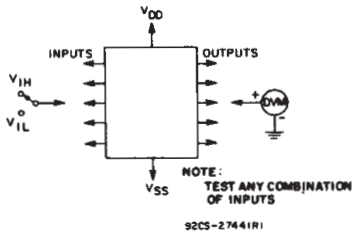


Fig.10 – Input voltage test circuit.

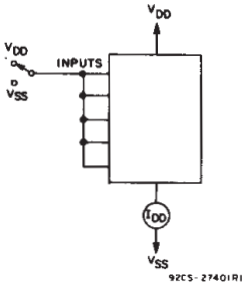
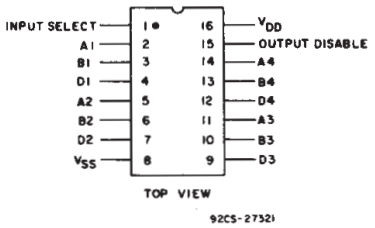
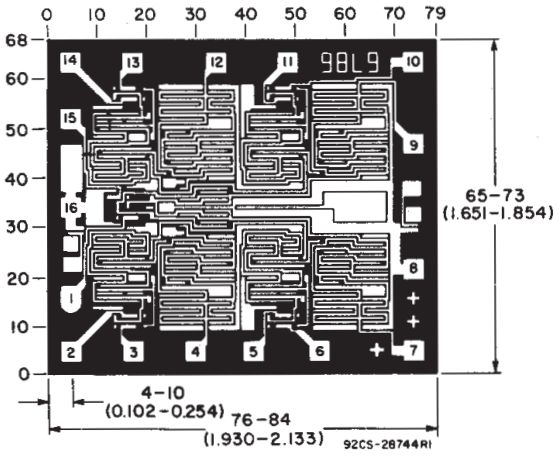


Fig.11 – Quiescent device current test circuit.



TERMINAL ASSIGNMENT

Dimensions and pad layout for CD40257BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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