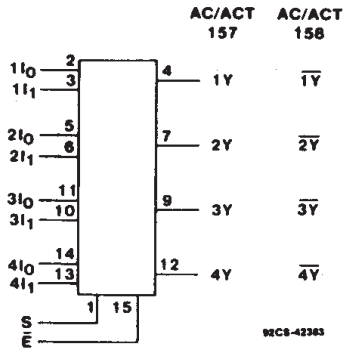
# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS283




FUNCTIONAL DIAGRAM

## Quad 2-Input Multiplexers

**AC/ACT157 - Non-Inverting**
**AC/ACT158 - Inverting**

**Type Features:**

- *Buffered inputs*
- *Typical propagation delay (AC/ACT158): 3.8 ns @ $V_{CC}$ = 5 V, $T_A$ = 25°C, $C_L$ = 50 pF*

The RCA CD54/74AC157, -158 and CD54/74ACT157, -158 quad 2-input multiplexers use the RCA ADVANCED CMOS technology. Both circuits can select four bits of data from two sources under the control of a common select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs of the 158 are forced HIGH and in the 157, all of the outputs are forced LOW, regardless of all other input conditions.

The CD74AC/ACT157 and CD74AC/ACT158 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC157, -158 and CD54ACT157, -158, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

**Family Features:**

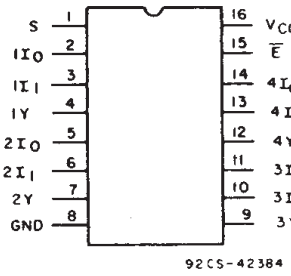
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

*®FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

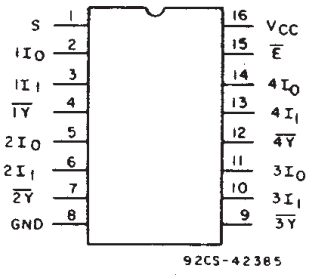
**TRUTH TABLE**

| Enable | Select Input | Data Inputs | | Output | |
|---|---|---|---|---|---|
| | | | | 157 | 158 |
| $\overline{E}$ | S | $I_0$ | $I_1$ | Y | $\overline{Y}$ |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = High level, L = Low level, X = Don't care




CD54/74AC/ACT157




CD54/74AC/ACT158

9

This data sheet is applicable to the CD54/74AC157 and CD74AC158. The CD54AC158, CD54ACT157, and CD54ACT158 were not acquired from Harris Semiconductor. See SCHS238 for information on the CD74ACT157 and CD74ACT158.

File Number **1910**

# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE ($V_{CC}$) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC $V_{CC}$ or GROUND CURRENT ($I_{CC}$ or $I_{GND}$) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For $T_A$ = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55 to +125°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range, $V_{CC}$*: (For $T_A$ = Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage, $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature, $T_A$ | -55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V(AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V(AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V(ACT Types) | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage $V_{IL}$ | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158

**STATIC ELECTRICAL CHARACTERISTICS: ACT Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| Low-Level Input Voltage $V_{IL}$ | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$ | $V_{CC}$-2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**ACT INPUT LOADING TABLE**

| INPUT | UNIT LOAD* | |
|---|---|---|
| | 157 | 158 |
| I (All) | 0.37 | 0.37 |
| $\overline{E}$ | 0.83 | 0.83 |
| S | 1.33 | 1.33 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158

**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | -40 to +85 | | -55 to +125 | | |
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 97 | — | 106 | ns |
| | | | 3.3* | 3.2 | 10.8 | 3 | 11.9 | |
| | | | 5† | 2.2 | 7.7 | 2.1 | 8.5 | |
| $\overline{\text{Enable}}$ to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 154 | — | 169 | ns |
| | | | 3.3 | 5.1 | 17.2 | 4.7 | 18.9 | |
| | | | 5 | 3.6 | 12.3 | 3.4 | 13.5 | |
| Select to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 164 | — | 180 | ns |
| | | | 3.3 | 5.4 | 18.5 | 5.1 | 20.3 | |
| | | | 5 | 3.8 | 13.2 | 3.6 | 14.5 | |
| Data to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 91 | — | 100 | ns |
| | | | 3.3 | 3 | 12.8 | 2.8 | 11.2 | |
| | | | 5 | 2.2 | 7.3 | 2 | 8 | |
| $\overline{\text{Enable}}$ to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 135 | — | 149 | ns |
| | | | 3.3 | 4.5 | 15.2 | 4.2 | 16.7 | |
| | | | 5 | 3.2 | 10.8 | 3 | 11.9 | |
| Select to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 147 | — | 161 | ns |
| | | | 3.3 | 4.9 | 16.5 | 4.5 | 18.1 | |
| | | | 5 | 3.5 | 11.7 | 3.2 | 12.9 | |
| Power Dissipation Capacitance | (157) (158) | $C_{PD}$§ | — | 156 Typ. 149 Typ. | | 156 Typ. 149 Typ. | | pF |
| Input Capacitance | | $C_I$ | — | — | 10 | — | 10 | pF |

**SWITCHING CHARACTERISTIS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | -40 to +85 | | -55 to +125 | | |
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 5† | 2.5 | 8.6 | 2.4 | 9.5 | ns |
| $\overline{\text{Enable}}$ to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 5 | 3.6 | 12.3 | 3.4 | 13.5 | ns |
| Select to Output | (157) | $t_{PLH}$ $t_{PHL}$ | 5 | 3.8 | 13.2 | 3.6 | 14.5 | ns |
| Data to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 5 | 2.4 | 8.4 | 2.3 | 9.2 | ns |
| $\overline{\text{Enable}}$ to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 5 | 3.3 | 11.3 | 3.1 | 12.4 | ns |
| Select to Output | (158) | $t_{PLH}$ $t_{PHL}$ | 5 | 3.6 | 12.3 | 3.4 | 13.5 | ns |
| Power Dissipation Capacitance | (157) (158) | $C_{PD}$§ | — | 156 Typ. 149 Typ. | | 156 Typ. 149 Typ. | | pF |
| Input Capacitance | | $C_I$ | — | — | 10 | — | 10 | pF |

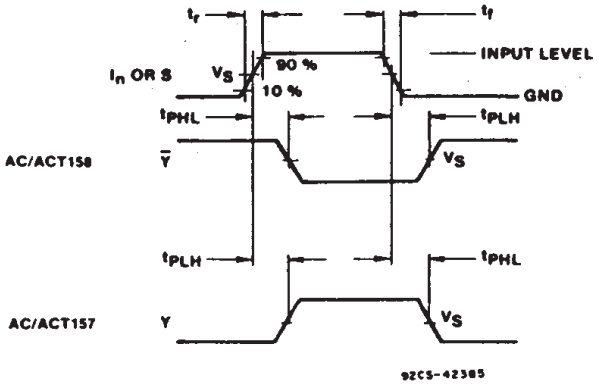
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

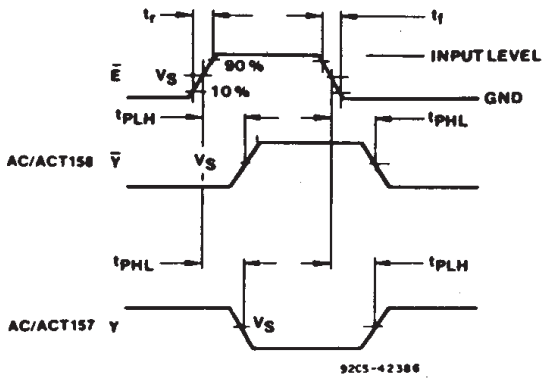
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption, per function.
For AC Series, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o)$
For ACT Series, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$
where $f_i$ = input frequency
$f_o$ = output frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage

9

# CD54/74AC157, CD54/74AC158
# CD54/74ACT157, CD54/74ACT158




| | CD54/74AC | CD54/74ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5 V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

*Fig. 3 - Inputs or select to output propagation delays.*

*Fig. 4 - $\overline{Enable}$ to output propagation delays.*

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.