TEXAS INSTRUMENTS

# CY74FCT399T

SCCS024 - March 1994 - Revised February 2000

# Quad 2-Input Register

## Features

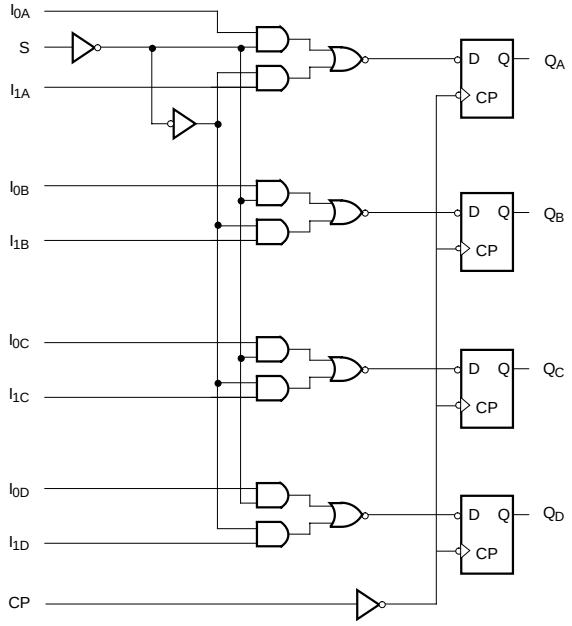
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 6.1 ns max. FCT-A speed at 7.0 ns max.**
- **Reduced $V_{OH}$ (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Extended commercial range of –40˚C to +85˚C**
- **Sink current 64 mA**
  **Source current 32 mA (Com'l),**

## Functional Description

The FCT399T is a high-speed quad dual-port register that selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs ($I_{0X}$, $I_{1X}$) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation. The FCT399T offers true outputs.

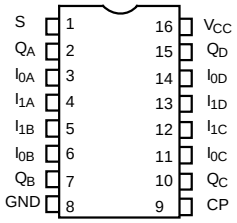
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

## Logic Block Diagram

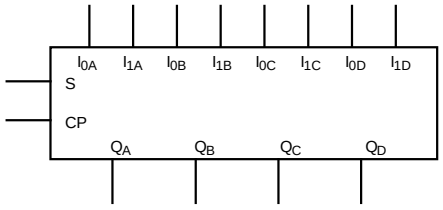



## Pin Configurations

SOIC
Top View




## Logic Symbol




## Pin Description

| Name | Description |
|---|---|
| S | Common Select Input |
| CP | Clock Pulse Input (Active Rising Edge) |
| $I_0$ | Data Inputs from Source 0 |
| $I_1$ | Data Inputs from Source 1 |
| Q | Register True Outputs |

## Function Table[1]

| Inputs | | | Outputs |
|---|---|---|---|
| **S** | **$I_0$** | **$I_1$** | **Q** |
| l | l | X | L |
| l | h | X | H |
| h | X | l | L |
| h | X | h | H |

**Note:**

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care

## Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage.....–0.5V to +7.0V

DC Output Voltage.....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation .....0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

## Operating Range

| Range | Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|---|
| Commercial | All | –40°C to +85°C | 5V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=–32 mA | 2.0 | | | V |
| | | $V_{CC}$=Min., $I_{OH}$=–15 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=64 mA | | 0.3 | 0.55 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_H$ | Hysteresis[5] | All inputs | | 0.2 | | V |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$=Min., $I_{IN}$=–18 mA | | –0.7 | –1.2 | V |
| $I_I$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=$V_{CC}$ | | | 5 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=2.7V | | | ±1 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$=Max., $V_{IN}$=0.5V | | | ±1 | µA |
| $I_{OS}$ | Output Short Circuit Current[6] | $V_{CC}$=Max., $V_{OUT}$=0.0V | –60 | –120 | –225 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$=0V, $V_{OUT}$=4.5V | | | ±1 | µA |

## Capacitance[5]

| Parameter | Description | Typ.[4] | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | 9 | 12 | pF |

**Notes:**

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.
4. Typical values are at $V_{CC}$=5.0V, $T_A$=+25˚C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques is preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs) | $V_{CC}$=Max., $V_{IN}$=3.4V, $f_1$=0, Outputs Open [7] | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[8] | $V_{CC}$=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 0.06 | 0.12 | mA/MHz |
| $I_C$ | Total Power Supply Current[9] | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1$=5 MHz, S=Steady State $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 0.7 | 1.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1$=5 MHz, S=Steady State $V_{IN}$=3.4V or $V_{IN}$=GND | 1.2 | 3.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Four Inputs Toggling at $f_1$=5 MHz, S=Steady State $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V | 1.6 | 3.2[10] | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Four Inputs Toggling at $f_1$=5 MHz, S=Steady State $V_{IN}$=3.4V or $V_{IN}$=GND | 2.9 | 8.2[10] | mA |

**Notes:**

7. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
   $I_{CC}$ = Quiescent Current with CMOS input levels
   $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input ($V_{IN}$=3.4V)
   $D_H$ = Duty Cycle for TTL inputs HIGH
   $N_T$ = Number of TTL inputs at $D_H$
   $I_{CCD}$ = Dynamic Current caused by an input transition pair (HLH or LHL)
   $f_0$ = Clock frequency for registered devices, otherwise zero
   $f_1$ = Input signal frequency
   $N_1$ = Number of inputs changing at $f_1$
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the $I_{CC}$ formula. These limits are specified but not tested.

## Switching Characteristics Over the Operating Range[11]

| Parameter | Description | CY74FCT399AT Commercial Min. | CY74FCT399AT Commercial Max. | CY74FCT399CT Commercial Min. | CY74FCT399CT Commercial Max. | Unit | Fig. No.[12] |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to Q | 2.5 | 7.0 | 2.5 | 6.1 | ns | 1, 5 |
| $t_S$ | Set-Up Time HIGH or LOW<br>$I_n$ to CP | 3.5 | | 3.5 | | ns | 4 |
| $t_H$ | Hold Time HIGH or LOW<br>$I_n$ to CP | 1.0 | | 1.0 | | ns | 4 |
| $t_S$ | Set-Up Time HIGH or LOW<br>S to CP | 8.5 | | 8.5 | | ns | 4 |
| $t_H$ | Hold Time HIGH or LOW<br>S to CP | 0 | | 0 | | ns | 4 |
| $t_W$ | Clock Pulse Width[5]<br>HIGH or LOW | 5.0 | | 5.0 | | ns | 5 |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 6.1 | CY74FCT399CTSOC/SOCT | S1 | 16-Lead (300-Mil) Molded SOIC | Commercial |
| 7.0 | CY74FCT399ATSOC/SOCT | S1 | 16-Lead (300-Mil) Molded SOIC | Commercial |

**Notes:**
11. Minimum limits are specified but not tested on Propagation Delays.
12. See “Parameter Measurement Information” in the General Information Section.

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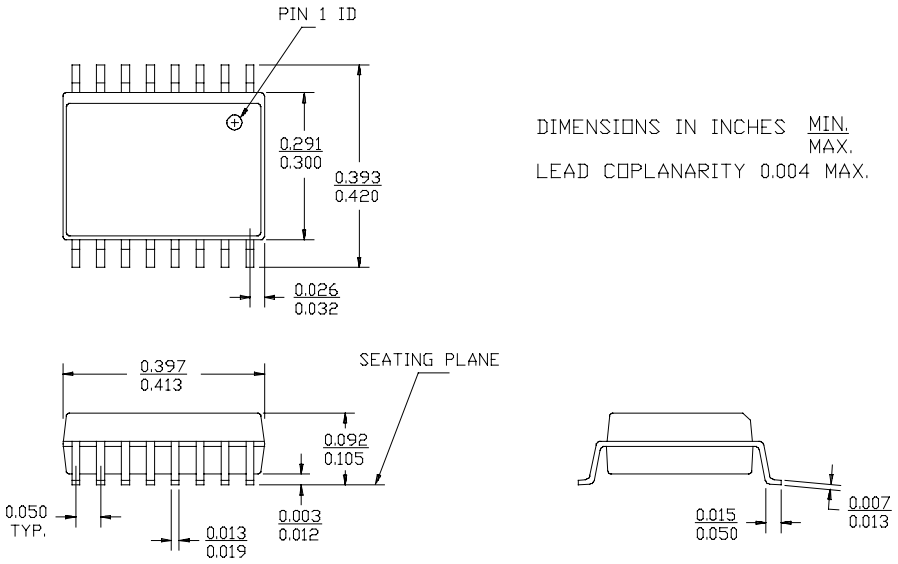
## Package Diagrams

**16-Lead Molded SOIC S1**



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