features

- **Dual-Input, Single-Output MOSFET Switch With No Reverse Current Flow (No Parasitic Diodes)**
- **IN1 . . . 250-mΩ, 500-mA N-Channel; 14-μA Supply Current**
- **IN2 . . . 1.3-Ω, 100-mA P-Channel; 0.75-μA Supply Current (V$_{AUX}$ Mode)**
- **Advanced Switch Control Logic**
- **CMOS and TTL Compatible Enable Input**
- **Controlled Rise, Fall, and Transition Times**
- **2.7 V to 4 V Operating Range**
- **SOT-23-5 and SOIC-8 Package**
- **–40°C to 70°C Ambient Temperature Range**
- **2-kV Human Body Model, 750-V Charged Device Model, 200-V Machine-Model ESD Protection**

typical applications

- **Notebook and Desktop PCs**
- **Cell phone, Palmtops, and PDAs**
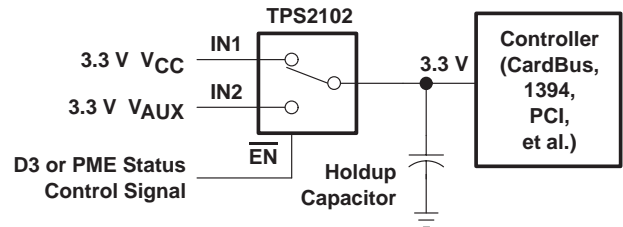- **Battery Management**

Figure 1. Typical Dual-Input Single-Output Application

description

The TPS2102 and TPS2103 are dual-input, single-output power switches designed to provide uninterrupted output voltage when transitioning between two independent power supplies. Both devices combine one n-channel (250 mΩ) and one p-channel (1.3 Ω) MOSFET with a single output. The p-channel MOSFET (IN2) is used with auxiliary power supplies that deliver lower current for standby modes. The n-channel MOSFET (IN1) is used with a main power supply that delivers higher current required for normal operation. Low on-resistance makes the n-channel the ideal path for higher main supply current when power-supply regulation and system voltage drops are critical. When using the p-channel MOSFET, quiescent current is reduced to 0.75 μA to decrease the demand on the standby power supply. The MOSFETs in the TPS2102 and TPS2103 do not have the parasitic diodes, typically found in discrete MOSFETs, thereby preventing back-flow current when the switch is off.
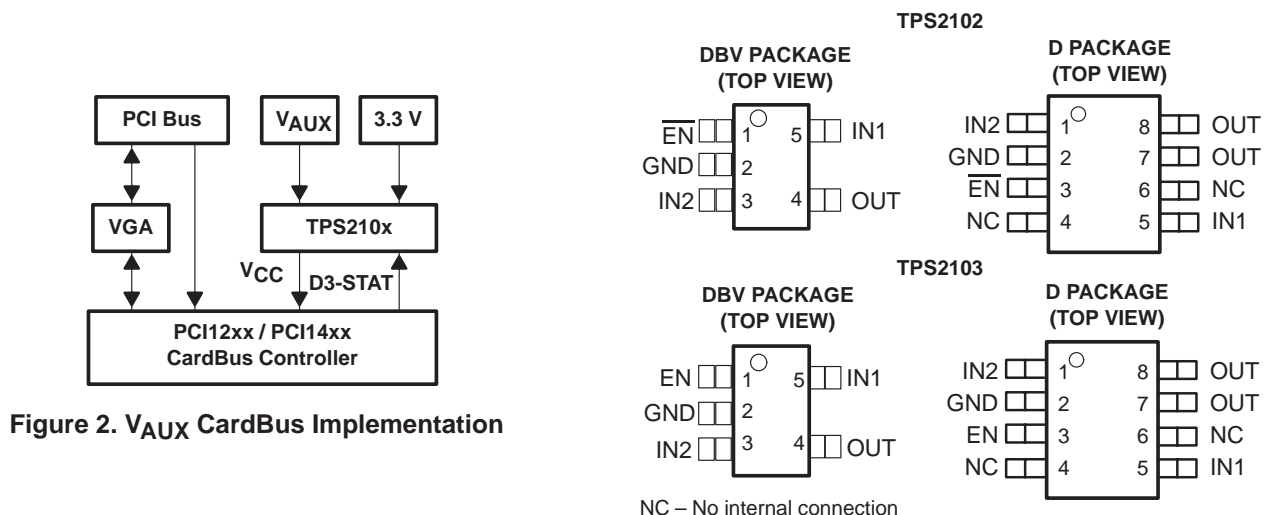

Figure 2. V$_{AUX}$ CardBus Implementation

NC – No internal connection

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TPS2102, TPS2103
V$_{AUX}$ POWER-DISTRIBUTION SWITCHES

Selection Guide, V$_{AUX}$ Power-Distribution Switches

DEVICE	ENABLE	OPERATING VOLTAGE RANGE (V)	MAXIMUM INPUT CURRENT, IN1 (mA)	MAXIMUM INPUT CURRENT, IN2 (mA)	AMBIENT TEMPERATURE RANGE (°C)
TPS2100	$\overline{EN}$	2.7 to 4	500	10	−40 to 70
TPS2101	EN	2.7 to 4	500	10	−40 to 70
TPS2102	$\overline{EN}$	2.7 to 4	500	100	−40 to 70
TPS2103	EN	2.7 to 4	500	100	−40 to 70
TPS2104	$\overline{EN}$	2.7 to 5.5	500	100	−40 to 85
TPS2105	EN	2.7 to 5.5	500	100	−40 to 85

AVAILABLE OPTIONS FOR TPS2102, TPS2103

T$_A$	DEVICE	ENABLE	PACKAGED DEVICES	
			SOT-23-5 (DBV)[†]	SOIC-8 (D)
−40°C to 70°C	TPS2102	$\overline{EN}$	TSP2102DBV[†]	TPS2102D
	TPS2103	EN	TPS2103DBV[†]	TPS2103D

Both packages are available left-end taped and reeled. Add an R suffix to the D device type (e.g., TPS2103DR).

[†] Add T (e.g., TPS2102DBVT) to indicate tape and reel at order quantity of 250 parts.
Add R (e.g., TPS2102DBVR) to indicate tape and reel at order quantity of 3000 parts.

Function Tables

TPS2102			
VIN1	VIN2	$\overline{EN}$	OUT
0 V	0 V	XX	GND
0 V	3.3 V	L	GND
3.3 V	0 V	L	VIN1
3.3 V	3.3 V	L	VIN1
0 V	3.3 V	H	VIN2
3.3 V	0 V	H	VIN2
3.3 V	3.3 V	H	VIN2

TPS2103			
VIN1	VIN2	EN	OUT
0 V	0 V	XX	GND
0 V	3.3 V	H	GND
3.3 V	0 V	H	VIN1
3.3 V	3.3 V	H	VIN1
0 V	3.3 V	L	VIN2
3.3 V	0 V	L	VIN2
3.3 V	3.3 V	L	VIN2

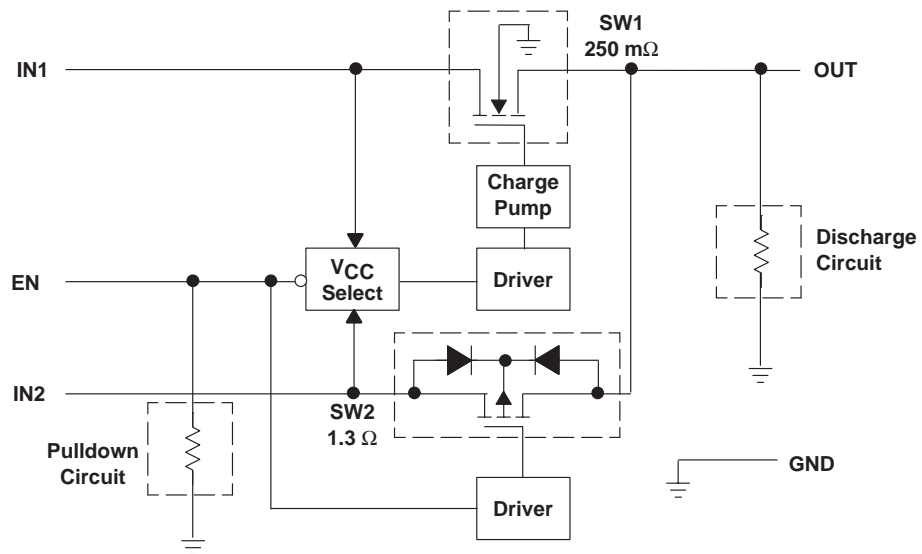XX = don't care

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TPS2102 functional block diagram

TPS2103 functional block diagram

TPS2102, TPS2103
V_AUX POWER-DISTRIBUTION SWITCHES

Terminal Functions

NAME	TERMINAL				I/O	DESCRIPTION
	NO.					
	TPS2102		TPS2103			
	DBV	D	DBV	D		
EN			1	3	I	Active-high enable for IN1-OUT switch
$\overline{EN}$	1	3			I	Active-low enable for IN1-OUT switch
GND	2	2	2	2	I	Ground
IN1†	5	5	5	5	I	Main Input voltage, NMOS drain (250 mΩ), require 0.22 µF bypass
IN2†	3	1	3	1	I	Auxilliary input voltage, PMOS drain (1.3 Ω), require 0.22 µF bypass
OUT	4	7, 8	4	7, 8	O	Power switch output
NC		4, 6		4, 6		No connection

† Unused INx should not be grounded.

detailed description

power switches

n-channel MOSFET

The IN1-OUT n-channel MOSFET power switch has a typical on-resistance of 250 mΩ at 3.3-V input voltage, and is configured as a high-side switch.

p-channel MOSFET

The IN2-OUT p-channel MOSFET power switch has a typical on-resistance of 1.3 Ω at 3.3-V input voltage and is configured as a high-side switch. When operating, the p-channel MOSFET quiescent current is reduced to typically 0.75 µA.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the IN1-OUT and IN2-OUT power switches. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the drivers incorporate circuitry that controls the rise times and fall times of the output voltage.

enable

The logic enable will turn on the IN2-OUT power switch when a logic high is present on $\overline{EN}$ (TPS2102) or logic low is present on EN (TPS2103). A logic low input on $\overline{EN}$ (TPS2102) or logic high on EN (TPS2103) restores bias to the drive and control circuits and turns on the IN1-OUT power switch. The enable input is compatible with both TTL and CMOS logic levels.

the V_AUX application for CardBus controllers

The PC Card specification requires the support of V_{AUX} to the CardBus controller as well as to the PC Card sockets. Both are 3.3-V requirements; however the CardBus controller's current demand from the V_{AUX} supply is limited to 10 µA, whereas the PC Card may consume as much as 200 mA. In either implementation, if support of a wake-up event is required, the controller and the socket will transition from the 3.3-V V_{CC} rail to the 3.3-V V_{AUX} rail when the equipment moves into a low power mode such as D3. The transition from V_{CC} to V_{AUX} needs to be seamless in order to maintain all memory and register information in the system. If V_{AUX} is not supported, the system will lose all register information when it transitions to the D3 state.

TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, $V_{I(IN1)}$ (see Note 1) .... −0.3 V to 5 V

Input voltage range, $V_{I(IN2)}$ (see Note 1) .... −0.3 V to 5 V

Input voltage range, V_I at $\overline{EN}$ or EN (see Note 1) .... −0.3 V to 5 V

Output voltage range, V_O (see Note 1) .... −0.3 V to 5 V

Continuous output current, $I_{O(IN1)}$ .... 700 mA

Continuous output current, $I_{O(IN2)}$ .... 140 mA

Continuous total power dissipation .... See dissipation rating table

Operating virtual junction temperature range, T_J .... −40°C to 85°C

Storage temperature range, T_{stg} .... −65°C to 150°C

Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

Electrostatic discharge (ESD) protection: Human body model .... 2 kV

Machine model .... 200 V

Charged device model .... 750 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	309 mW	3.1 mW/°C	170 mW	123 mW
D	568 mW	5.7 mW/°C	313 mW	227 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(INx)}$	2.7	4	V
Input voltage, V_I at $\overline{EN}$ and EN	0	4	V
Continuous output current, $I_{O(IN1)}$		500	mA
Continuous output current, $I_{O(IN2)}$		100‡	mA
Operating virtual junction temperature, T_J	−40	85	°C

‡ The device can deliver up to 220 mA at $I_{O(IN2)}$. However, operation at the higher current levels will result in greater voltage drop across the device, and greater voltage droop when switching between IN1 and IN2.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN1)} = V_{(IN2)} = 3.3$ V, I_O = rated current (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$r_{DS(on)}$ On-state resistance	IN1-OUT	T_J = 25°C		250		mΩ
		T_J = 85°C		300	375	
	IN2-OUT	T_J = 25°C		1.3		Ω
		T_J = 85°C		1.5	2.1	

† Pulse-testing techniques maintain junction temperature close to ambient termperature; thermal effects must be taken into account separately.

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating junction temperature range, V$_{I(IN1)}$ = V$_{(IN2)}$ = 3.3 V, I$_O$ = rated current (unless otherwise noted) (continued)

enable input ($\overline{EN}$ and EN)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V$_{IH}$	High-level input voltage	2.7 V ≤ V$_{I(INx)}$ ≤ 4 V		2			V
V$_{IL}$	Low-level input voltage	2.7 V ≤ V$_{I(INx)}$ ≤ 4 V				0.8	V
I$_I$	Input current	TPS2102	$\overline{EN}$ = 0 V or $\overline{EN}$ = V$_{I(INx)}$	−0.5		0.5	µA
		TPS2103	EN = 0 V or EN = V$_{I(INx)}$	−0.5		0.5	µA

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I$_I$	Supply current	TPS2102	$\overline{EN}$ = H, IN2 selected	T$_J$ = 25°C		0.75		µA
				−40°C ≤ T$_J$ ≤ 85°C			1.5	
			$\overline{EN}$ = L, IN1 selected	T$_J$ = 25°C		14		µA
				−40°C ≤ T$_J$ ≤ 85°C			24	
		TPS2103	EN = L, IN2 selected	T$_J$ = 25°C		0.75		µA
				−40°C ≤ T$_J$ ≤ 85°C			1.5	
			EN = H, IN1 selected	T$_J$ = 25°C		14		µA
				−40°C ≤ T$_J$ ≤ 85°C			24	

switching characteristics, T$_J$ = 25°C, V$_{I(IN1)}$ = V$_{I(IN2)}$ = 3.3 V (unless otherwise noted)[†]

PARAMETER			TEST CONDITIONS[†]		MIN	TYP	MAX	UNIT
t$_r$	Output rise time	IN1-OUT	V$_{I(IN2)}$ = 0	C$_L$ = 1 µF, I$_L$ = 500 mA		440		µs
				C$_L$ = 10 µF, I$_L$ = 500 mA		440		
				C$_L$ = 1 µF, I$_L$ = 100 mA		370		
		IN2-OUT	V$_{I(IN1)}$ = 0	C$_L$ = 1 µF, I$_L$ = 100 mA		4.6		
				C$_L$ = 10 µF, I$_L$ = 100 mA		50		
				C$_L$ = 1 µF, I$_L$ = 10 mA		4.6		
t$_f$	Output fall time	IN1-OUT	V$_{I(IN2)}$ = 0	C$_L$ = 1 µF, I$_L$ = 500 mA		5		µs
				C$_L$ = 10 µF, I$_L$ = 500 mA		100		
				C$_L$ = 1 µF, I$_L$ = 100 mA		13		
		IN2-OUT	V$_{I(IN1)}$ = 0	C$_L$ = 1 µF, I$_L$ = 100 mA		68		
				C$_L$ = 10 µF, I$_L$ = 100 mA		680		
				C$_L$ = 1 µF, I$_L$ = 10 mA		720		
t$_{PLH}$	Propagation delay time, low-to-high output	IN1-OUT	V$_{I(IN2)}$ = 0	C$_L$ = 10 µF, I$_L$ = 100 mA		80		µs
		IN2-OUT	V$_{I(IN1)}$ = 0			2		
t$_{PHL}$	Propagation delay time, high-to-low output	IN1-OUT	V$_{I(IN2)}$ = 0	C$_L$ = 10 µF, I$_L$ = 100 mA		3		µs
		IN2-OUT	V$_{I(IN1)}$ = 0			40		

[†] All timing parameters refer to Figure 3.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

Propagation Delay Time, Low-to-High-Level Output

Propagation Delay Time, High-to–Low-Level Output

Rise/Fall Time

Turn-on Transition Time

Turn-off Transition Time
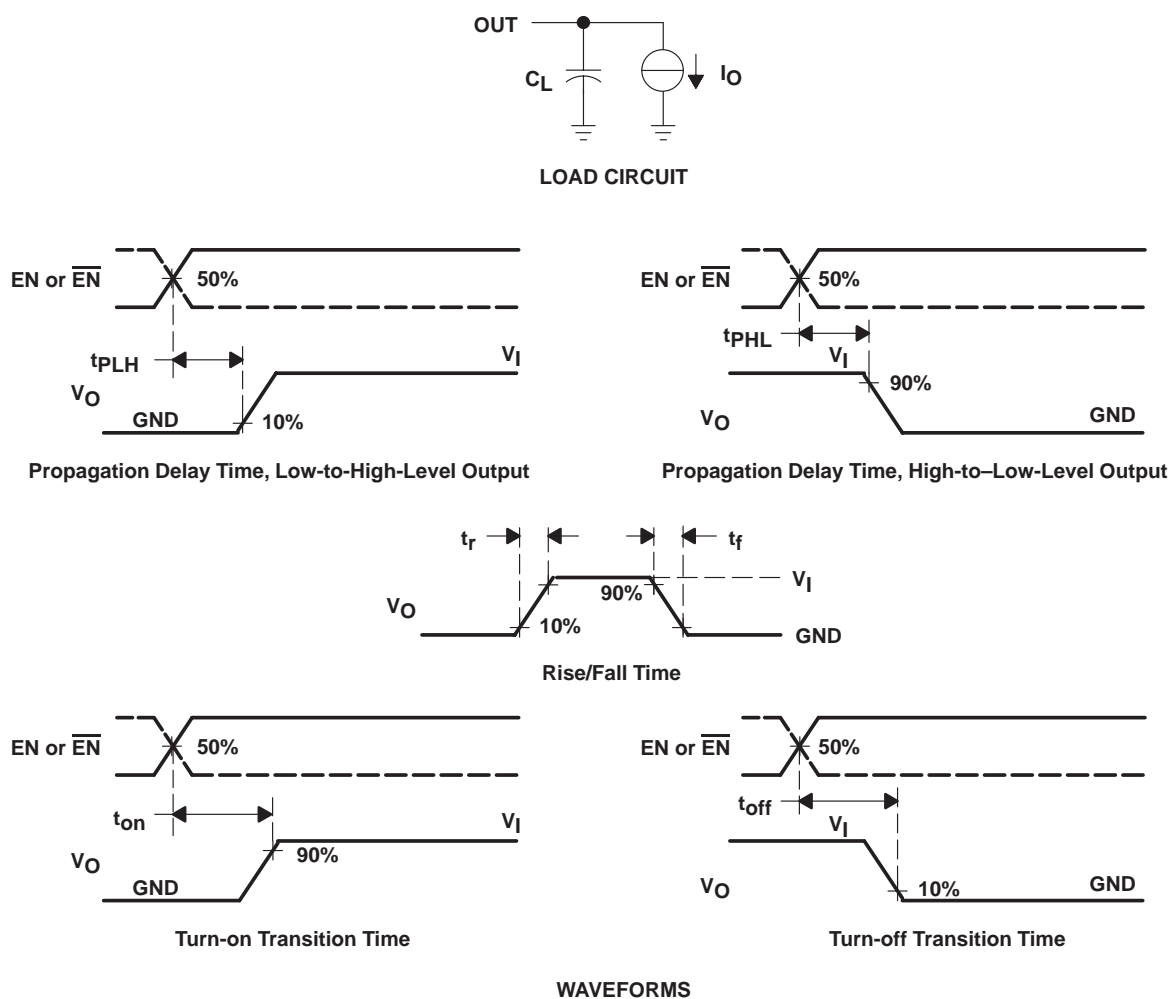
WAVEFORMS

Figure 3. Test Circuit and Voltage Waveforms

Table of Timing Diagrams†

	FIGURE
Propagation Delay and Rise Time With 0.1-μF Load, IN1	4
Propagation Delay and Rise Time With 0.1-μF Load, IN2	5
Propagation Delay and Fall Time With 0.1-μF Load, IN1	6
Propagation Delay and Fall Time With 0.1-μF Load, IN2	7
Propagation Delay and Rise Time With 1-μF Load, IN1	8
Propagation Delay and Rise Time With 1-μF Load, IN2	9
Propagation Delay and Fall Time With 1-μF Load, IN1	10
Propagation Delay and Fall Time With 1-μF Load, IN2	11

† Waveforms shown in Figures 4–11 refer to TPS2102 at T_J = 25°C

TPS2102, TPS2103
V_{AUX} POWER-DISTRIBUTION SWITCHES

PARAMETER MEASUREMENT INFORMATION
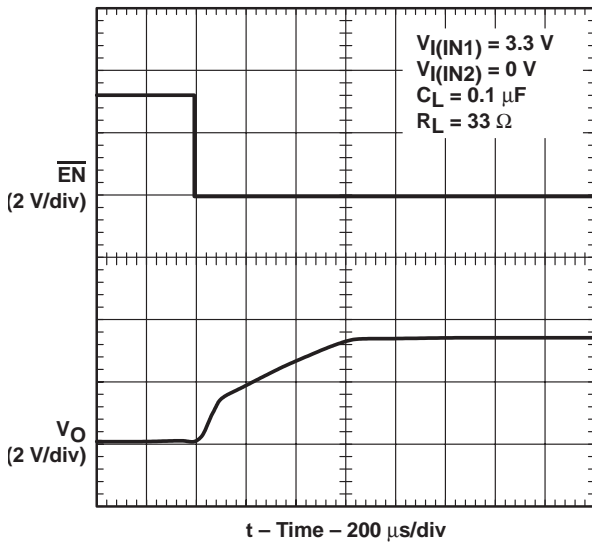
Figure 4. Propagation Delay and Rise Time
With 0.1-μF Load, IN1 Turnon
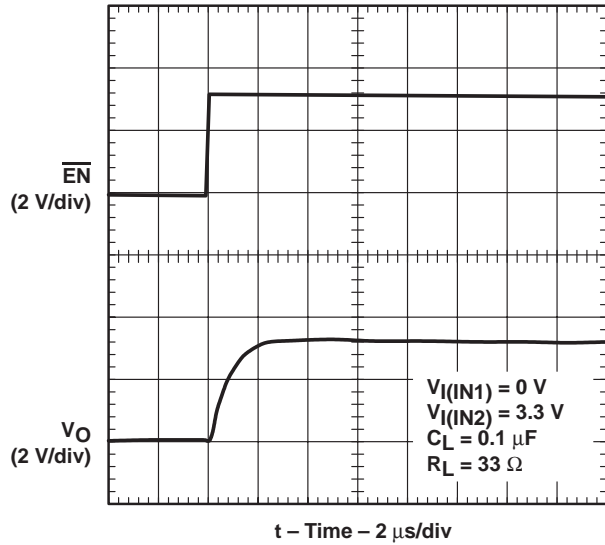
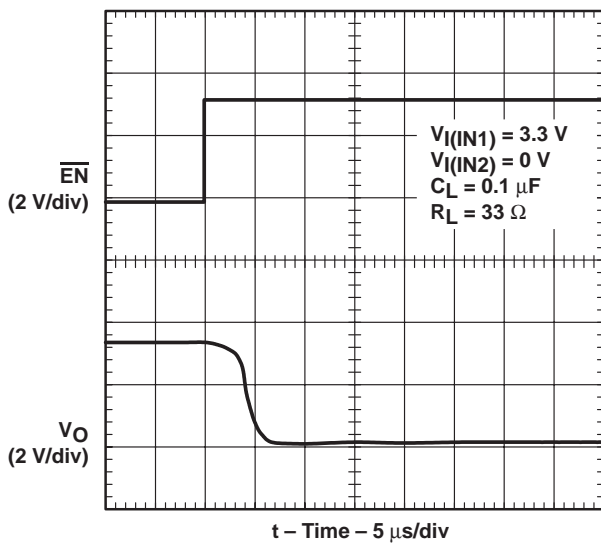Figure 5. Propagation Delay and Fall Time
With 0.1-μF Load, IN2 Turnon

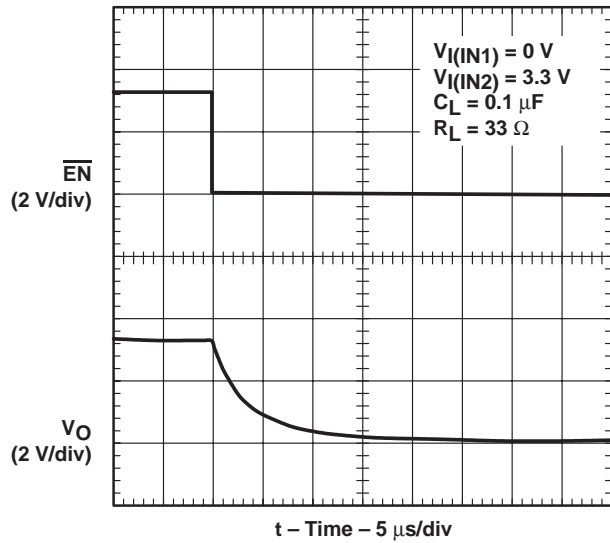Figure 6. Propagation Delay and Fall Time
With 0.1-μF Load, IN1 Turnoff

Figure 7. Propagation Delay and Fall Time
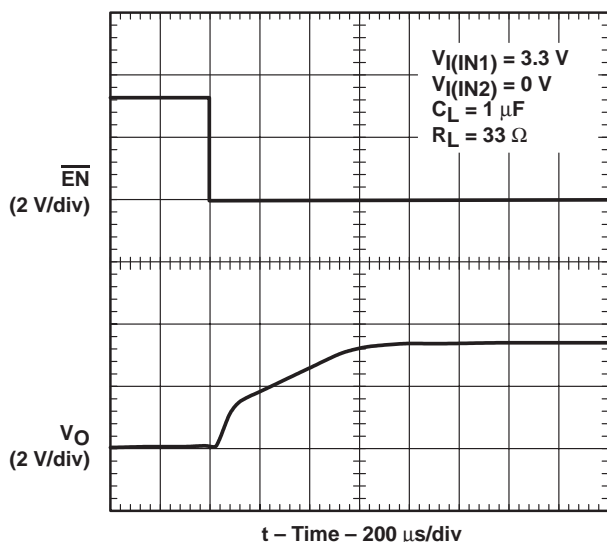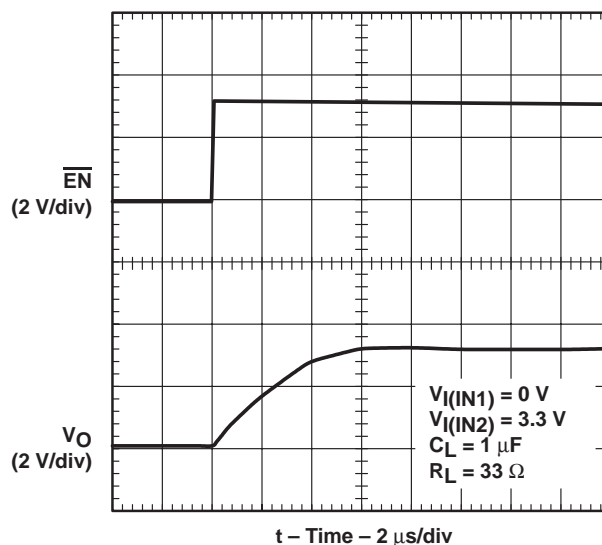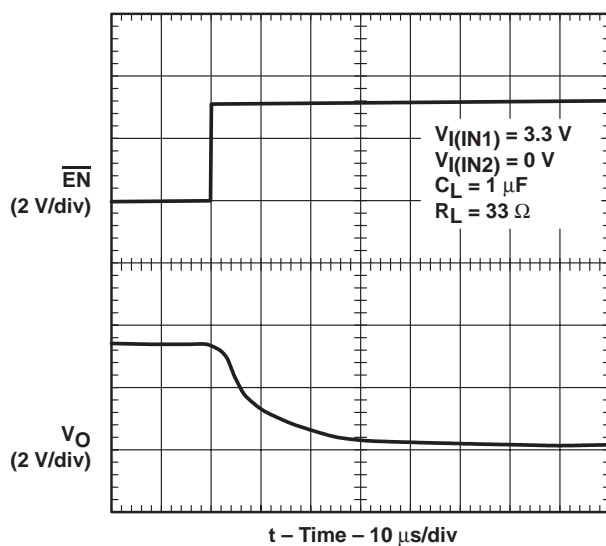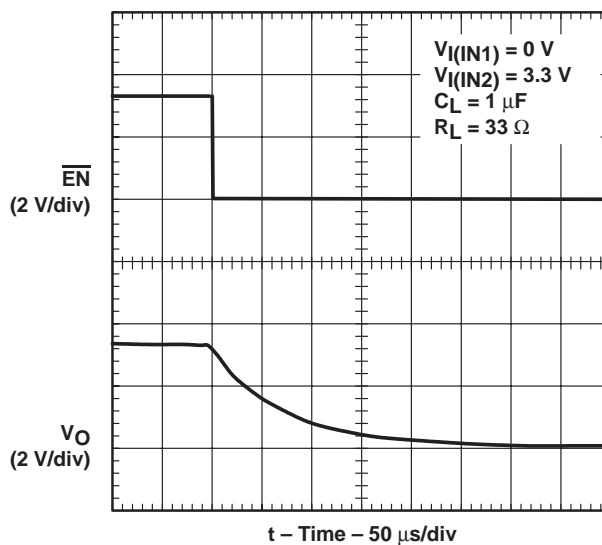With 0.1-μF Load, IN2 Turnoff

PARAMETER MEASUREMENT INFORMATION

$V_{I(IN1)}$ = 3.3 V
$V_{I(IN2)}$ = 0 V
C_L = 1 μF
R_L = 33 Ω

$\overline{EN}$
(2 V/div)

V$_O$
(2 V/div)

t – Time – 200 μs/div

**Figure 8. Propagation Delay and Rise Time
With 1-μF Load, IN1 Turnon**

$\overline{EN}$
(2 V/div)

V$_O$
(2 V/div)

$V_{I(IN1)}$ = 0 V
$V_{I(IN2)}$ = 3.3 V
C_L = 1 μF
R_L = 33 Ω

t – Time – 2 μs/div

**Figure 9. Propagation Delay and Rise Time
With 1-μF Load, IN2 Turnon**

$\overline{EN}$
(2 V/div)

$V_{I(IN1)}$ = 3.3 V
$V_{I(IN2)}$ = 0 V
C_L = 1 μF
R_L = 33 Ω

V$_O$
(2 V/div)

t – Time – 10 μs/div

**Figure 10. Propagation Delay and Fall Time
With 1-μF Load, IN1 Turnoff**

$V_{I(IN1)}$ = 0 V
$V_{I(IN2)}$ = 3.3 V
C_L = 1 μF
R_L = 33 Ω

$\overline{EN}$
(2 V/div)

V$_O$
(2 V/div)

t – Time – 50 μs/div

**Figure 11. Propagation Delay and Fall Time
With 1-μF Load, IN2 Turnoff**

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TPS2102, TPS2103
V$_{AUX}$ POWER-DISTRIBUTION SWITCHES

SLVS234A – SEPTEMBER 1999 – REVISED APRIL 2000

TYPICAL CHARACTERISTICS

Table of Graphs

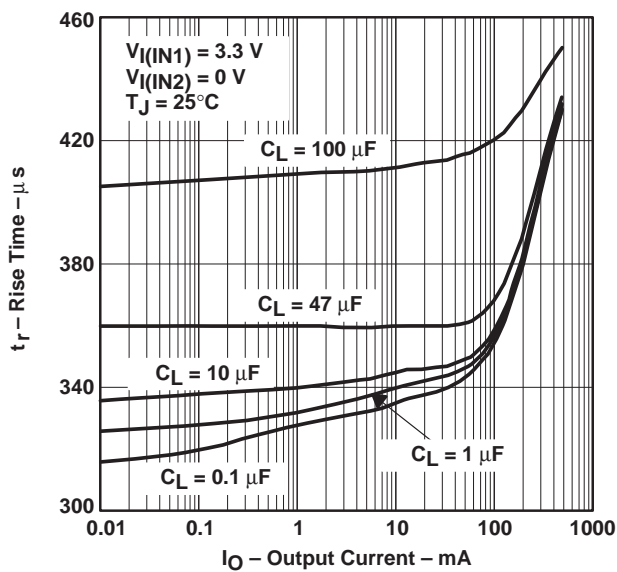|		FIGURE
IN1 Switch Rise Time	vs Output Current	12
IN2 Switch Fall Time	vs Output Current	13
IN1 Switch Fall Time	vs Output Current	14
IN2 Switch Fall Time	vs Output Current	15
Output Voltage Droop	vs Output Current When Output Is Switched From IN2 to IN1	16
Inrush Current	vs Output Capacitance	17
IN1 Supply Current	vs Junction Temperature (IN1 Enabled)	18
IN1 Supply Current	vs Junction Temperature (IN1 Disabled)	19
IN2 Supply Current	vs Junction Temperature (IN2 Enabled)	20
IN2 Supply Current	vs Junction Temperature (IN2 Disabled)	21
IN1-OUT On-State Resistance	vs Junction Temperature	22
IN2-OUT On-State Resistance	vs Junction Temperature	23

IN1 SWITCH RISE TIME
vs
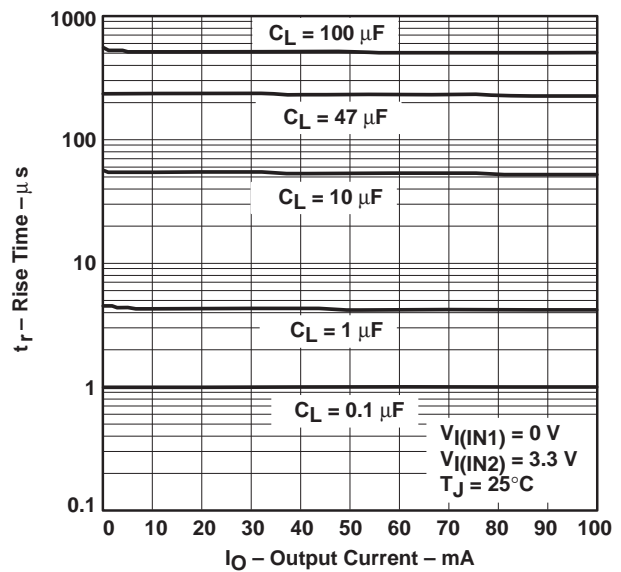OUTPUT CURRENT

Figure 12

IN2 SWITCH RISE TIME
vs
OUTPUT CURRENT

Figure 13

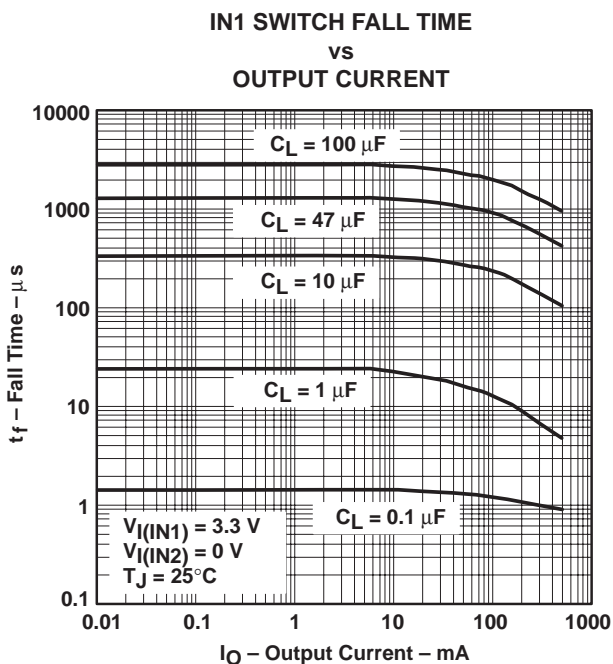POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

IN1 SWITCH FALL TIME
vs
OUTPUT CURRENT

Figure 14

IN2 SWITCH FALL TIME
vs
OUTPUT CURRENT

Figure 15

OUTPUT VOLTAGE DROOP
vs
OUTPUT CURRENT WHEN OUTPUT
IS SWITCHED FROM IN2 TO IN1†
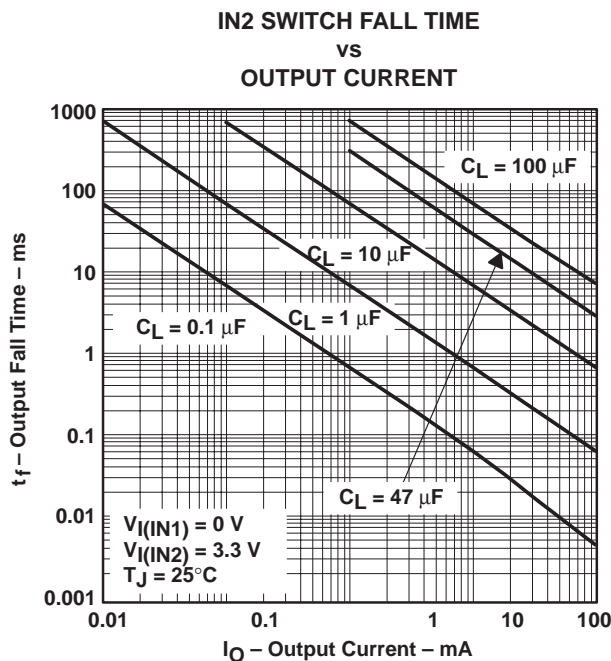

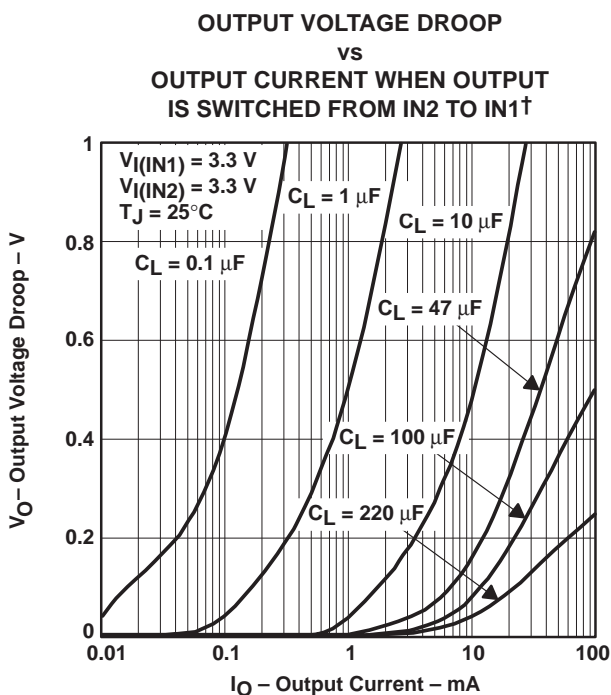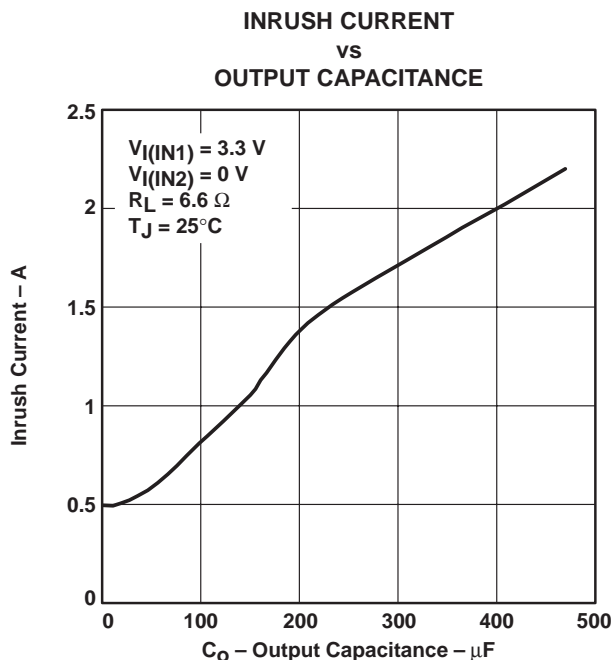**Figure 16**

INRUSH CURRENT
vs
OUTPUT CAPACITANCE

Figure 17

† If switching from IN1 to IN2, the voltage droop is much smaller. Therefore, the load capacitance should be chosen according to the curves in Figure 16.
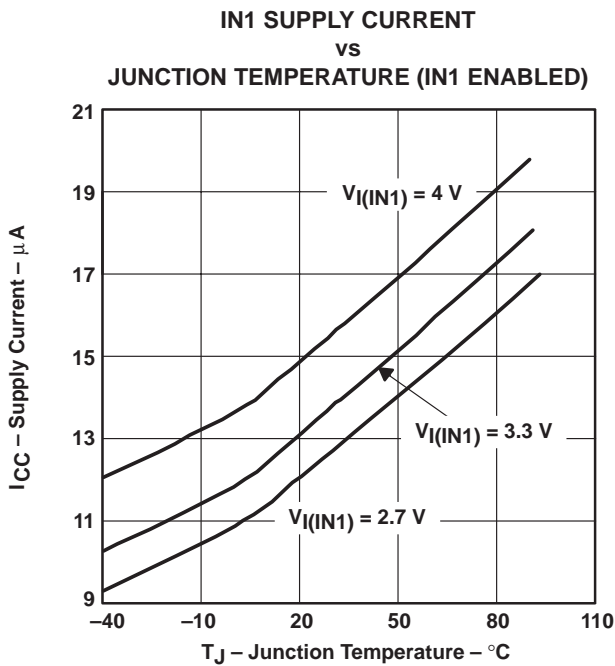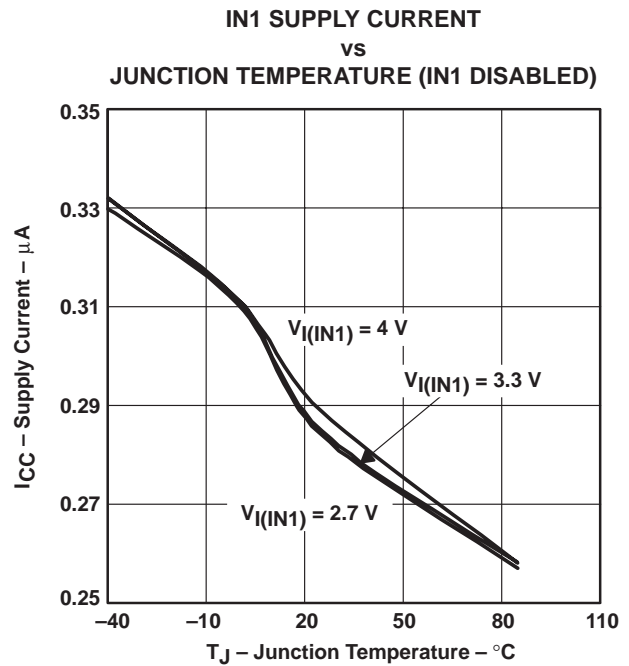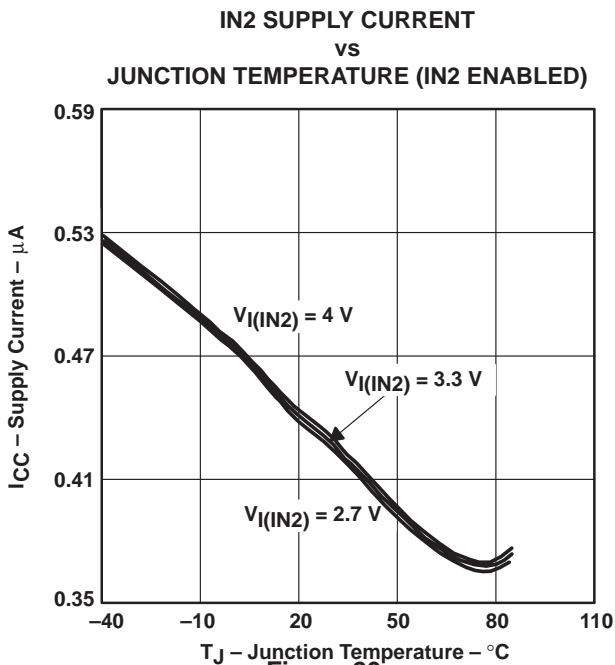
TYPICAL CHARACTERISTICS

IN1 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN1 ENABLED)

Figure 18

IN1 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN1 DISABLED)

Figure 19

IN2 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN2 ENABLED)

Figure 20

IN2 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN2 DISABLED)

Figure 21

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TYPICAL CHARACTERISTICS

IN1-OUT ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

Figure 22

IN2-OUT ON-STATE RESISTANCE
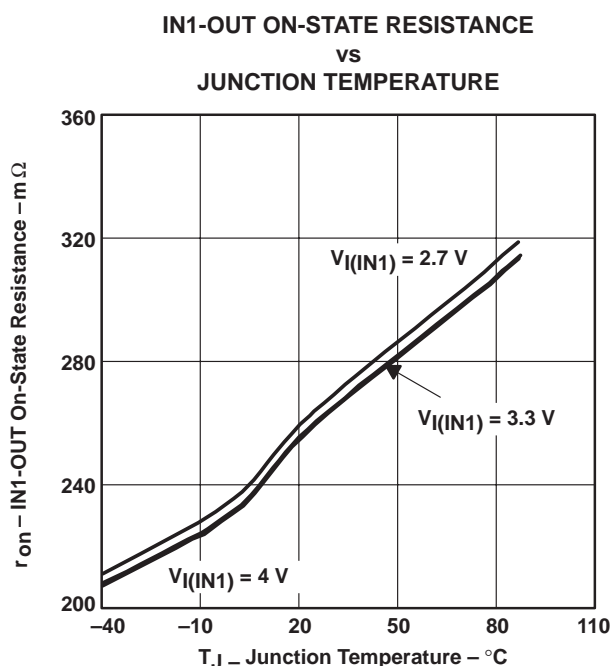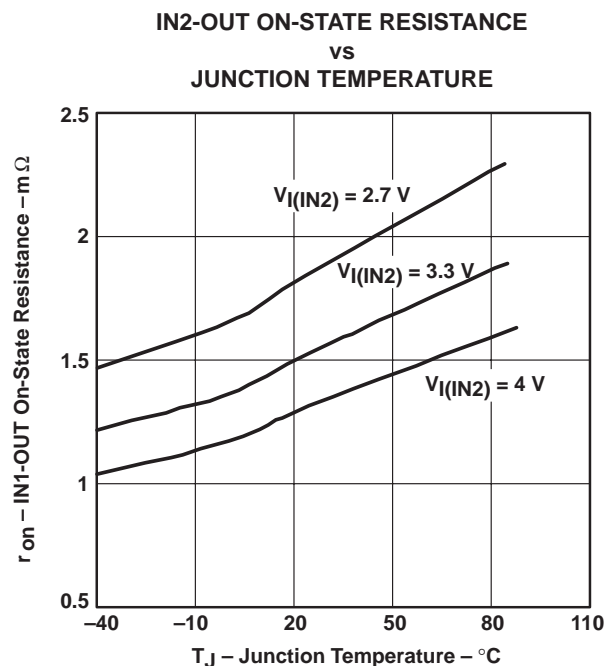**vs**
JUNCTION TEMPERATURE
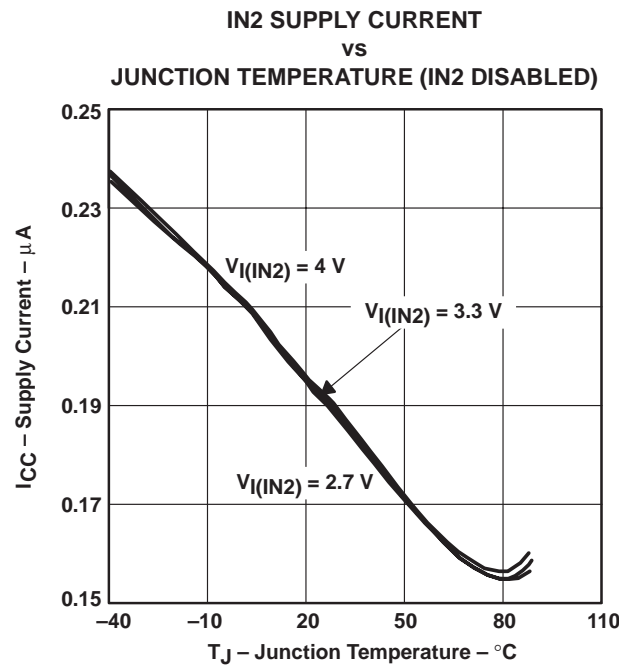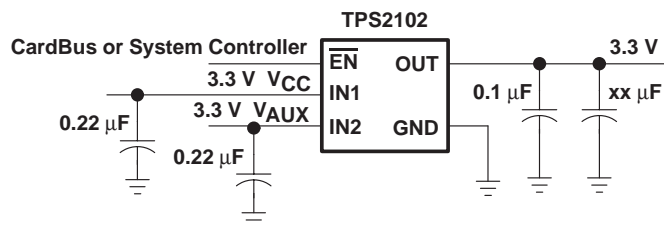

Figure 23

APPLICATION INFORMATION

Figure 24. Typical Application

power-supply considerations

A 0.22-µF ceramic bypass capacitor between IN and GND, close to the device is recommended. The output capacitor should be chosen based on the size of the load during the transition of the switch. A 220-µF capacitor is recommended for 100 mA loads. Typical output capacitors (xx µF, shown in Figure 24) required for a given load can be determined from Figure 16 which shows the output voltage droop when output is switched from IN2 to IN1. The output voltage droop is insignificant when output is switched from IN1 to IN2. Additionally, bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

power supply considerations (continued)

switch transition

The n-channel MOSFET on IN1 uses a charge pump to create the gate-drive voltage, which gives the IN1 switch a rise time of approximately 0.5 ms. The p-channel MOSFET on IN2 has a simpler drive circuit that allows a rise time of approximately 5 μs. Because the device has two switches and a single enable pin, these rise times are seen as transition times, from IN1 to IN2, or IN2 to IN1, by the output. The controlled transition times help limit the surge currents seen by the power supply during switching.

thermal protection

Thermal protection provided on the IN1 switch prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off at approximately 145°C (T_J). The switch remains off until the junction temperature has dropped approximately 10°C. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout

An undervoltage lockout function is provided to ensure that the power switch is in the off state at power-up. Whenever the input voltage falls below approximately 2 V, the power switch quickly turns off. This function facilitates the design of hot-insertion systems that may not have the capability to turn off the power switch before input power is removed. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. First, find r_{on} at the input voltage, and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 22 or Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to obtain a reasonable answer.
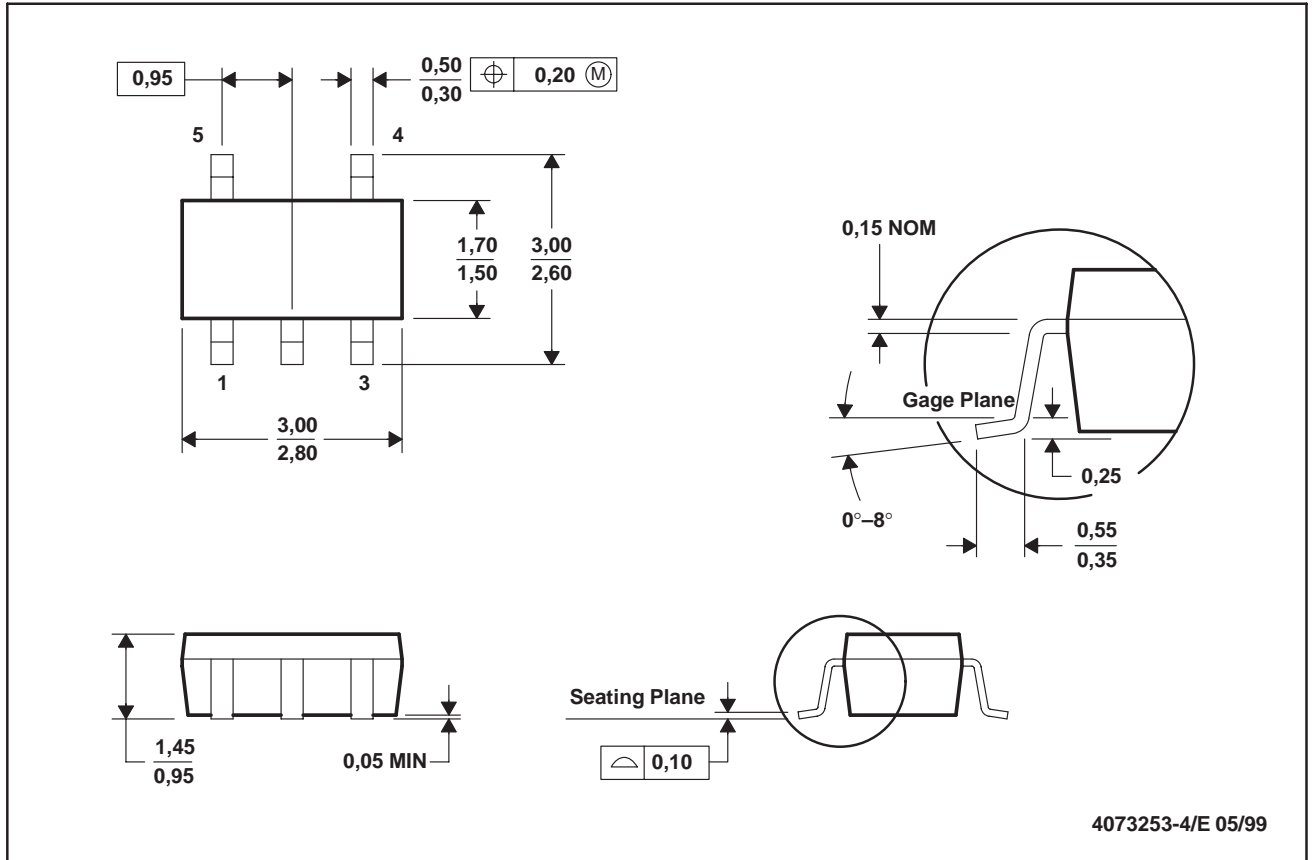
ESD protection

All TPS2102 and TPS2103 terminals incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model, 750-V CDM, and 200-V machine-model discharge as defined in MIL-STD-883C.

TEXAS
INSTRUMENTS

MECHANICAL DATA

DBV (R-PDSO-G5)   **PLASTIC SMALL-OUTLINE**

4073253-4/E 05/99

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MECHANICAL DATA

D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

	PINS **	8	14	16
DIM				
A MAX		0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN		0.189 (4,80)	0.337 (8,55)	0.386 (9,80)
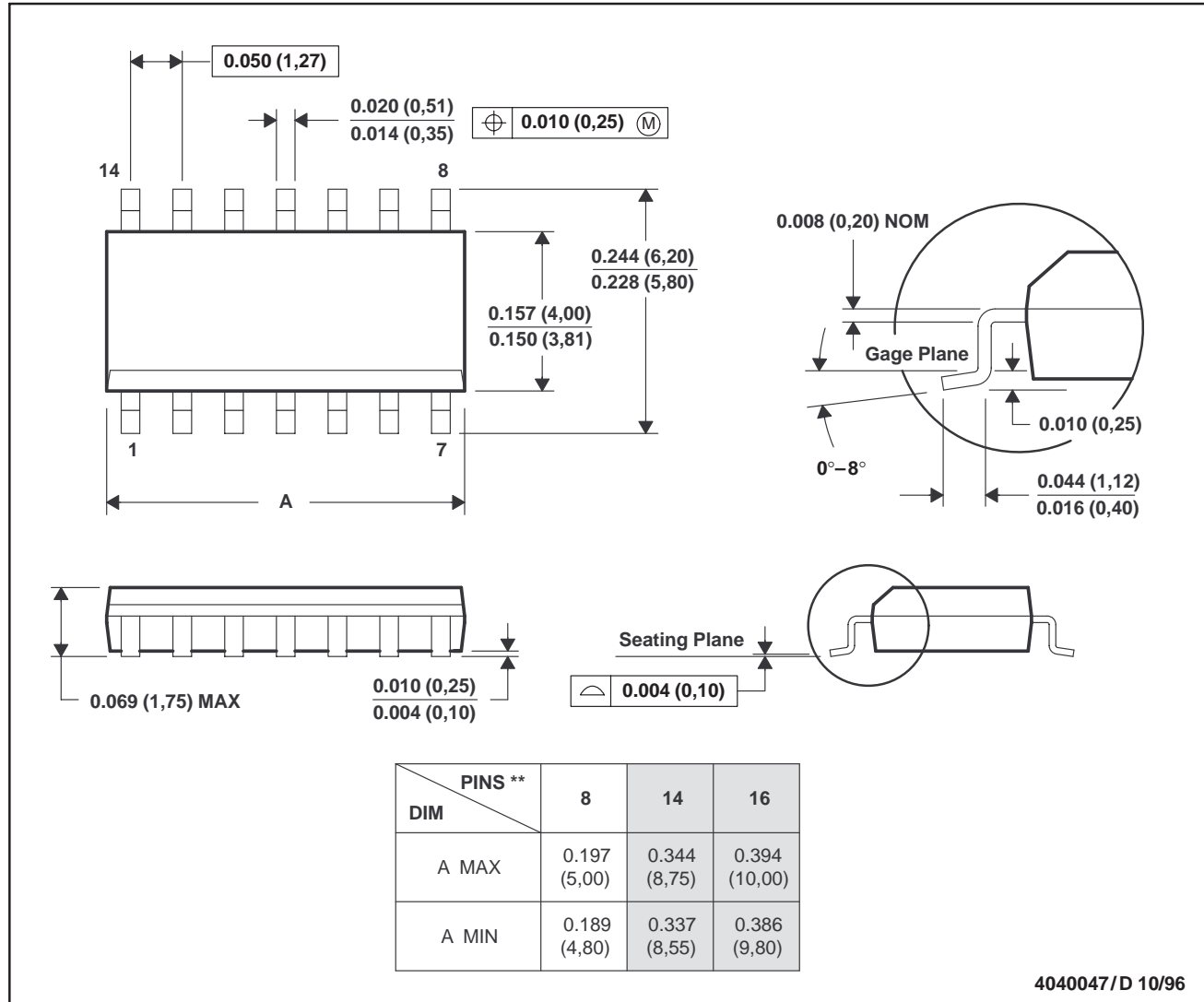
4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
          D. Falls within JEDEC MS-012

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