INTEGRATED CIRCUITS
UNITRODE

**UC1526A**
**UC2526A**
**UC3526A**

# Regulating Pulse Width Modulator

## FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation ($V_{IN}$ = $V_C$ = $V_{REF}$ = 5.0V)

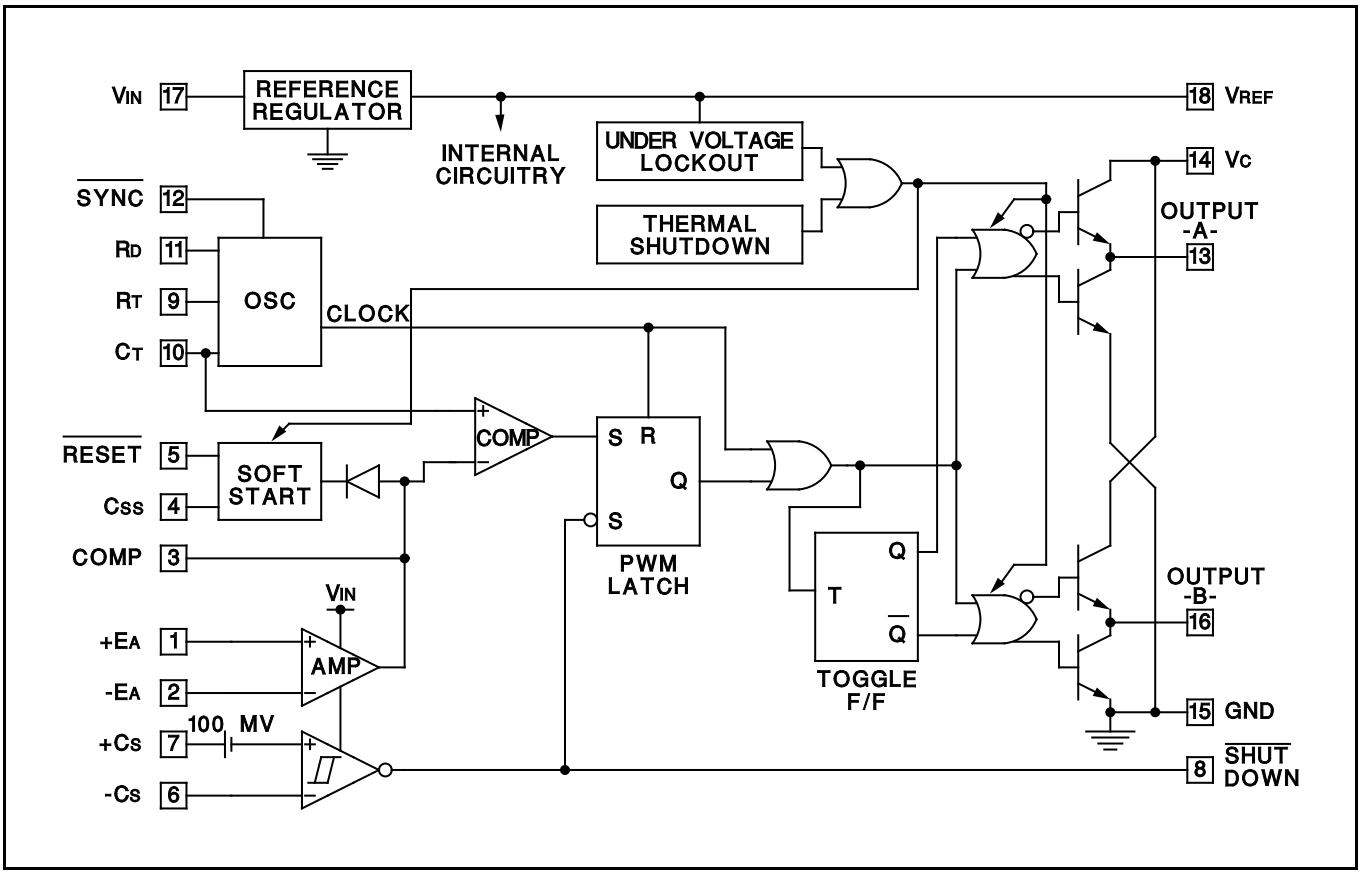
## DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting $V_{IN}$, $V_C$ and $V_{REF}$ to a precision 5V input supply. Consult factory for additional information.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage ($+V_{IN}$) . . . . . +40V
Collector Supply Voltage ($+V_C$) . . . . . +40V
Logic Inputs . . . . . -0.3V to +5.5V
Analog Inputs . . . . . -0.3V to $+V_{IN}$
Source/Sink Load Current (each output) . . . . . 200mA
Reference Load Current . . . . . 50mA
Logic Sink Current . . . . . 15mA
Power Dissipation at $T_A$ = +25°C (Note 2) . . . . . 1000mW
Power Dissipation at $T_C$ = +25°C (Note 2) . . . . . 3000mW
Operating Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

*Note 1: Values beyond which damage may occur.*
*Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.*

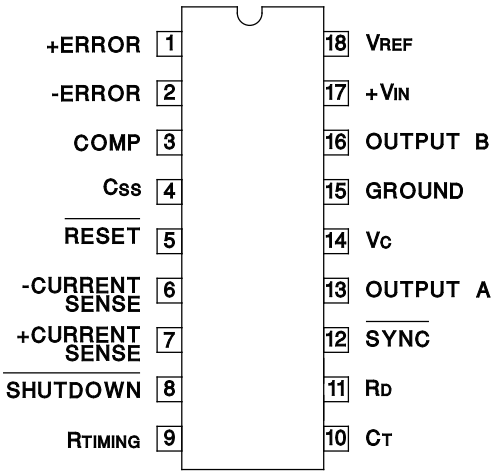
## RECOMMENDED OPERATING CONDITIONS

(Note 3)
Input Voltage . . . . . +7V to +35V
Collector Supply Voltage . . . . . +4.5V to +35V
Sink/Source Load Current (each output) . . . . . 0 to 100mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 1Hz to 600kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 400pF to 20µF
Available Deadtime Range at 40kHz . . . . . 1% to 50%
Operating Ambient Temperature Range
UC1526A . . . . . -55°C to +125°C
UC2526A . . . . . -25°C to +85°C
UC3526A . . . . . 0°C to +70°C

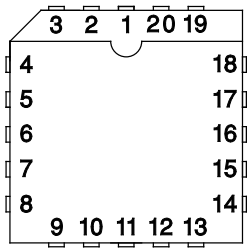
*Note 3: Range over which the device is functional and parameter limits are guaranteed.*

## CONNECTION DIAGRAMS

**DIL-18, SOIC-18 (TOP VIEW)**
**J or N Package, DW Package**




**PLCC-20, LCC-20**
**(TOP VIEW)**
**Q and L Packages**




| PACKAGE PIN FUNCTION | |
|---|---|
| **FUNCTION** | **PIN** |
| N/C | 1 |
| +ERROR | 2 |
| -ERROR | 3 |
| COMP. | 4 |
| $C_{SS}$ | 5 |
| $\overline{\text{RESET}}$ | 6 |
| - CURRENT SENSE | 7 |
| + CURRENT SENSE | 8 |
| $\overline{\text{SHUTDOWN}}$ | 9 |
| $R_{TIMING}$ | 10 |
| $C_T$ | 11 |
| $R_D$ | 12 |
| $\overline{\text{SYNC}}$ | 13 |
| OUTPUT A | 14 |
| $V_C$ | 15 |
| N/C | 16 |
| GROUND | 17 |
| OUTPUT B | 18 |
| $+V_{IN}$ | 19 |
| $V_{REF}$ | 20 |

**ELECTRICAL CHARACTERISTICS:** +$V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1526A / UC2526A | | | UC3526A | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Reference Section (Note 4)** | | | | | | | | |
| Output Voltage | $T_J$ = +25°C | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| Line Regulation | +$V_{IN}$ = 7 to 35V | | 2 | 10 | | 2 | 15 | mV |
| Load Regulation | $I_L$ = 0 to 20mA | | 5 | 20 | | 5 | 20 | mV |
| Temperature Stability | Over Operating $T_J$ (Note 5) | | 15 | 50 | | 15 | 50 | mV |
| Total Output Voltage Range | Over Recommended Operating Conditions | 4.90 | 5.00 | 5.10 | 4.85 | 5.00 | 5.15 | V |
| Short Circuit Current | $V_{REF}$ = 0V | 25 | 50 | 100 | 25 | 50 | 100 | mA |
| **Under-Voltage Lockout** | | | | | | | | |
| $\overline{\text{RESET}}$ Output Voltage | $V_{REF}$ = 3.8V | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| | $V_{REF}$ = 4.7V | 2.4 | 4.7 | | 2.4 | 4.8 | | V |
| **Oscillator Section (Note 6)** | | | | | | | | |
| Initial Accuracy | $T_J$ = +25°C | | ±3 | ±8 | | ±3 | ±8 | % |
| Voltage Stability | +$V_{IN}$ = 7 to 35V | | 0.5 | 1 | | 0.5 | 1 | % |
| Temperature Stability | Over Operating $T_J$ (Note 5) | | 2 | 6 | | 1 | 3 | % |
| Minimum Frequency | $R_T$ = 150kΩ, $C_T$ = 20µF (Note 5) | | | 1 | | | 1 | Hz |
| Maximum Frequency | $R_T$ = 2kΩ, $C_T$ = 470pF | 550 | | | 650 | | | kHz |
| Sawtooth Peak Voltage | +$V_{IN}$ = 35V | | 3.0 | 3.5 | | 3.0 | 3.5 | V |
| Sawtooth Valley Voltage | +$V_{IN}$ =7V | 0.5 | 1.0 | | 0.5 | 1.0 | | V |
| $\overline{\text{SYNC}}$ Pulse Width | $T_J$ = 25°C, $R_L$ = 2.7kΩ to $V_{REF}$ | | 1.1 | | | 1.1 | | µs |
| **Error Amplifier Section (Note 7)** | | | | | | | | |
| Input Offset Voltage | $R_S$ ≤ 2kΩ | | 2 | 5 | | 2 | 10 | mV |
| Input Bias Current | | | -350 | -1000 | | -350 | -2000 | nA |
| Input Offset Current | | | 35 | 100 | | 35 | 200 | nA |
| DC Open Loop Gain | $R_L$ ≥ 10MΩ | 64 | 72 | | 60 | 72 | | dB |
| HIGH Output Voltage | $V_{PIN\ 1}$ - $V_{PIN\ 2}$ ≥ 150mV, $I_{SOURCE}$ = 100µA | 3.6 | 4.2 | | 3.6 | 4.2 | | V |
| LOW Output Voltage | $V_{PIN\ 2}$ - $V_{PIN\ 1}$ ≥ 150mV, $I_{SINK}$ = 100µA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| Common Mode Rejection | $R_S$ ≤ 2kΩ | 70 | 94 | | 70 | 94 | | dB |
| Supply Voltage Rejection | +$V_{IN}$ = 12 to 18V | 66 | 80 | | 66 | 80 | | dB |
| **PWM Comparator (Note 6)** | | | | | | | | |
| Minimum Duty Cycle | $V_{COMPENSATION}$ = +0.4V | | | 0 | | | 0 | % |
| Maximum Duty Cycle | $V_{COMPENSATION}$ = +3.6V | 45 | 49 | | 45 | 49 | | % |
| **Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)** | | | | | | | | |
| HIGH Output Voltage | $I_{SOURCE}$ = 40µA | 2.4 | 4.0 | | 2.4 | 4.0 | | V |
| LOW Output Voltage | $I_{SINK}$ = 3.6mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| HIGH Input Current | $V_{IH}$ = +2.4V | | -125 | -200 | | -125 | -200 | µA |
| LOW Input Current | $V_{IL}$ = +0.4V | | -225 | -360 | | -225 | -360 | µA |
| Shutdown Delay | From Pin 8, $T_J$ = 25°C | | 160 | | | 160 | | ns |
| **Current Limit Comparator (Note 8)** | | | | | | | | |
| Sense Voltage | $R_S$ ≤ 50Ω | 90 | 100 | 110 | 80 | 100 | 120 | mV |
| Input Bias Current | | | -3 | -10 | | -3 | -10 | µA |
| Shutdown Delay | From pin 7, 100mV Overdrive, $T_J$ = 25°C | | 260 | | | 260 | | ns |

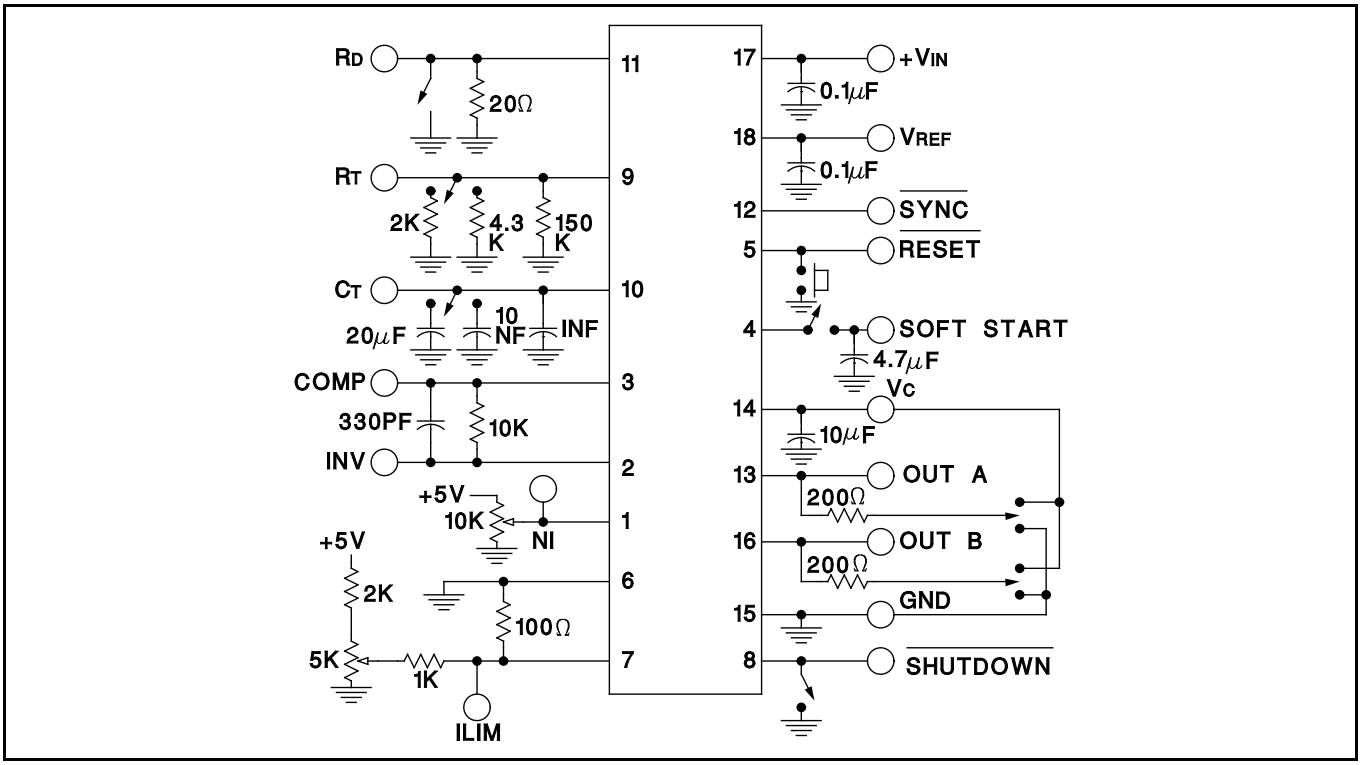
*Note 4: $I_L$ = 0mA.*
*Note 5: Guaranteed by design, not 100% tested in production.*
*Note 6: $F_{OSC}$ = 40kHz, ($R_T$ = 4.12kΩ ± 1%, $C_T$ = 0.01µF± 1%, $R_D$ = 0 Ω).*
*Note 7: $V_{CM}$ = 0 to +5.2V*
*Note 8: $V_{CM}$ = 0 to +12V.*
*Note 9: $V_C$ = +15V.*
*Note 10:$V_{IN}$ = +35V, $R_T$ = 4.12kΩ.*

**ELECTRICAL CHARACTERISTICS:** +$V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1526A UC2526A | | | UC3526A | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Soft-Start Section** | | | | | | | | |
| Error Clamp Voltage | $\overline{RESET}$ = +0.4V | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| $C_S$ Charging Current | $\overline{RESET}$ = +2.4V | 50 | 100 | 150 | 50 | 100 | 150 | µA |
| **Output Drivers (Each Output) (Note 9)** | | | | | | | | |
| HIGH Output Voltage | $I_{SOURCE}$ = 20mA | 12.5 | 13.5 | | 12.5 | 13.5 | | V |
| | $I_{SOURCE}$ = 100mA | 12 | 13 | | 12 | 13 | | V |
| LOW Output Voltage | $I_{SINK}$ = 20mA | | 0.2 | 0.3 | | 0.2 | 0.3 | V |
| | $I_{SINK}$ = 100mA | | 1.2 | 2.0 | | 1.2 | 2.0 | V |
| Collector Leakage | $V_C$ = 40V | | 50 | 150 | | 50 | 150 | µA |
| Rise Time | $C_L$ = 1000pF (Note 5) | | 0.3 | 0.6 | | 0.3 | 0.6 | µs |
| Fall Time | $C_L$ = 1000pF (Note 5) | | 0.1 | 0.2 | | 0.1 | 0.2 | µs |
| Cross-Conduction Charge | Per cycle, $T_J$ = 25°C | | 8 | | | 8 | | nC |
| **Power Consumption (Note 10)** | | | | | | | | |
| Standby Current | $\overline{SHUTDOWN}$ = +0.4V | | 14 | 20 | | 14 | 20 | mA |

*Note 4: $I_L$ = 0mA.*
*Note 5: Guaranteed by design, not 100% tested in production.*
*Note 6: $F_{OSC}$ = 40kHz, ($R_T$ = 4.12kΩ ± 1%, $C_T$ = 0.01µF± 1%, $R_D$ = 0 Ω).*
*Note 7: $V_{CM}$ = 0 to +5.2V*
*Note 8: $V_{CM}$ = 0 to +12V.*
*Note 9: $V_C$ = +15V.*
*Note 10: $V_{IN}$ = +35V, $R_T$ = 4.12kΩ.*

## Open Loop Test Circuit UC1526A



## APPLICATIONS INFORMATION

### Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

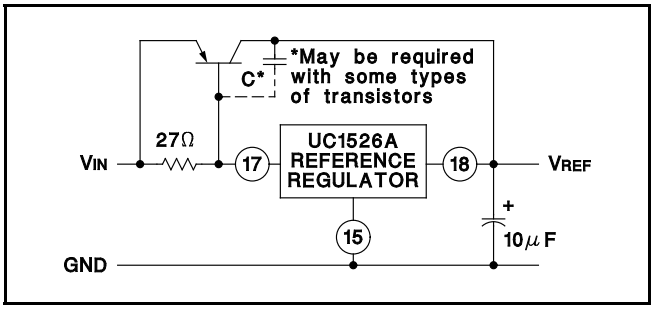



**Figure 1. Extending Reference Output Current**

### Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

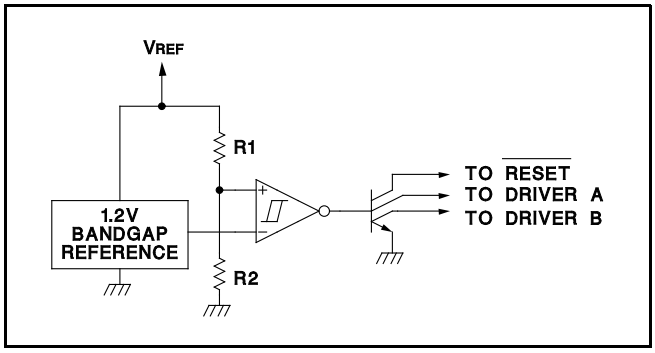



**Figure 2. Under-Voltage Lockout Schematic**

### Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100μA current source to charge CS. Q2 clamps the error amplifier output to 1VBE above the voltage on CS. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

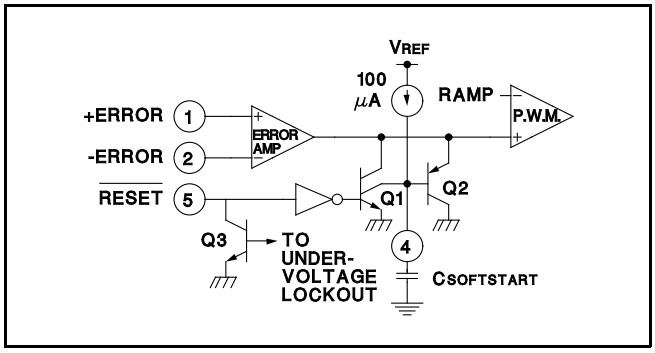



**Figure 3. Soft-Start Circuit Schematic**

### Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start

## APPLICATIONS INFORMATION (cont.)

capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

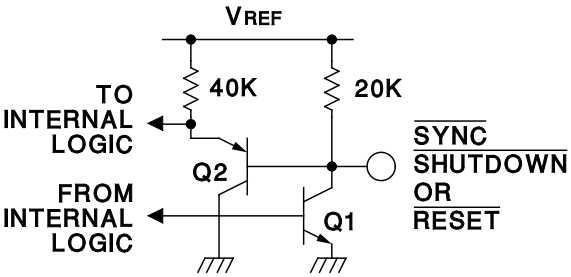



**Figure 4. Digital Control Port Schematic**

### Oscillators

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD= 0Ω (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +VC terminal is the same as the oscillator frequency.

2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by 400ns/Ω.

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the $\overline{\text{SYNC}}$ frequency.

A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

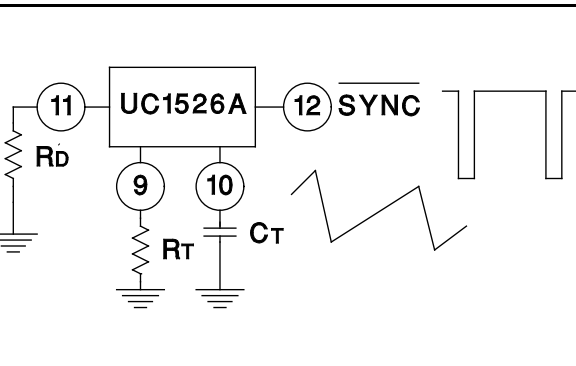



**Figure 5. Oscillator Connections and Waveforms**

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.

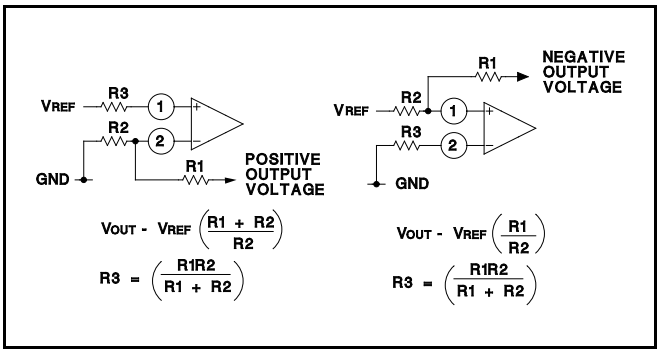



**Figure 6. Error Amplifier Connections**

### Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

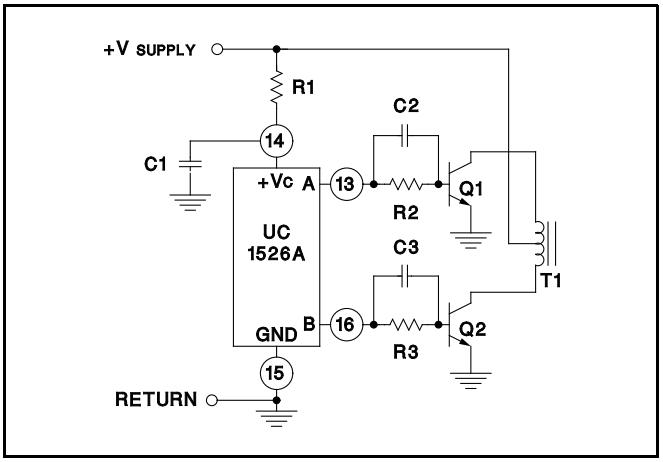



**Figure 7. Push-Pull Configuration**

## APPLICATIONS INFORMATION (cont.)

### Output Drivers

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

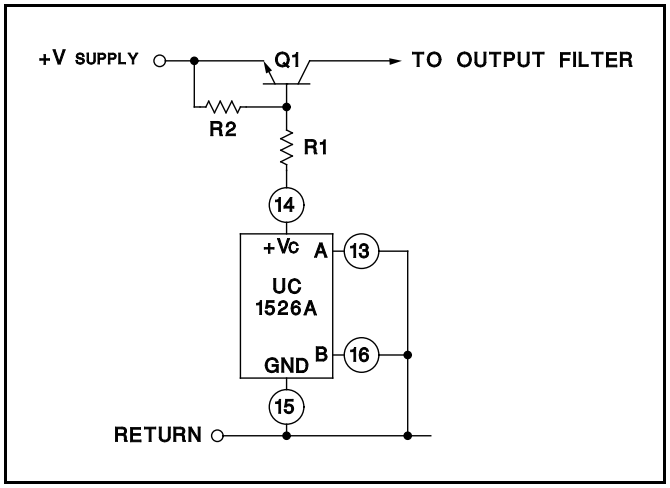



**Figure 8.** Single-Ended Configuration

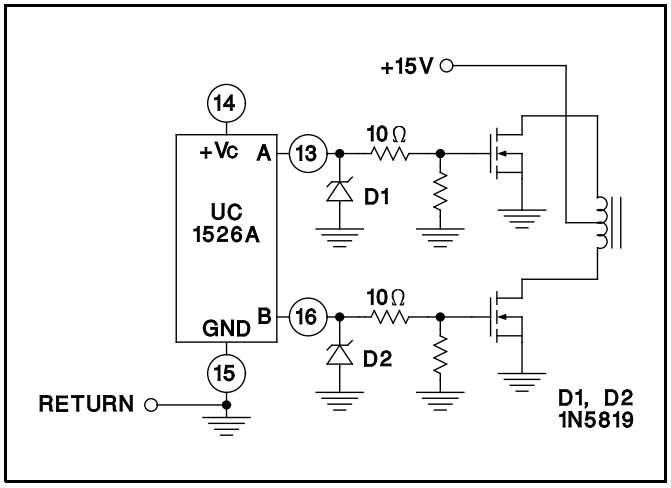
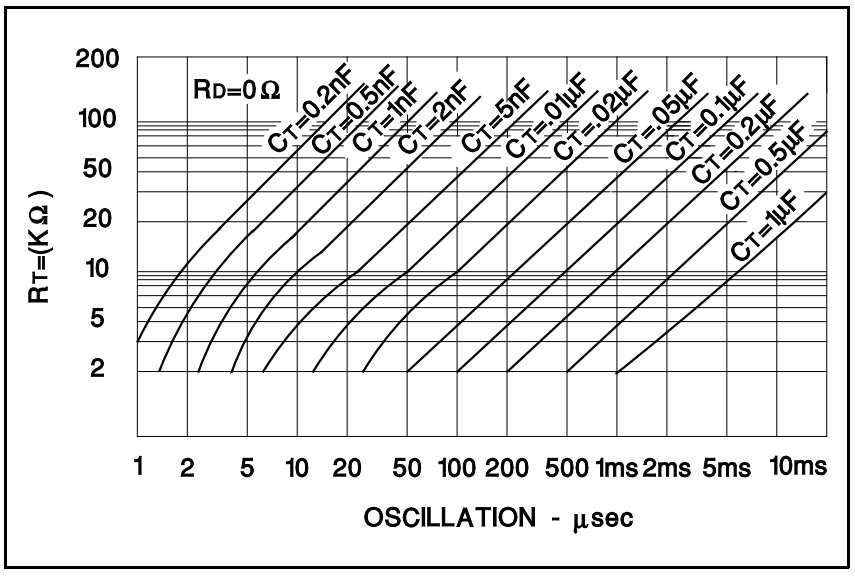


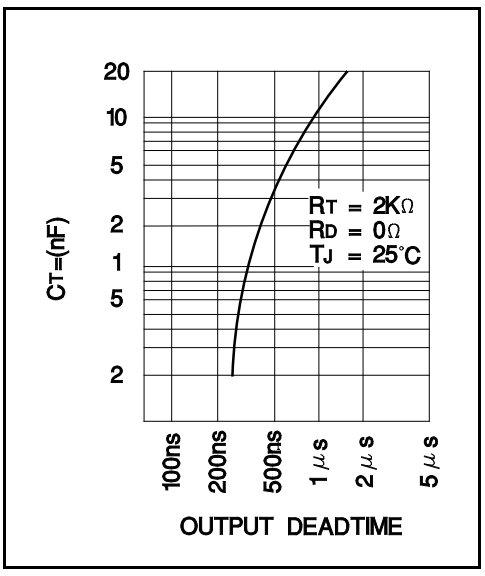

**Figure 9.** Driving N-Channel Power MOSFETs

## TYPICAL CHARACTERISTICS

**OSCILLATOR PERIOD vs RT and CT**

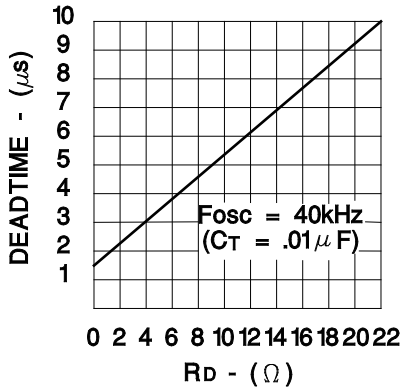



**OUTPUT BLANKING**

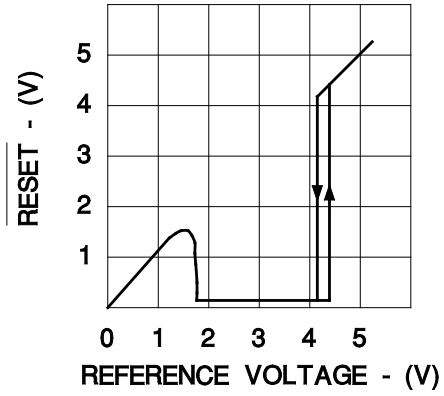


## TYPICAL CHARACTERISTICS (Cont.)

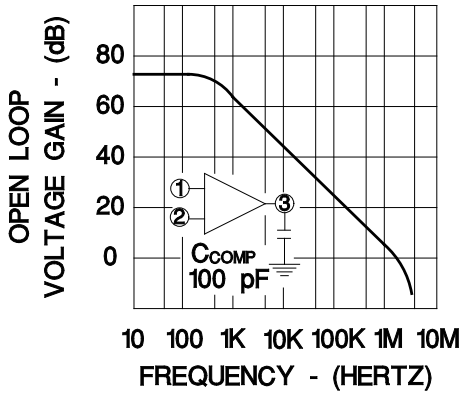
**Output Driver Deadtime vs. $R_D$ Value**



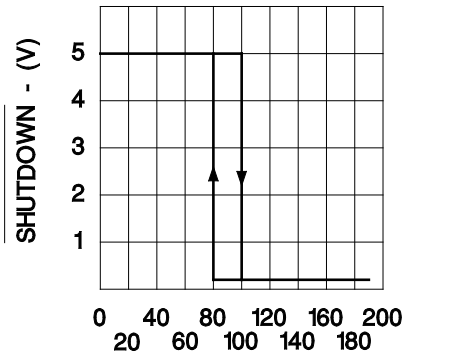

**Under Voltage Lockout Characteristic**



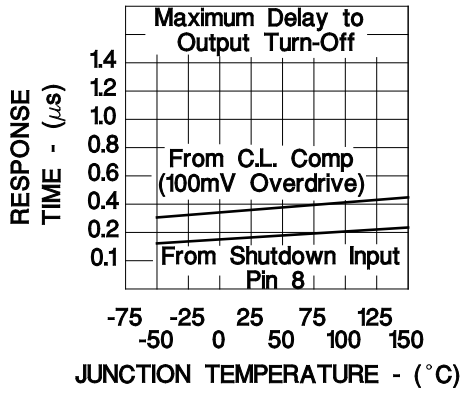

**Error Amplifier Open Loop Gain vs. Frequency**



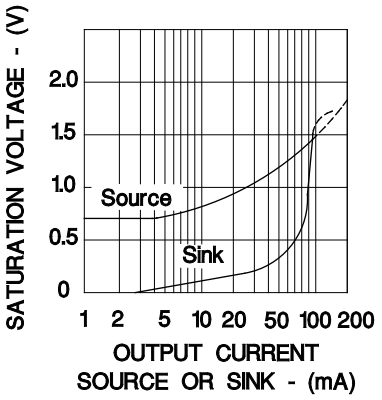

**Current Limit Transfer Function**




**Shutdown Delay**




**Output Driver Saturation Voltage**

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